Bt8040

T-1 Tri-Port Memory

Distinguishing Features

- 64 x 8 Bit Static Memory
- Single +5 V Supply
- Two Independent Read Ports
- Multiple Read Access Time < 430 ns (Worst Case)
- Selectable Random- or Sequential-Address Write Operation
- On-Chip Sequential Address Counter
- Three-State Drivers for Chip-Selectable Bus Operation
- 40-Pin Dual In-line Package
- LSTTL Schottky-Compatible (12 kΩ Pullup to Drive CMOS)

Applications

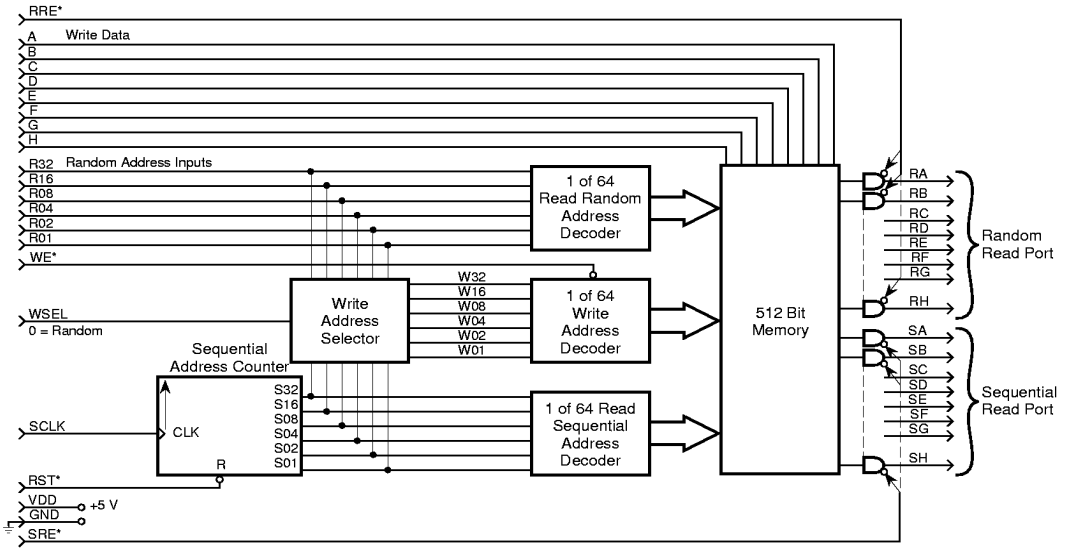
- Time-Division Multiplex (TDM) Digital Switching
- Data and Control Stores
  - -TDM Sequential Machines
  - -Elastic Stores
  - -Hardware/Software Control Interfaces
  - -I/O Buffers

Product Description

The T-1 Tri-Port Memory circuit is designed to function as an assembly point and temporary storage area for 8-bit T-1 data. It provides 64 8-bit locations of on-chip RAM, which can be accessed through external addressing or internal sequential addressing.

The Tri-Port Memory operates on a single 5 V supply and is low-power TTL Schottky compatible. The circuit is packaged in a 40-pin Dual In-line Package (DIP) and is illustrated in Figure 1.

Functional Block Diagram



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L804001 Rev. A

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Tri-Port Memory Operation

The Tri-Port Memory device accepts 8-bit parallel input data on lines A–H. This data is stored in an internal memory location that is selected by either random address lines R01–R32 or by the device's sequential address counter. Write Select signal (WSEL) determines the source of the address. In the logical zero state, WSEL selects the random address. In the logical one state, WSEL selects the internal sequential address.

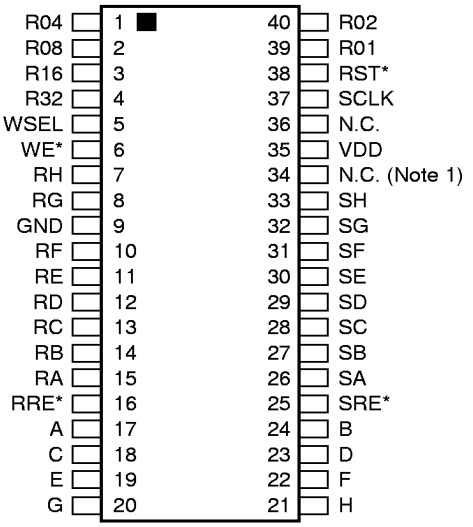
The state of Write Enable signal (WE*) determines whether the data on lines A–H will be written into memory. Data will be written into memory only when WE* goes low (to a logical zero state) and the address inputs have stabilized.

The on-chip, 6-bit sequential address counter is a binary counter that increments on each positive transition of Sequential Clock (SCLK). When the counter attains binary 111111, the next positive transition on SCLK will clear it to binary 000000. The counter will also be cleared unconditionally if the Reset signal (RST*) has been set to logical zero when the positive transition of SCLK occurs.

The Sequential Read Enable signal (SRE*) enables sequentially addressed read operations. If SRE* is logical zero, the sequential accessed data outputs (SA–SH) will become valid within 430 ns after the next positive transition on SCLK. If SRE* is a logical one, and 350 ns have elapsed since the positive transition of SCLK, the sequential accessed data outputs will become valid 80 ns after the negative transition of SRE*. The sequential read data will cease to be valid 100 ns after the negative transition of SRE* or 20 ns after the next positive transition of SCLK, becoming valid with the content of the next sequential location within 430 ns of that SCLK transition.

The Random Read Enable signal (RRE*) enables random-accessed read operations. If RRE* is a logical zero, the random accessed data outputs (RA–RH) will become valid within 380 ns after the random address lines have stabilized. If RRE* is a logical one, and 300 ns have elapsed since the random address lines have stabilized, the random accessed data outputs will become valid 80 ns after the negative transition of RRE*. The random accessed data outputs will cease to be valid 100 ns after a positive transition of RRE* or 20 ns after the random address input lines change, becoming valid with the contents of the newly addressed location within 380 ns after the random address inputs have stabilized.

In the case of a same location read/write cycle, the sequential and/or random data outputs will cease to be valid after a negative transition of WE*, and will become valid with the newly written contents within 340 ns of that transition. Control of this parameter minimizes external circuitry required for resolution of read-write contention.



Note 1: Pin 34 has an output signal applicable only to Brooktree testing. Make no connection to this pin.

Figure 1. Pin Configuration.

Recommended Operating Conditions

Signal	Setup		Hold	
	Measure to	ns	Measure to	ns
SCLK ↑	WE* ↓	300	WE* ↑	0
WSEL	WE* ↓	280	WE* ↑	0
R01–R32	WE* ↓	250	WE* ↑	0
A–H	WE* ↑	150	WE* ↑	100
RST*	SCLK ↓	180	SCLK ↑	0

Minimum Setup/Hold Times

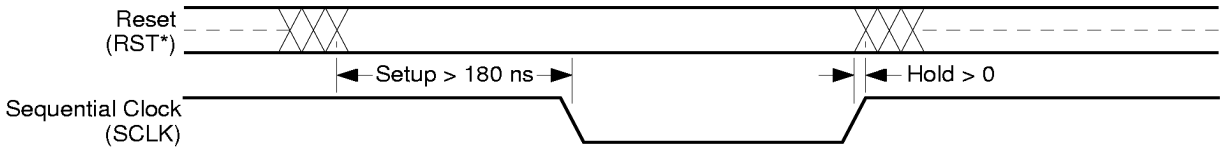
Signal	Minimum Pulse Width
WE* (=0)	170 ns
SCLK	220 ns

Minimum Pulse Widths

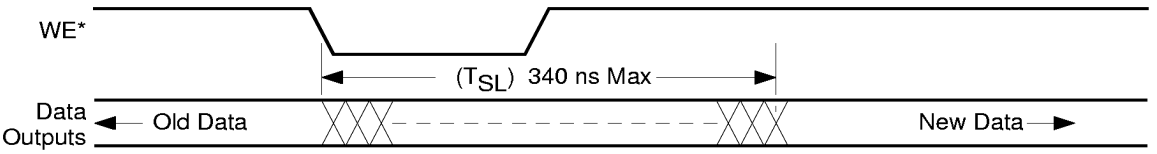
Parameter	Symbol	Min	Max	Unit
Random Read Access Time	t_{RA}	0	380	ns
Sequential Read Access Time	t_{SA}	0	430	ns
Read Port Disable (to HI-Z)	t_{PD}	0	100	ns
Read Port Enable	t_{PE}	0	80	ns
Same-Location Read After Write	t_{SL}	0	340	ns

Propagation Delays

Timing Diagrams

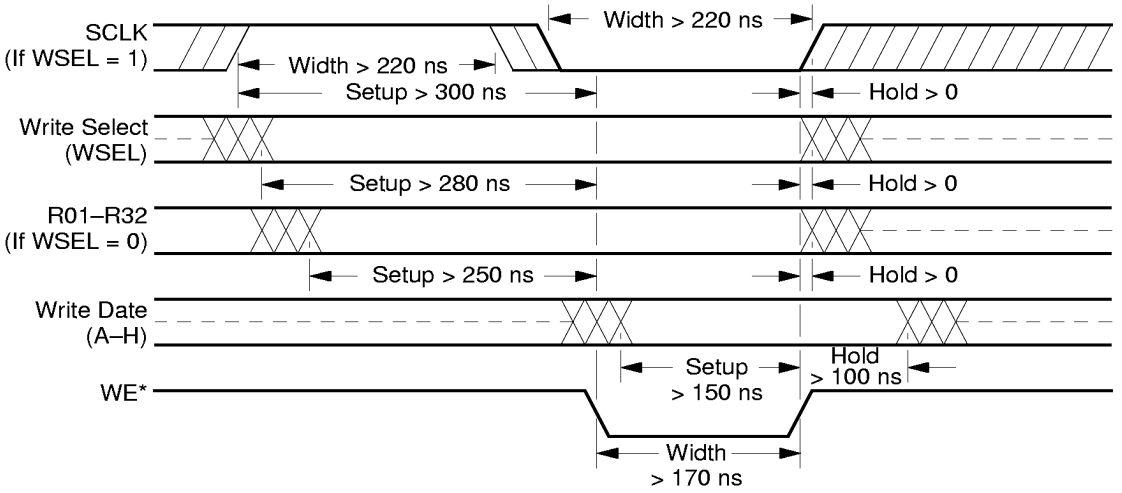


Sequential Counter Reset Setup and Hold Timing.



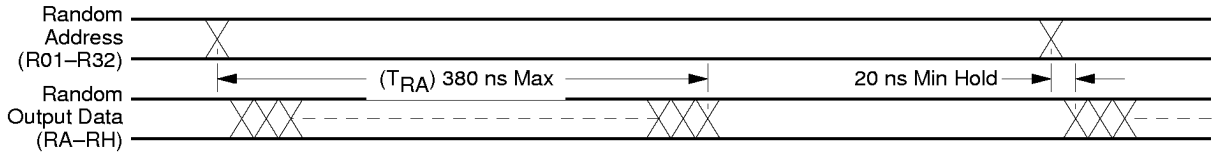
Note: Random write *always* affects random read outputs; sequential write *always* affects sequential read outputs. Either write (random or sequential) *will* affect the opposite read output, if, and only if, the random address and sequential address are equal.

Read Outputs at Same Location as Write (All Other Inputs Stable).

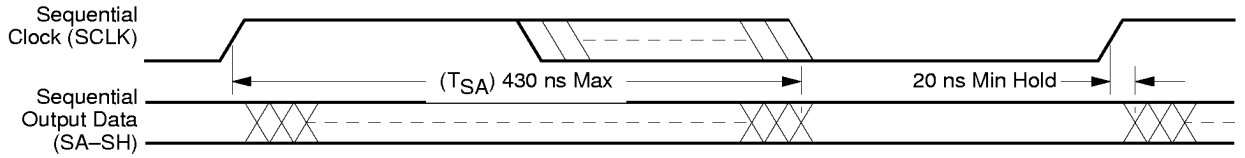


Write Setup and Hold Timing.

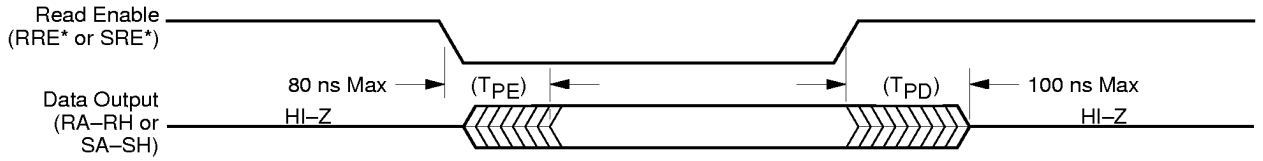
Timing Diagrams *(continued)*



Random Read (RRE* = 0 and WE* = 1).



Sequential Read (SRE* = 0 and WE* = 1).



Read Port Enable/Disable (Address Stable and WE* = 1).

Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	–55 to +150	°C

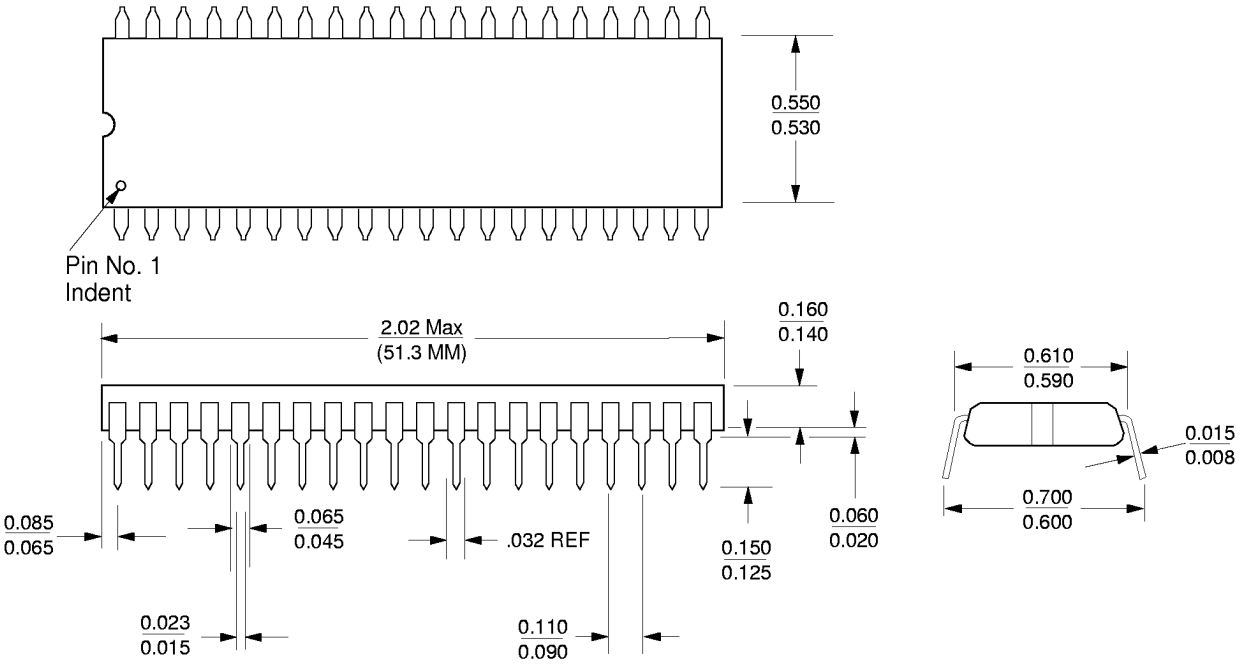
Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

V_{DD} = +5 V ±5%, V_{SS} = 0 V, and T_A = 25°C

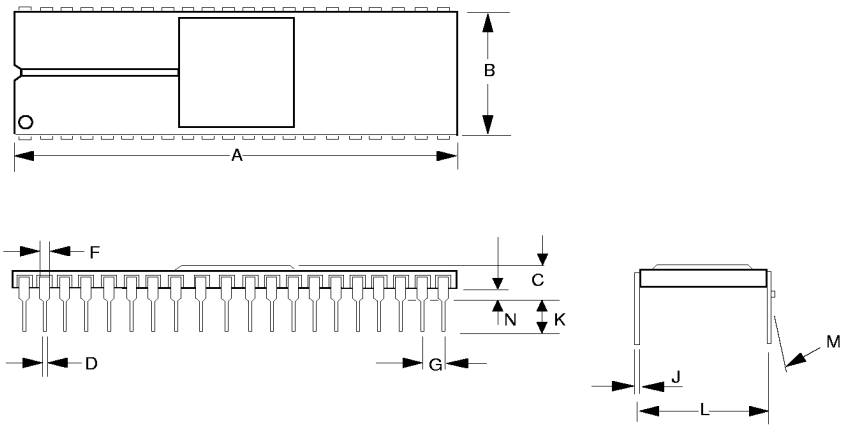
Parameter	Symbol	Min	Max	Unit
Input Logical One Voltage	V_{IH}	2.0		V
Input Logical Zero Voltage	V_{IL}		0.8	V
Input Logical One Voltage	V_{OL}	2.4		V
Output Logical Zero Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	–100		µA
Output Sink Current	I_{OL}	400		µA
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation (at 25°C)	P_{DSS}		300	mW

Package Dimensions



Note: Dimensions are given in inches.

40-Pin Plastic DIP



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	50.29	51.31	1.980	2.020
B	14.73	15.24	0.580	0.600
C	3.30	4.32	0.130	0.170
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.06	0.100	0.160
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	1.02	1.52	0.040	0.060

40-Pin Ceramic DIP

Ordering Information

Part Number	Package	Temperature Range
Bt8040KP	40-Pin Plastic DIP	0°C to 70°C
Bt8040KC	40-Pin Ceramic DIP	0°C to 70°C

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CAUTION

ESD-sensitive device.
Permanent damage may occur on unconnected devices subjected to high-energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.

Do not insert this device into powered sockets.

Remove power before insertion or removal.

PRINTED IN THE USA
Print date:12/10/93

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