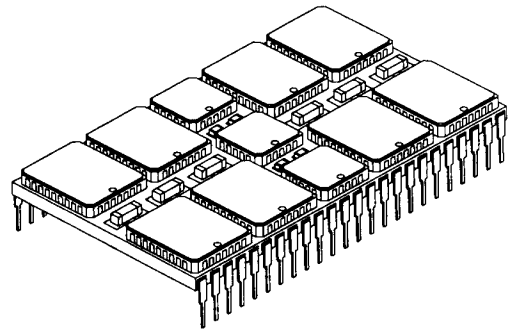
DPS45128

512K X 8 CMOS SRAM MODULE



DESCRIPTION:

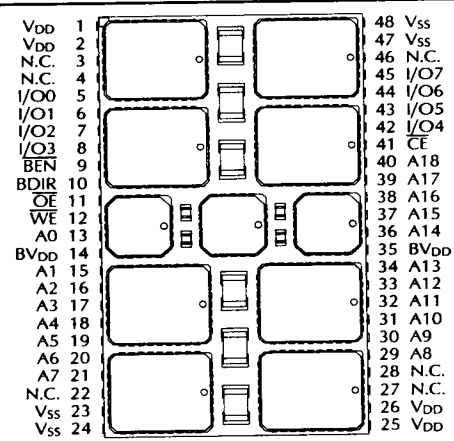
The DPS45128 is a four Megabit Static Random Access Memory module organized as 512K X 8 bit, consisting of sixteen DPS92256G, 32K X 8 SRAM's plus complete signal and I/O interface logic and on-board capacitors.

The DPS45128 is ideally suited for high density, high performance applications where fast access time and ease of use is required.

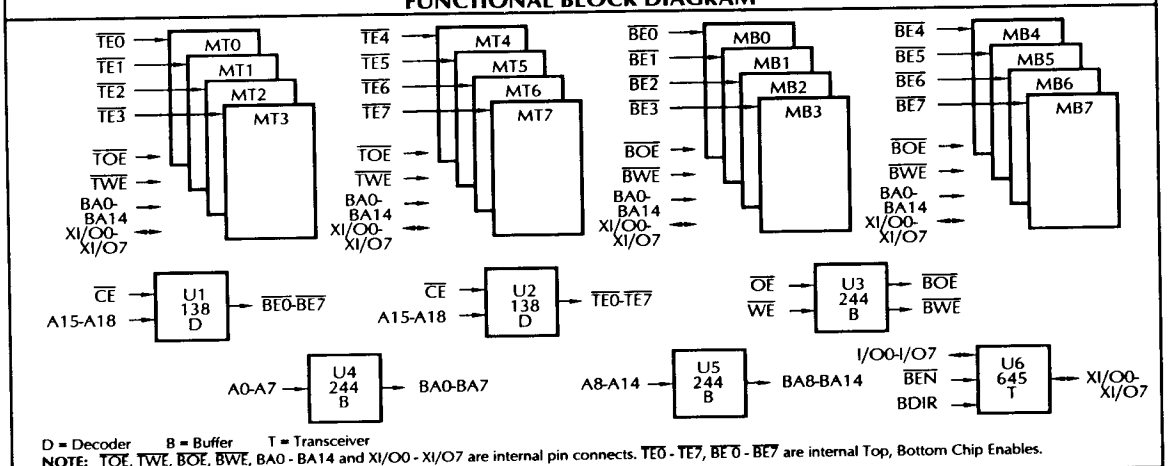
FEATURES:

- Organization Available: 512K x 8
- Fast Access Times:
  55, 70, 85, 100, 120, 135, 150, 170, 200ns (max.)
- Fully Static Operation; No Clock or Refresh Required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Fully Buffered and Decoded Memory Array
- Common Data Input and Output
- Low Data Retention Voltage: 2.0V min.
- Standard 48-Pin DIP Package
- Available with all Semiconductor Components used in the Construction of the Module Compliant to MIL-STD-883; Class B

PIN-OUT DIAGRAMS



FUNCTIONAL BLOCK DIAGRAM



NOTE: TOE, TWE, BOE, BWE, BA0 - BA14 and XI/O0 - XI/O7 are internal pin connects. TE0 - TE7, BE0 - BE7 are internal Top, Bottom Chip Enables.

PIN NAMES	
A0 - A18	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{BEN}$	Buffer Enable
BDIR	Buffer Direction
V_{DD}	Power (+5V)
BV_{DD}	Buffer Power (+5V)
V_{SS}	Ground
N.C.	No Connect

RECOMMENDED OPERATING RANGE[1]

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.65	V

DC OUTPUT CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 2.1mA	-	0.4	V

ABSOLUTE MAXIMUM RATINGS[3]

Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to + 150	°C
T_{BIAS}	Temperature Under Bias	-55 to + 125	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
BV_{DD}	Buffer Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} + 0.5	V

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BEN}$	BDIR	I/O	Supply Current
Disabled	H	X	X	H	X	High-Z	Standby
Read	L	H	L	L	H	D_{OUT}	Active
Write	L	L	X	L	L	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz

Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	25	pF	V_{IN} = 0V
C_{CE}	Chip Enable	25		
C_{WE}	Write Enable	12		
C_{OE}	Output Enable	12		
C_{BEN}	Buffer Enable	85		
C_{BDIR}	Buffer Direction	12		
$C_{I/O}$	Data Input/Output	80		

DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-20	+20	-20	+20	-20	+20	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-20	+20	-20	+20	-20	+20	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		260 (75)		350 (80)		430 (80)	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		300 (150)		395 (155)		470 (155)	mA
I_{SB1}	Full Standby Supply Current (CMOS)	$V_{IN} \le V_{DD}$ -0.2V or $V_{IN} \le$ 0.2V $\overline{CE} \ge V_{DD}$ -0.2V		170 (5)		250 (5)		330 (5)	mA
I_{SB2}	Standby Supply (TTL)	$\overline{CE}$ = V_{IH}		460 (95)		570 (105)		570 (105)	mA
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V		5 (0.185)		6 (0.500)		10 (8)	mA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V		6 (0.25)		6.5 (0.60)		13 (10)	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

NOTE: Values for speeds 120, 135, 150, 170, and 200ns (max.) are represented in parentheses. I_{IN}, I_{OUT}, V_{OL} and V_{OH} are valid for all speeds.

DATA RETENTION CHARACTERISTICS						
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	Data Retention Voltage	$\overline{CE} \geq V_{DD}$ -0.2V	2.0	5.0	5.5	V
t_{CDRS}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	t_{RC}			ns

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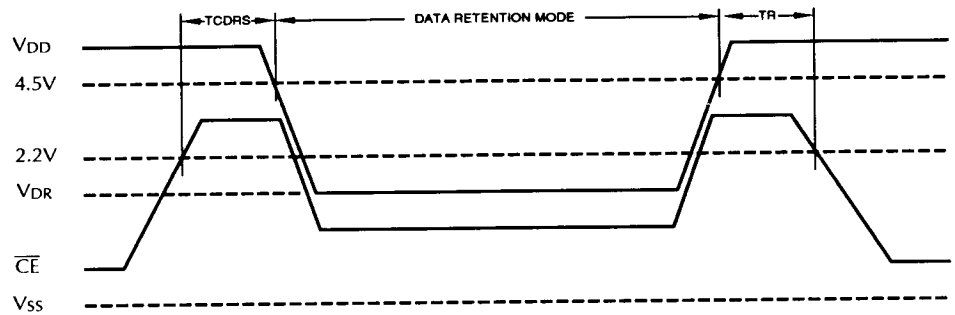
DATA RETENTION WAVEFORM

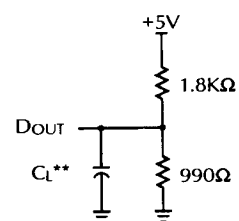


AC TEST CONDITIONS: Including Programming	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Time	≤ 5ns *
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

* Trasnsition measured between 0.8V and 2.2V.

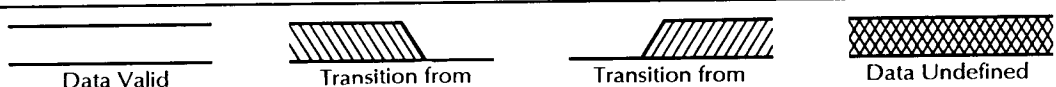
Figure 1. Output Load

** Including Probe and Jig Capacitance.



Output Load		
Float	C_L	Parameters Measured
1	100 pF	except t_{LZ} and t_{HZ}
2	5 pF	t_{LZ} and t_{HZ}

WAVEFORM KEY



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

No.	Symbol	Parameter	-55		-70		-85		-100		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	55		70		85		100		ns
2	t_{AA}	Address Access Time		55		70		85		100	ns
3	t_{CO}	Chip Enable to Output Valid		55		70		85		100	ns
4	t_{OV}	Output Enable to Output Valid		25		30		35		50	ns
5	t_{OH}	Output Hold from Address Change		10		10		10		10	ns
6	t_{DRS}	BDIR Setup before Output Enable	15		15		15		15		ns
7	t_{LZ}	$\overline{BEN}$ to Output LOW-Z [4] (BDIR HIGH)	10		10		10		10		ns
8	t_{HZ}	$\overline{BEN}$ to Output HIGH-Z [4]		15		15		15		15	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [8, 9]

No.	Symbol	Parameter	-55		-70		-85		-100		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
9	t_{WC}	Write Cycle Time	55		70		85		100		ns
10	t_{AW}	Address Valid to End of Write	50		60		70		80		ns
11	t_{CW}	Chip Enable to End of Write	50		60		70		80		ns
12	t_{DW}	Data Valid to End of Write	25		30		35		40		ns
13	t_{DH}	Data Hold Time	3		3		3		3		ns
14	t_{WP}	Write Pulse Width	40		45		50		60		ns
15	$t_{AS\ (\overline{CE})}$	Chip Enable Start from Address Start *		5		5		5		5	ns
16	$t_{AS\ (\overline{BEN})}$	Buffer Enable Start from Address Start *		10		10		10		10	ns
17	t_{AH}	Write Recovery Time	0		0		0		0		ns
18	t_{DRS}	BDIR Setup Time to Data Valid	12		12		12		12		ns
19	t_{DRH}	BDIR Hold from Data Valid	16		21		26		31		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

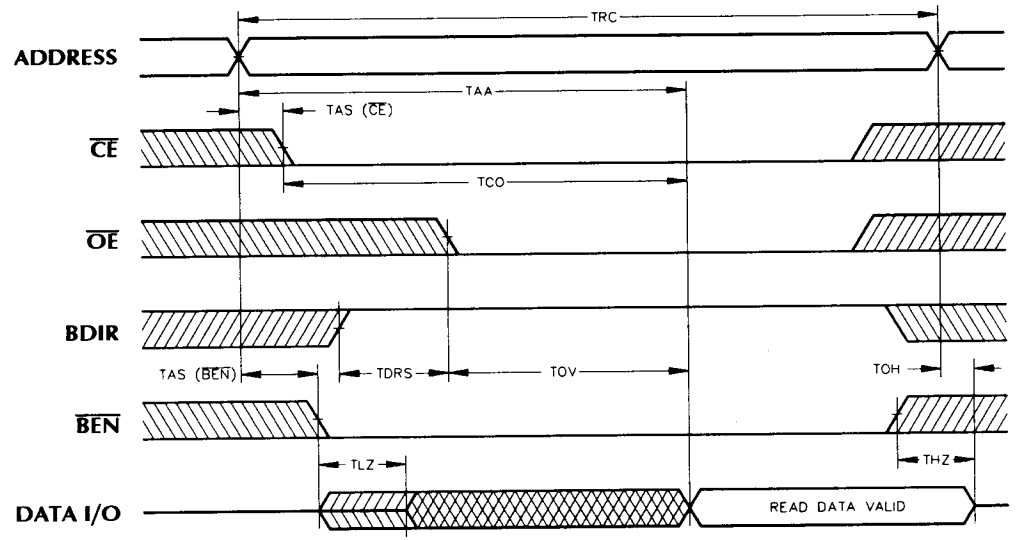
No.	Symbol	Parameter	-120		-135		-150		-170		-200		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	120		135		150		170		200		ns
2	t_{AA}	Address Access Time		120		135		150		170		200	ns
3	t_{CO}	Chip Enable to Output Valid		120		135		150		170		200	ns
4	t_{OV}	Output Enable to Output Valid		60		60		60		75		80	ns
5	t_{OH}	Output Hold from Address Change		22		22		22		22		22	ns
6	t_{DRS}	BDIR Setup before Output Enable	15		15		15		15		15		ns
7	t_{LZ}	$\overline{BEN}$ to Output LOW-Z [4] (BDIR HIGH)	10		10		10		10		10		ns
8	t_{HZ}	$\overline{BEN}$ to Output HIGH-Z [4]		15		15		15		15		15	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [8, 9]

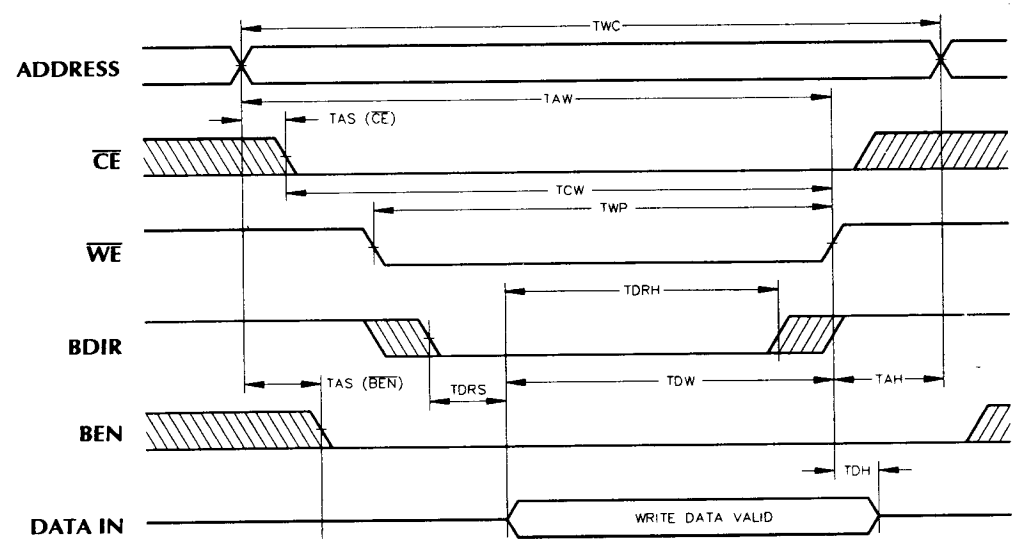
No.	Symbol	Parameter	-120		-135		-150		-170		-200		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
9	t_{WC}	Write Cycle Time	120		135		150		170		200		ns
10	t_{AW}	Address Valid to End of Write	100		110		120		140		170		ns
11	t_{CW}	Chip Enable to End of Write	100		110		120		140		170		ns
12	t_{DW}	Data Valid to End of Write	55		60		65		75		90		ns
13	t_{DH}	Data Hold Time	0		0		0		0		0		ns
14	t_{WP}	Write Pulse Width	70		75		80		90		100		ns
15	$t_{AS\ (\overline{CE})}$	Chip Enable Start from Address Start *		5		5		5		5		5	ns
16	$t_{AS\ (\overline{BEN})}$	Buffer Enable Start from Address Start *		10		10		10		10		10	ns
17	t_{AH}	Write Recovery Time	0		0		0		0		0		ns
18	t_{DRS}	BDIR Setup Time to Data Valid	12		12		12		12		12		ns
19	t_{DRH}	BDIR Hold from Data Valid	43		48		53		63		78		ns

* Valid for both Read and Write Cycles.

READ CYCLE



WRITE CYCLE: OE is HIGH.



ORDERING INFORMATION

DP S45128 – XXX X

PREFIX | DEVICE TYPE | SPEED | GRADE

GRADE		
C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	−40°C to +85°C
M	MILITARY	−55°C to +125°C
B *	MIL−PROCESSED	−55°C to +125°C

SPEED	
55	55ns
70	70ns
85	85ns
100	100ns
120	120ns
135	135ns
150	150ns
170	170ns
200	200ns

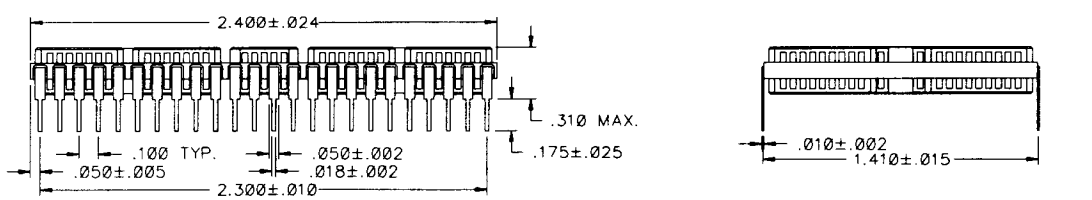
DEVICE TYPE: 512KX8 CMOS SRAM 48−PIN DIP

* B grade modules are available with all semiconductor devices compliant to MIL-STD- 883C.

NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min.= -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500mV from steady state voltage.
6. Some AC Operating Conditions and Characteristics may vary on buffers and transceivers due to propagation delays added by these logic devices.

MECHANICAL DRAWING



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