ADE-203-072C(Z)
Rev. 3
Jan.08,1994
Target Specification

HM67W1664 Series

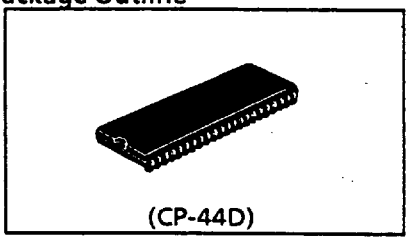
65536-Word x 16-Bit High Speed Bi-CMOS Static RAM

• DESCRIPTION

The HM67W1664 is asynchronous high speed static RAM organized as 64K word x 16bit. These operate **3.3V**. It realizes high speed access time of 10/12ns by employing 0.5μm Bi-CMOS process technology.

It is most appropriate for applications which require high speed, high density memory and word width configuration, such as cache and buffer memory.

Package Outline



(CP-44D)

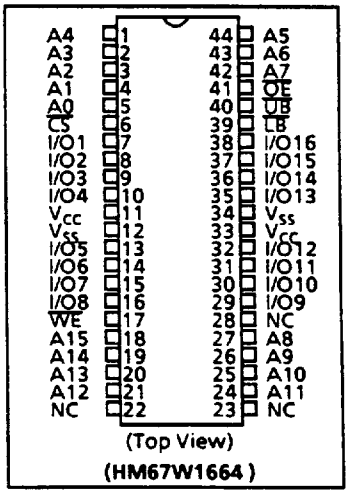
• FEATURES

- Single **3.3V** supply
- Fast Access Times: **10/12**ns(max)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Directly LV TTL compatible
  All inputs and outputs
- Low Active Power
  900/792mW max
- 400-mil 44-pin SOJ package
- Center Vcc and Vss type pinout

• ORDERING INFORMATION

Type NO.	Organization	Access time	package
HM67W1664JP-10	64K x 16	10ns	400mil 44pin plastic SOJ (CP-44D)
HM67W1664JP-12		12ns	

Pin Arrangement



(Top View)

(HM67W1664)

• Pin Description

(HM67W1664)

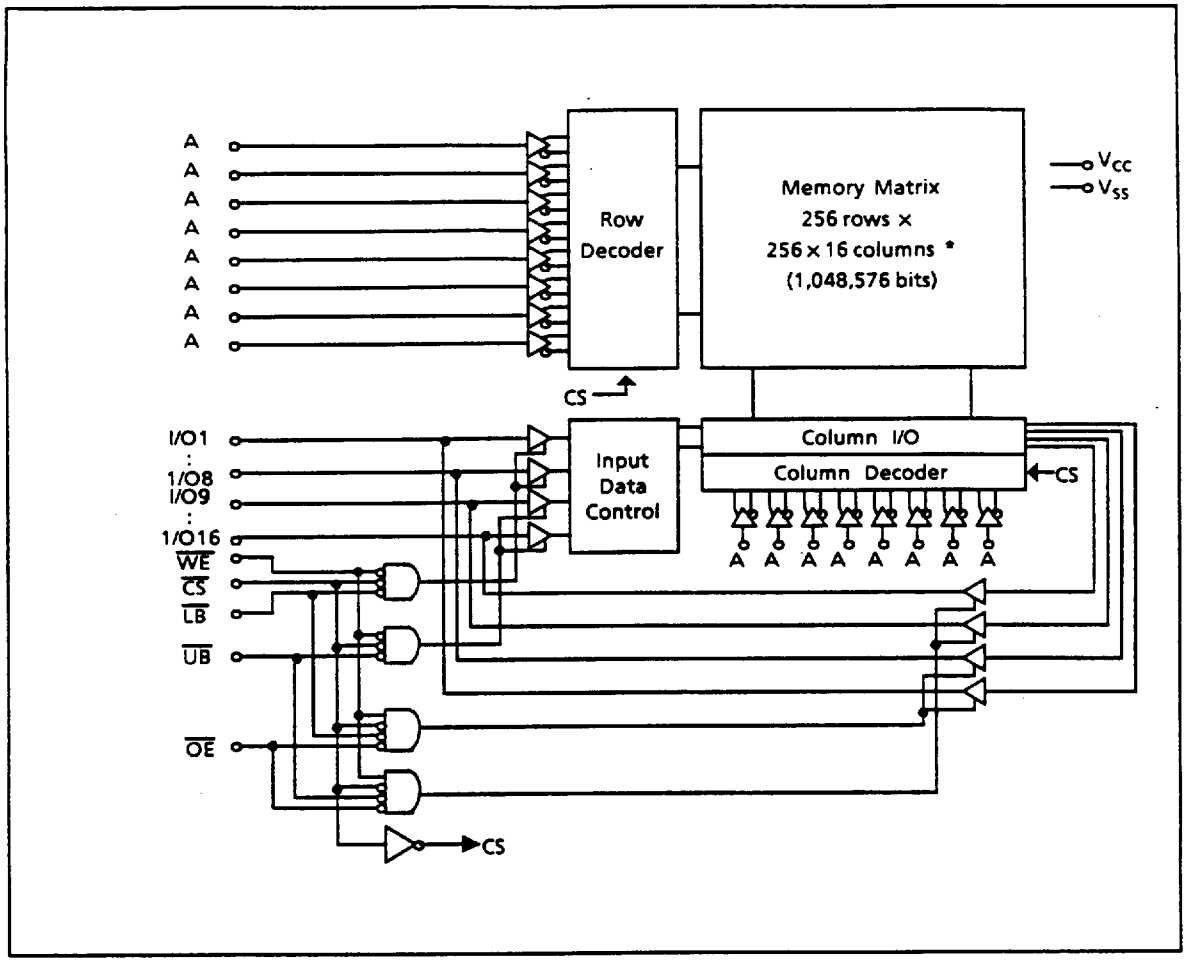
Pin name	Function
A0-A15	Address
I/O1-I/O8	Input/Output(lower byte)
I/O9-I/O16	Input/Output(upper byte)
$\overline{CS}$	Chip select
$\overline{LB}$	Lower byte select
$\overline{UB}$	Upper byte select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.
This document contains information on a new product.
Specifications and information contained herein are subject to change without notice.

Hitachi semiconductor

Block Diagram

HM67W1664 Series



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage relative to Vss	Vcc	-0.5 to 4.6	V
Voltage on any pin relative to Vss	V_T	-0.5*1 to V_{CC} + 0.5 (≤ 4.6max)	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	-55 to + 125	°C
Storage temperature under bias	Tbias	-10 to + 85	°C

Notes : 1. -2.0V for pulse width ≤ 10ns

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Under the DC and AC specifications shown in the tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

Function Table

HM67W1664 Series

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	V_{CC} Current	I/O1-I/O8	I/O9-I/O16	Ref.cycle
H	X	X	X	X	I_{SB}, I_{SB1}	High-Z	High-Z	-
L	H	H	X	X	I_{CC}	High-Z	High-Z	-
L	L	H	L	L	I_{CC}	Output	Output	Read cycle
L	L	H	L	H	I_{CC}	Output	High-Z	Read cycle
L	L	H	H	L	I_{CC}	High-Z	Output	Read cycle
L	L	H	H	H	I_{CC}	High-Z	High-Z	-
L	X	L	L	L	I_{CC}	Input	Input	Write cycle
L	X	L	L	H	I_{CC}	Input	High-Z	Write cycle
L	X	L	H	L	I_{CC}	High-Z	Input	Write cycle
L	X	L	H	H	I_{CC}	High-Z	High-Z	-

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage*2	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 0.5	V
	V_{IL}	-0.5*1	-	0.8	V

Note: 1. -2.0V for pulse width ≤ 10ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V)

Parameter	Symbol	min	typ	max	Unit		Test Conditions	Notes
Input leakage current	$\|I_{LI}\|$	-	-	2	μA		Vin = V_{SS} to V_{CC} V_{CC} = 3.6V	
Output leakage current	$\|I_{LO}\|$	-	-	10	μA		$V_{I/O}$ = V_{SS} to V_{CC} $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{LB}$ = $\overline{UB}$ = V_{IH} or $\overline{WE}$ = V_{IL}	
Operating power supply current	I_{CC}	-	-	250	mA	10ns cycle	$\overline{CS}$ = V_{IL} Iout = 0mA	
		-	-	220	mA	12ns cycle	Other inputs = V_{IH} / V_{IL}	
Standby power supply current	I_{SB}	-	-	80	mA	10ns cycle	$\overline{CS}$ = V_{IH}	
		-	-	60	mA	12ns cycle	Other inputs = V_{IH} / V_{IL}	
Standby power supply current(1)	I_{SB1}	-	-	15	mA		V_{CC} ≥ $\overline{CS}$ ≥ V_{CC}-0.2V, 0V ≤ Vin ≤ 0.2V or V_{CC} ≥ Vin ≥ V_{CC}-0.2V	
Output Voltage	V_{OL}	-	-	0.4	V		I_{OL} = 4mA	
	V_{OH}	2.4	-	-	V		I_{OH} = -2mA	

Capacitance (Ta = 25°C, f = 1.0MHz) *1

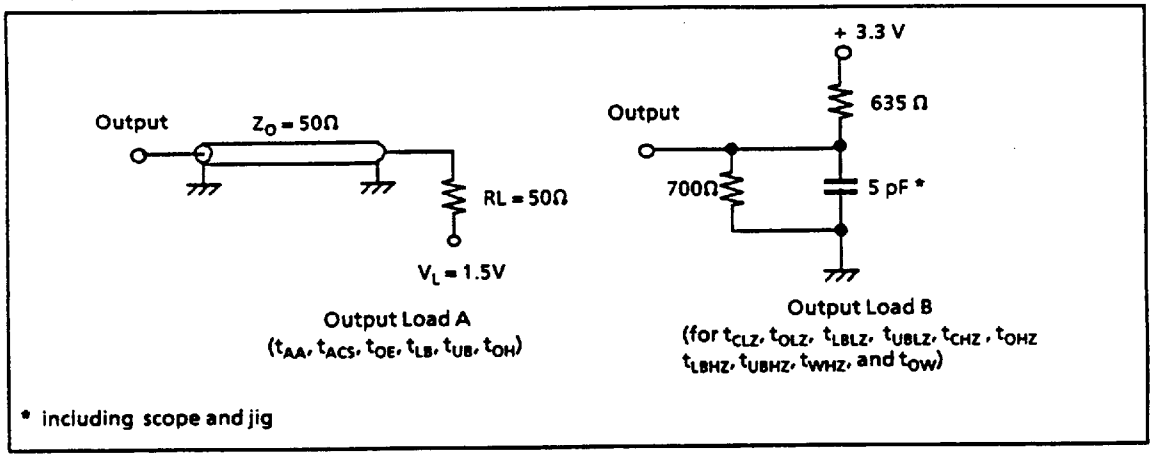
Parameter	Symbol	min	typ	max	Unit	Test Conditions
Input Capacitance	Cin	-	-	5	pF	Vin = 0V
Input/Output Capacitance	$C_{I/O}$	-	-	7	pF	$V_{I/O}$ = 0V

Notes: 1. This parameter is sampled and not 100% tested

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, unless otherwise noted.)

Test conditions

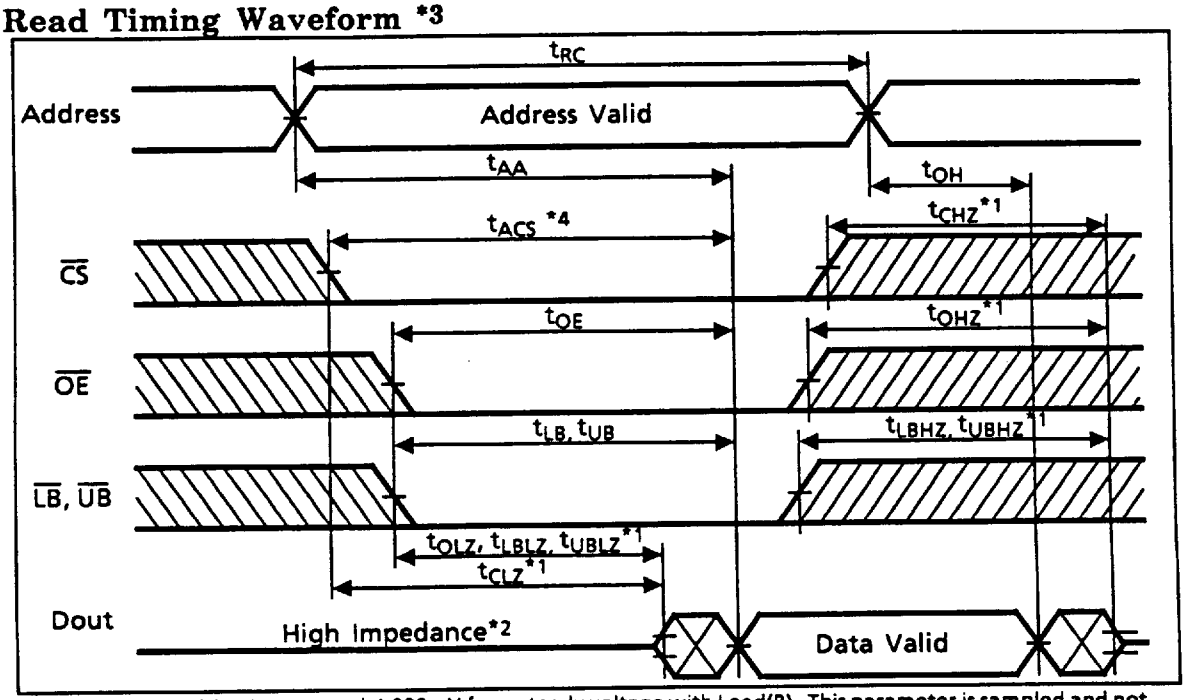
- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 3ns
- Input and output timing reference levels: 1.5V
- Output load: See figures



Read Cycle

Parameter	Symbol	HM67W1664-10 Min	HM67W1664-10 Max	HM67W1664-12 Min	HM67W1664-12 Max	Unit
Read cycle time	t_{RC}	10	-	12	-	ns
Address Access time	t_{AA}	-	10	-	12	ns
Chip select access time	t_{ACS}	-	10	-	12	ns
Output enable to output vaild	t_{OE}	-	5	-	6	ns
Byte select to output vaild	t_{LB},t_{UB}	-	5	-	6	ns
Output hold from address change	t_{OH}	3	-	3	-	ns
Chip select to output in low-Z	t_{CLZ}	3	-	3	-	ns
Output enable to output in low-Z	t_{OLZ}	0	-	0	-	ns
Byte select to output in low-Z	t_{LBLZ},t_{UBLZ}	0	-	0	-	ns
Chip deselect to output in high-Z	t_{CHZ}	-	5	-	5	ns
Output disable to output in high-Z	t_{OHZ}	-	5	-	5	ns
Byte deselect to output in high-Z	t_{LBHZ},t_{UBHZ}	-	5	-	5	ns

Read Timing Waveform *3



Notes : 1. Transition is measured ±200mV from steady voltage with Load(B). This parameter is sampled and not 100% tested.

2. When $\overline{CS}$, $\overline{OE}$, and $\overline{LB}$ are low, Dout(lower byte) is low impedance.
When $\overline{CS}$, $\overline{OE}$, and $\overline{UB}$ are low, Dout(upper byte) is low impedance.

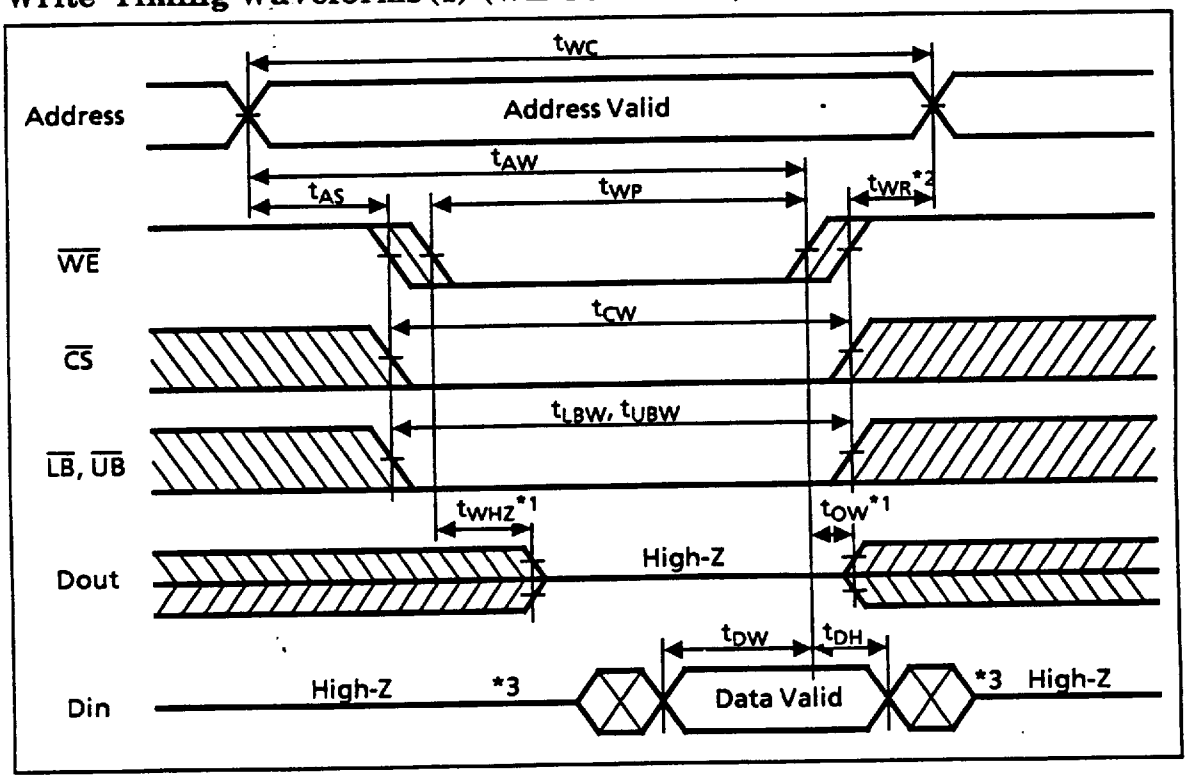
3. $\overline{WE}$ is high for read cycle.

4. Address valid prior to or coincident with $\overline{CS}$ transition low.

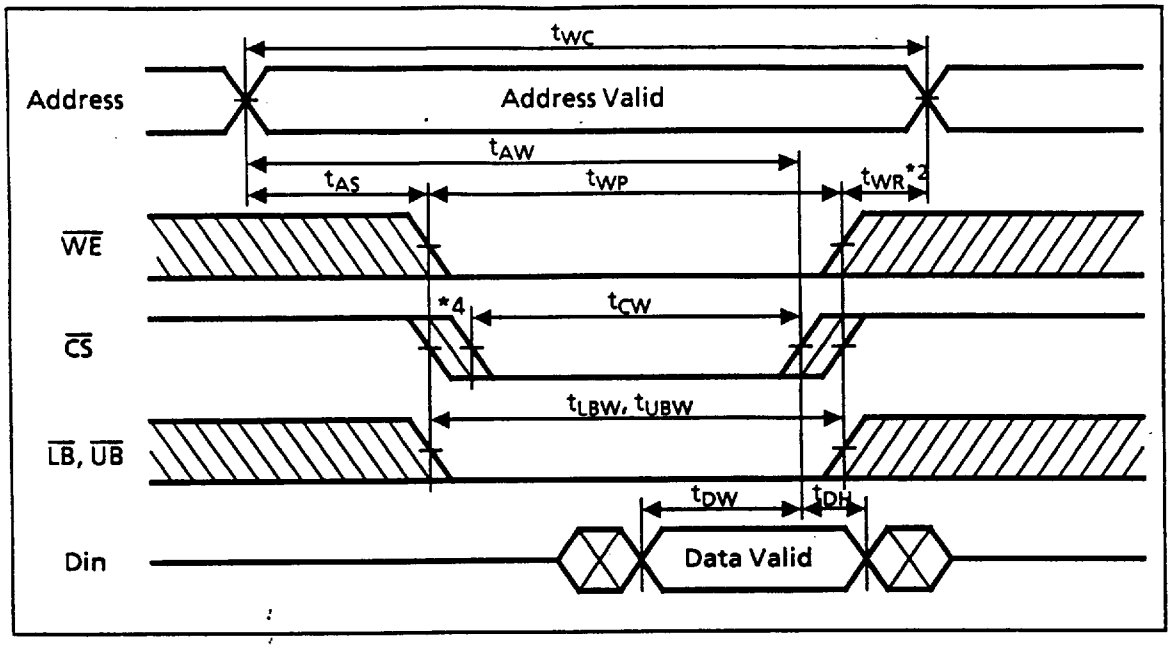
Write Cycle

Parameter	Symbol	HM67W1664-10 Min	HM67W1664-10 Max	HM67W1664-12 Min	HM67W1664-12 Max	Unit
Write cycle time	t_{WC}	10	-	12	-	ns
Address valid to end of write	t_{AW}	9	-	10	-	ns
Chip select to end of write	t_{CW}	8	-	9	-	ns
Write pulse width	t_{WP}	8	-	9	-	ns
Byte select to end of write	t_{LBW}, t_{UBW}	8	-	9	-	ns
Address setup time	t_{AS}	0	-	0	-	ns
Write recovery time	t_{WR}	0	-	0	-	ns
Data valid to end of write	t_{DW}	5	-	6	-	ns
Data hold time from end of write	t_{DH}	0	-	0	-	ns
Write diasble to output in low-Z	t_{OW}	3	-	3	-	ns
Write enable to output in high-Z	t_{WHZ}	-	5	-	5	ns

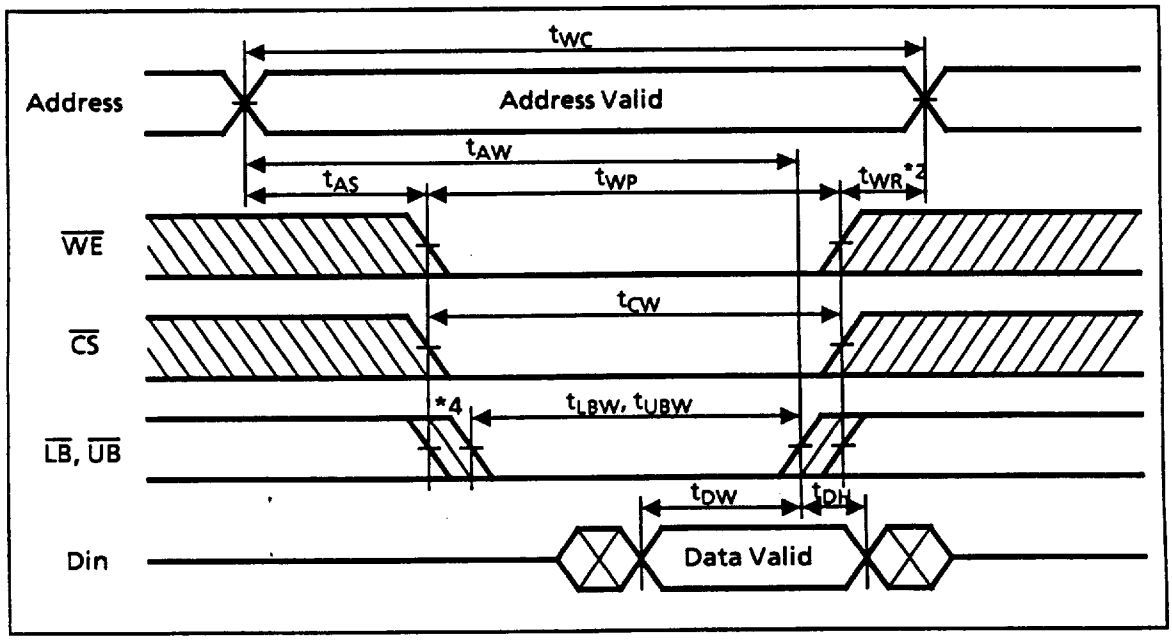
Write Timing Waveforms (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Write Timing Waveform (3) ($\overline{LB}$, $\overline{UB}$ Controlled)



Notes:
1. Transition is measured ± 200mV from high impedance voltage with Load(B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ must be high during address transition except when the device is disabled with $\overline{CS}$, $\overline{LB}$ or $\overline{UB}$.
3. If $\overline{CS}$, $\overline{OE}$, $\overline{LB}$, and $\overline{UB}$ are low durinig this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
4. If the $\overline{CS}$, or $\overline{LB}$ or $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transistions or after the $\overline{WE}$ transition, output remains a high impedance state.
5. All Write occurs during the overlap of a low $\overline{CS}$, low $\overline{UB}$ or low $\overline{LB}$, and a low $\overline{WE}$ (t_{WP}).
6. All Write cycle timings are referenced from the last vaild address to the first transitioning address.

Package Dimensions

HM67W1664JP Series (CP-44D)

Unit : mm