T-46-23-17

HYUNDAI SEMICONDUCTOR HYM59256A

256K×9-Bit CMOS DRAM MODULE

M451201A-APR91

DESCRIPTION

The HYM59256A is a 256K words by 9bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of two HY534256J in 20/26 pin SOJ and one HY53C256LF in 18 pin PLCC mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM59256AM is a socket type and HYM59256AP is a leaded type single-in line module, these are suitable for easy interchange and addition of 256K bytes memory with parity RAM.

FEATURES

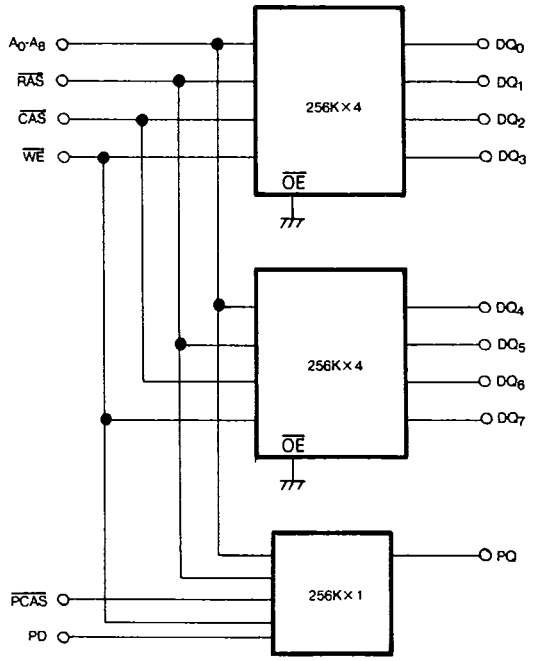
- **Fast Page Mode operation**
- **Fast Access Time**

	t_{RAC}	t_{CAC}	t_{PC}
HYM59256A-70	70	20	50
HYM59256A-80	80	25	55
HYM59256A-10	100	25	60

- **Single power supply of 5V± 10%**
- **$\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.**
- **Low power operating**
  1.26W max (HYM59256A-70)
  1.10W max (HYM59256A-80)
  0.93W max (HYM59256A-10)
- **TTL compatible inputs and outputs**
- **512 refresh cycles / 8ms**

5

BLOCK DIAGRAM

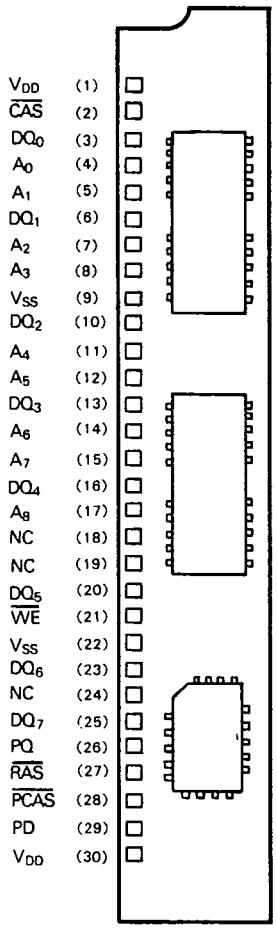


PIN NAMES

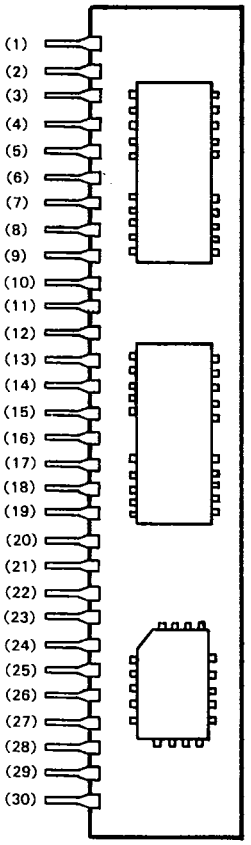
A_0-A_8	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
PD	DATA IN FOR PARITY
PQ	DATA OUT FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	$\overline{CAS}$ FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS

HYM59256AM



HYM59256AP



NOTES :
1. HYM59256AP's pin configuration is the same as HYM59256AM's.
2. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
3. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
4. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature(Plastic)	−55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

5

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM59256A		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			30	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−70		230	mA	1, 2
			−80		200		
			−10		170		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}			6	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70		230	mA	2
			−80		200		
			−10		170		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70		165	mA	1, 2
			−80		140		
			−10		115		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}=V_{IH}$, other inputs ≥ V_{SS}			3	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−70		230	mA	2
			−80		200		
			−10		170		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :

1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM59256A						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	130		150		180		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		70		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	15		15		15		ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40		50		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	50	20	60	25	75	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		20		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	55	25	60	25	75	ns	2
11	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100	ns	3,4,5
12	t_{AA}	Access Time from Column Address		35		40		50	ns	5,7
13	t_{CAC}	Access Time from $\overline{CAS}$		20		25		25	ns	5,6
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20		25		30		ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	25		25		30		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		ns	8
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		ns	8
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15		15		15		ns	
20	t_{HZ}	$\overline{CAS}$ to Output High Impedance	0	20	0	25	0	30	ns	11
21	t_{WP}	Write Command Pulse Width	15		15		20		ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	15		15		20		ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		75		ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		75		ns	
25	t_{WCS}	Write Commnad Set-up Time	0		0		0		ns	9
26	t_{WCH}	Write Command Hold Time	15		15		20		ns	
27	t_{DS}	Data In Set-up Time	0		0		0		ns	10
28	t_{DH}	Data In Hold Time	15		15		20		ns	10

#	SYMBOL	PARAMETER	HYM59256A						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	55		60		75		ns	
30	t_{CPA}	Access Time from Column Precharge		35		40		50	ns	12
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	50		55		60		ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		30		ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		30		ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	20		25		30		ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	13
38	t_{REF}	Refresh Interval(512 Cycle)		8		8		8	ms	16
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	70	100K	80	100K	100	100K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40		40		50		ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0		0		0		ns	3

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.), If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds $t_{RAD(max.)}$.
4. Assume $t_{RCD} \leq t_{RCD}$(max.), If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.).
5. Measured with a load equivalent to two TTL loads and 100pF.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max.) and $t_{RAD} \leq t_{RAD}$(max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \leq t_{RAD}$(max.).
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as a electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$.
11. t_{HZ} defines the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.) and AC Measurements assume t_T=5ns.
14. An initial pause of 200μs is required after power-up and followed at least 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only Refresh). 8 initialization cycles are required after extended periods of bias without clocks.

5

CAPACITANCE

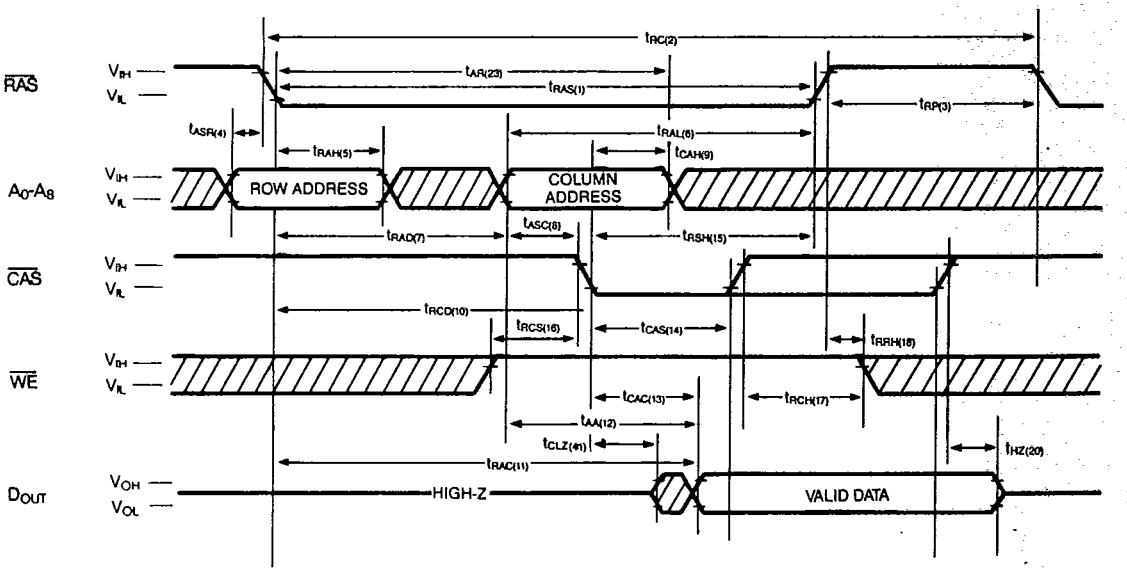
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_8, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	25	pF
C_{IN2}	Input Capacitance(PD, $\overline{PCAS}$)	–	10	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF
C_{PQ}	Output Capacitance(PQ)	–	10	pF

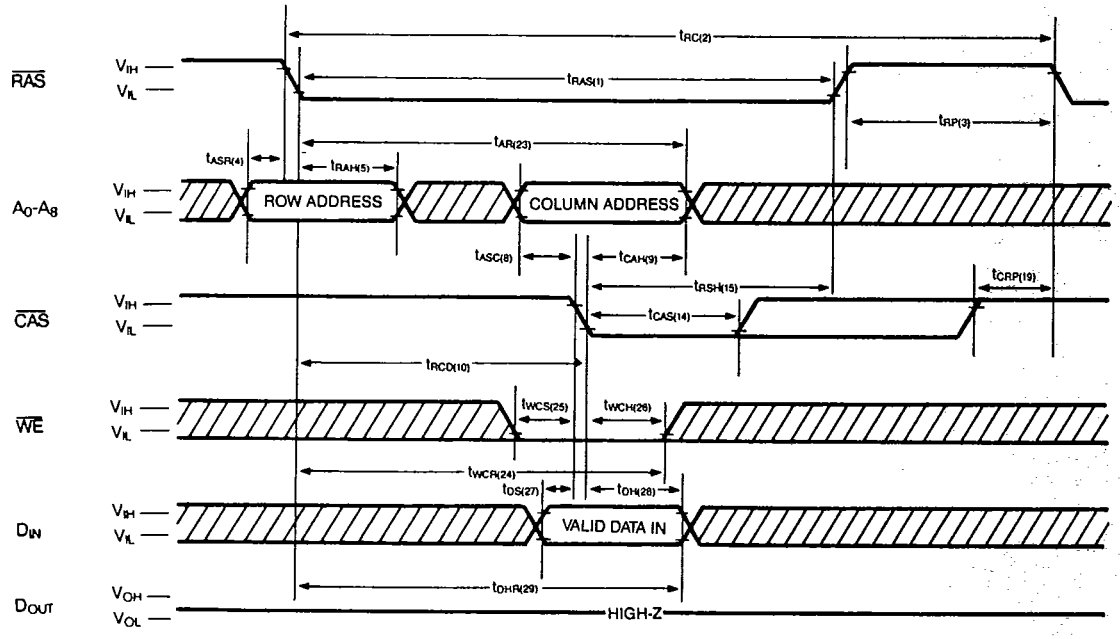
TIMING DIAGRAM

($\overline{CAS}$ includes $\overline{PCAS}$ and $\overline{CAS}$, D_{IN} includes DQ_0-DQ_7 and PD, D_{OUT} includes DQ_0-DQ_7 and PQ.)

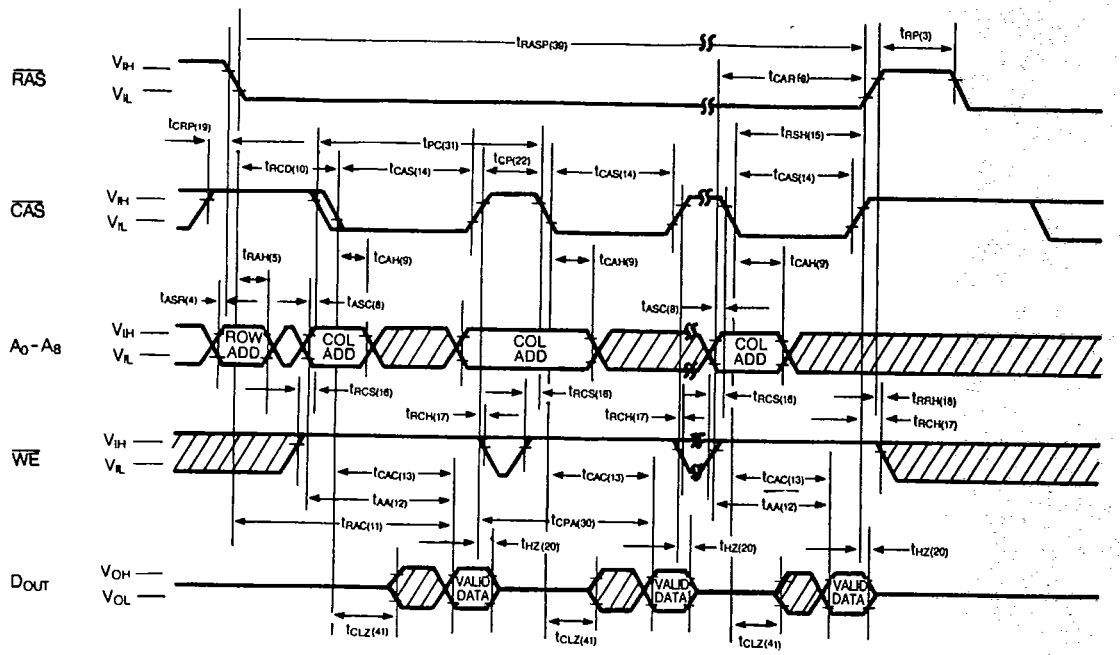
READ CYCLE



EARLY WRITE CYCLE

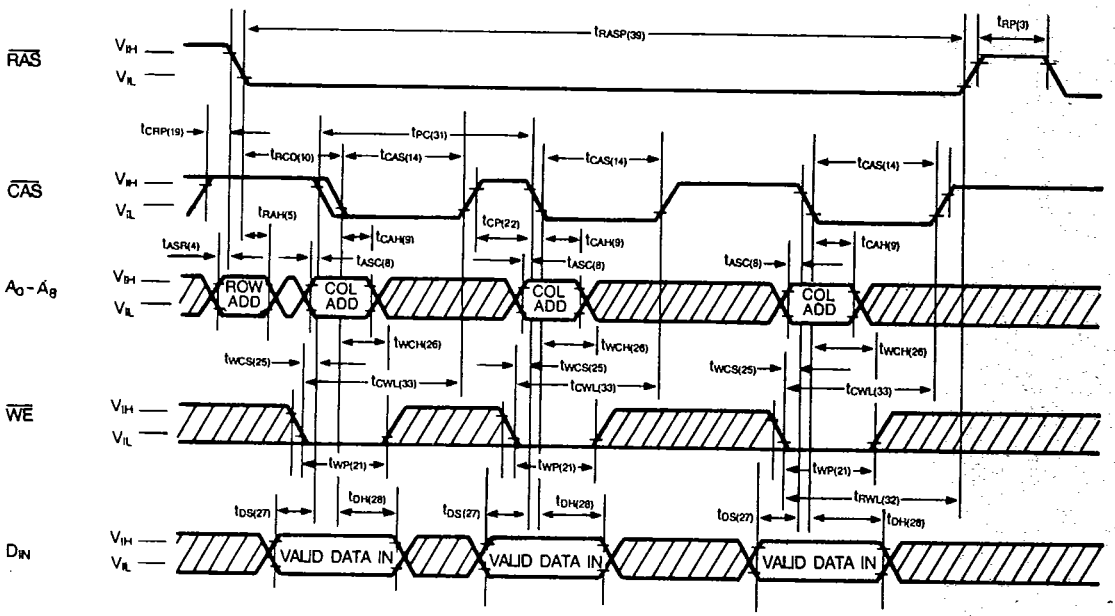


FAST PAGE MODE READ CYCLE

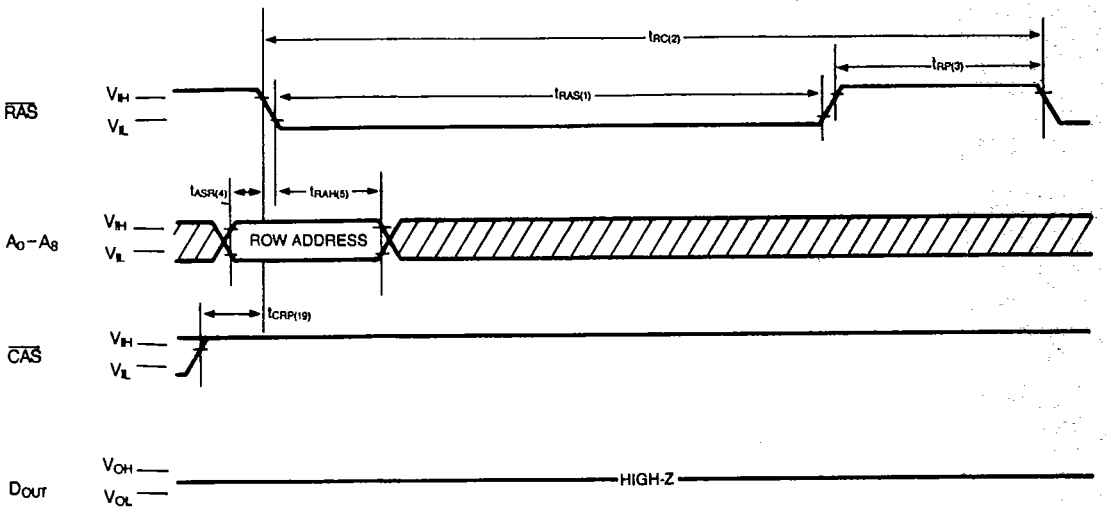


5

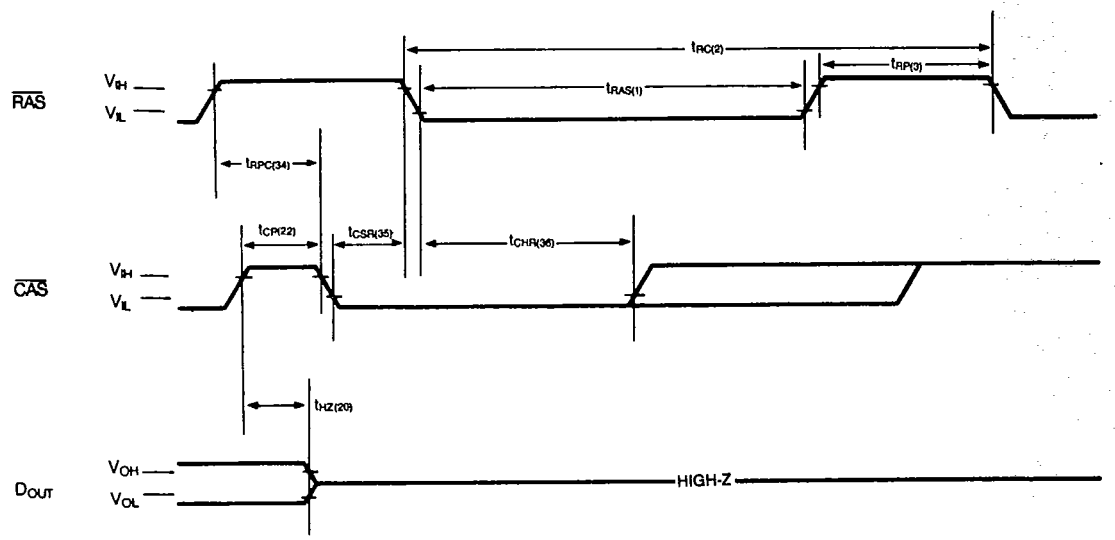
FAST PAGE MODE EARLY WRITE CYCLE



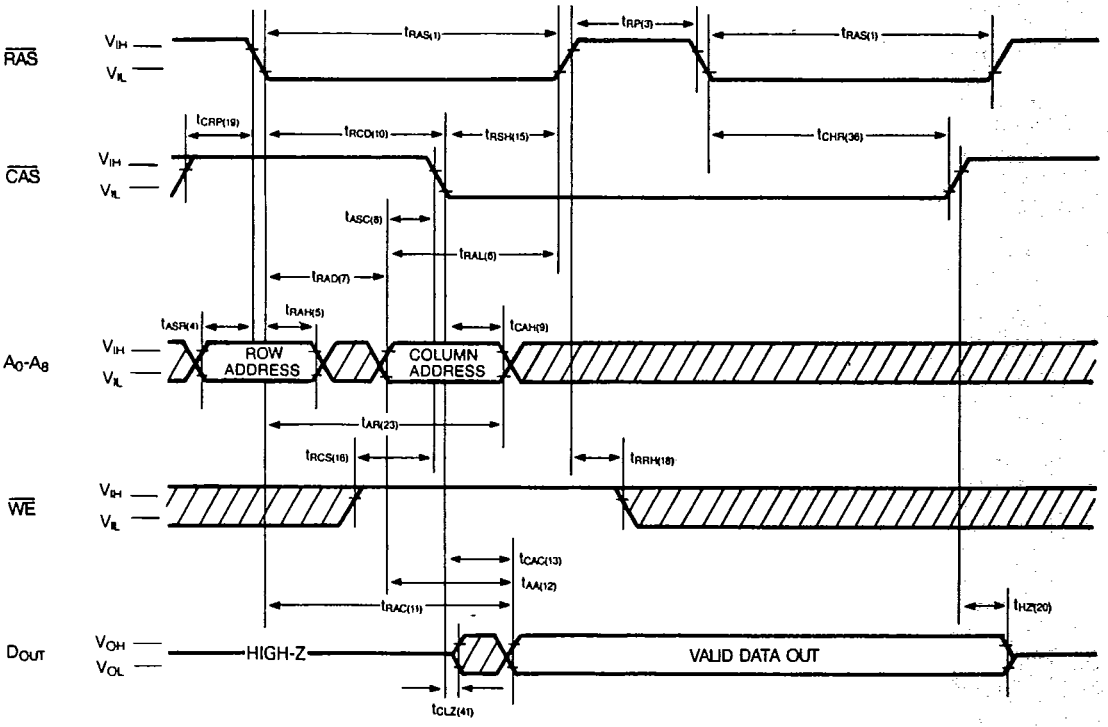
$\overline{RAS}$-ONLY REFRESH CYCLE



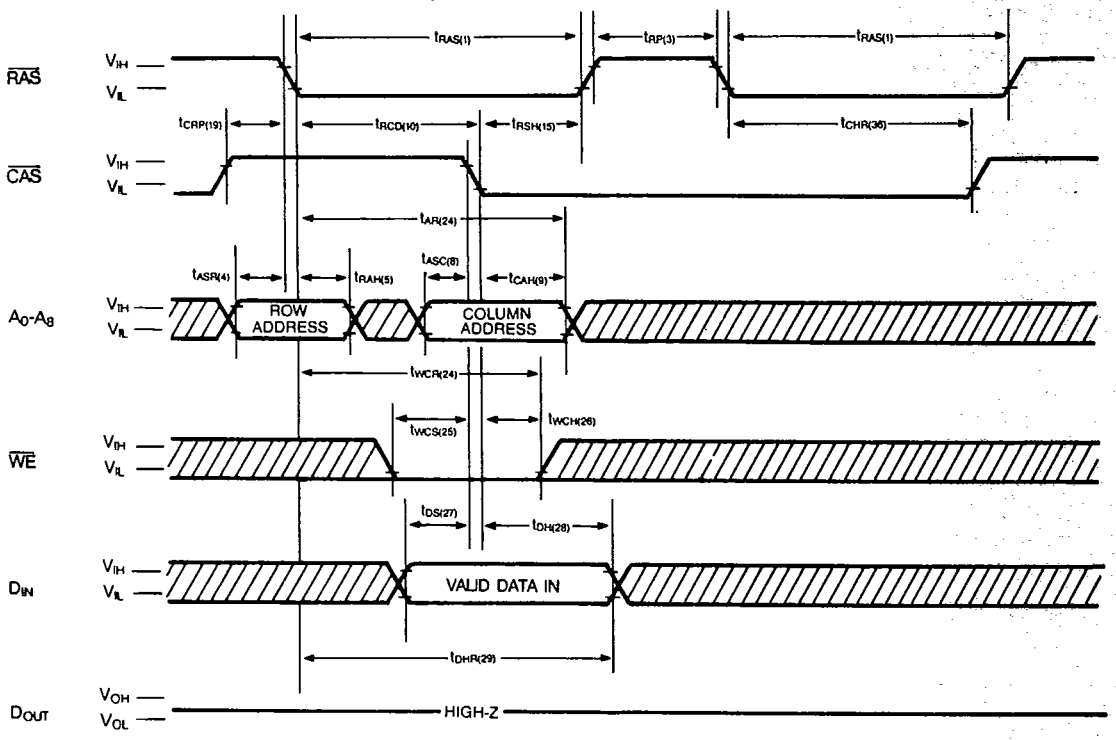
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE(READ)



HIDDEN REFRESH CYCLE (WRITE)



5

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE