Integrated Device Technology, Inc.

32K x 32, 3.3V SYNCHRONOUS SRAM WITH 3.3V/2.5V PIPELINED OUTPUTS AND INTERLEAVED/LINEAR BURST COUNTER

PRELIMINARY
IDT71V532

FEATURES:

- 32K x 32 memory configuration
- Supports high performance system speed - up to 133 MHz (4.5ns Clock-to-Data Access) in Pipelined Mode
- $\overline{LBO}$ input selects interleaved or linear burst mode
- Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BWx}$)
- Power down controlled by ZZ input
- The core operates with a 3.3V supply (V_{DD})
- I/O's can either operate at 3.3V (+10/-5%) or 2.5V (+0.4V/-0.2V) (V_{DDQ})
- Packaged in a JEDEC Standard 100-pin rectangular plastic thin quad flatpack (TQFP)

DESCRIPTION:

The IDT71V532 is a 3.3V high-speed 1,048,576-bit SRAM organized as 32K x 32 with full support of the Pentium™ and PowerPC™ processor interfaces. The pipelined burst architecture provides cost-effective 3-1-1-1 secondary cache performance for processors up to 133MHz.

The IDT71V532 SRAM contains write, data, address, and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V532 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses will be defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71V532 SRAM utilizes IDT's high-performance, high-volume 3.3V CMOS process, and is packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) for optimum board density in both desktop and notebook applications.

PIN DESCRIPTION SUMMARY

$A_0 - A_{14}$	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS_1}$	Chip Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear/Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}	Data Input/Output	I/O	Synchronous
V_{DD}, V_{DDQ}	3.3V Array, 3.3V or 2.5V I/O	Power	N/A
V_{SS}, V_{SSQ}	Array Ground, I/O Ground	Power	N/A

3616 tbl 01

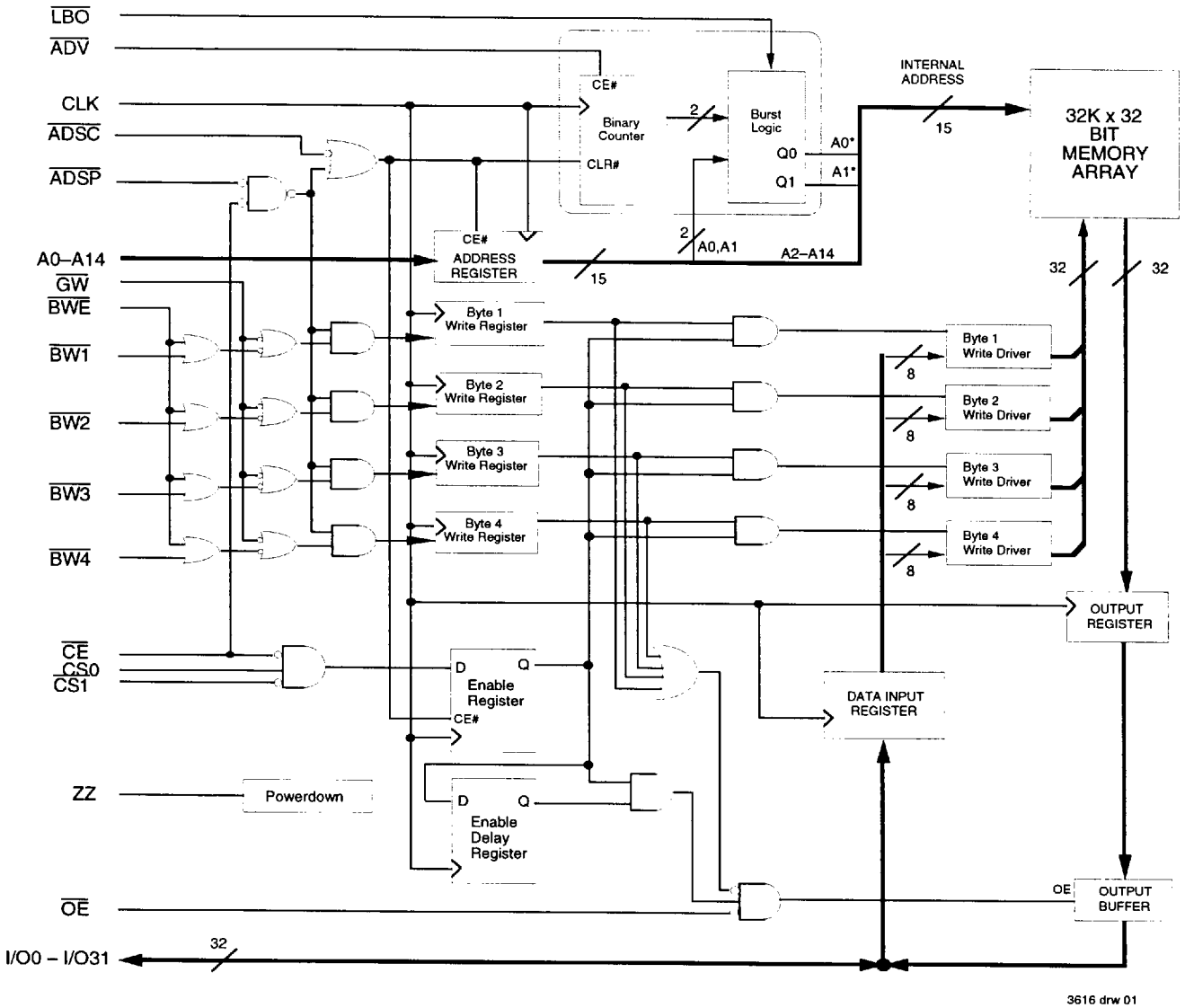
PIN DEFINITIONS(1)

Symbol	Pin Function	I/O	Active	Description
A_0-A_{14}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{ADSC}$ Low or $\overline{ADSP}$ Low and $\overline{CE}$ Low.
$\overline{ADSC}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{ADSC}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSC}$ is NOT GATED by $\overline{CE}$.
$\overline{ADSP}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{ADSP}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSP}$ is gated by $\overline{CE}$.
$\overline{ADV}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{ADV}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When this input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{BWE}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{BW_1}$-$\overline{BW_4}$. If $\overline{BWE}$ is LOW at the rising edge of CLK then $\overline{BW}$x inputs are passed to the next stage in the circuit. A byte write can still be blocked if $\overline{ADSP}$ is LOW at the rising edge of CLK. If $\overline{ADSP}$ is HIGH and $\overline{BW}$x is LOW at the rising edge of CLK then data will be written to the SRAM. If $\overline{BWE}$ is HIGH then the byte write inputs are blocked and only $\overline{GW}$ can initiate a write cycle.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 8-bit byte has its own active LOW byte write. Any active byte write causes all outputs to be disabled. $\overline{ADSP}$ LOW disables all byte writes. $\overline{BW_1}$-$\overline{BW_4}$ must meet specified setup and hold times with respect to CLK.
$\overline{CE}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{CE}$ is used with CS_0 and $\overline{CS_1}$ to enable the IDT71V532. $\overline{CE}$ also gates $\overline{ADSP}$.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS_0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS_0 is used with $\overline{CE}$ and $\overline{CS_1}$ to enable the chip.
$\overline{CS_1}$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{CS_1}$ is used with $\overline{CE}$ and CS_0 to enable the chip.
$\overline{GW}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 8-bit data bytes when LOW on the rising edge of CLK. $\overline{GW}$ superceeds individual byte write enables.
I/O_0-I/O_{31}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{LBO}$	Linear Burst Order	I	LOW	Asynchronous burst order selection DC input. When $\overline{LBO}$ is HIGH the Interleaved (Intel) burst sequence is selected. When $\overline{LBO}$ is LOW the Linear (PowerPC) burst sequence is selected. $\overline{LBO}$ is a static DC input and must not change state while the device is operating.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{OE}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedence state.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply inputs.
V_{DDQ}	Power Supply	N/A	N/A	User selectable 3.3V or 2.5V I/O power supply inputs.
VSS	Ground	N/A	N/A	Core ground pins.
VSSQ	Ground	N/A	N/A	I/O ground pins.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the chip.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V532 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

3616 tbl 02

FUNCTIONAL BLOCK DIAGRAM



3616 drw 01

RECOMMENDED DC OPERATING CONDITIONS WITH VDDQ AT 3.3V.

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	3.135	3.3	3.63	V
VDDQ	I/O Supply Voltage	3.135	3.3	3.63	V
VSS, VSSQ	Ground	0	0	0	V
VIH	Input High Voltage	2.0(1)	—	5.5(2)	V
VIL	Input Low Voltage	–0.5(3)	—	0.8	V

3616 tbl 03

NOTE:
1. VIH and VIL as indicated is for both input only and I/O pins.
2. VIH (max) = 6.0V for pulse width less than tCYC/2, once per cycle.
3. VIL (min) = -1.0V for pulse width less than tCYC/2, once per cycle.

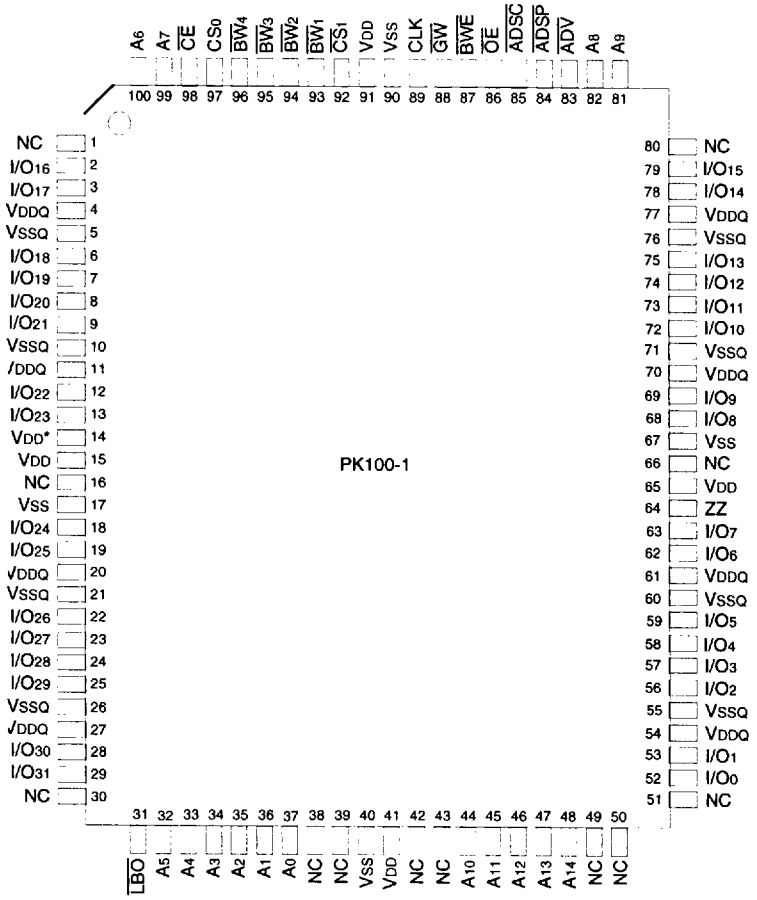
RECOMMENDED DC OPERATING CONDITIONS WITH VDDQ AT 2.5V.

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	3.135	3.3	3.465	V
VDDQ	I/O Supply Voltage	2.375	2.5	2.9	V
VSS, VSSQ	Ground	0	0	0	V
VIH	Input High Voltage	1.7(1)	—	5.5(2)	V
VIL	Input Low Voltage	–0.3(3)	—	0.7	V

3616 tbl 04

NOTE:
1. VIH and VIL as indicated is for both input only and I/O pins.
2. VIH (max) = 6.0V for pulse width less than tCYC/2, once per cycle.
3. VIL (min) = -1.0V for pulse width less than tCYC/2, once per cycle.

PIN CONFIGURATION



* Pin 14 does not have to be directly connected to VDD as long as the input voltage is ≥ VIH

3616 drw 02

TOP VIEW
TQFP

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
VTERM(3)	Terminal Voltage with Respect to GND	–0.5 to VDD+0.5	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTES: 3616 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDD, VDDQ and Input terminals only.
3. I/O terminals.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, TQFP package)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	6	pF
CI/O	I/O Capacitance	VOUT = 3dV	7	pF

NOTE: 3616 tbl 06

1. This parameter is guaranteed by device characterization, but not production tested.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	ZZ and $\overline{LBO}$ Input Leakage Current[1]	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$, V_{OUT} = 0V to V_{DD}, V_{DD} = Max.	—	5	µA
V_{OL}(3.3V)	Output Low Voltage	I_{OL} = 5mA, V_{DD} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage	I_{OH} = –5mA, V_{DD} = Min.	2.4	—	V
V_{OL}(2.5V)	Output Low Voltage	I_{OL} = 2mA, V_{DD} = Min.	—	0.7	V
V_{OH} (2.5V)	Output High Voltage	I_{OH} = –2mA, V_{DD} = Min.	1.7	—	V

NOTE:

3616 tbl 07

1. The ZZ pin will be internally pulled to Vss if it is not actively driven in the application.

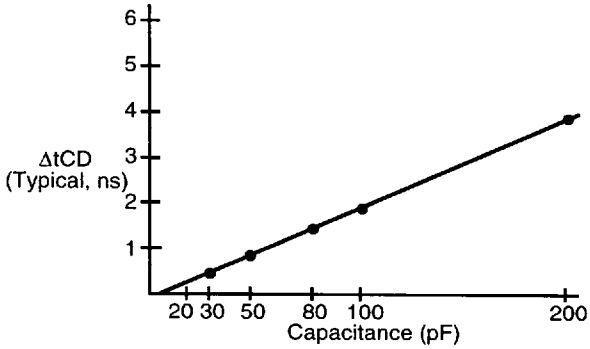
DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{HD} = V_{DDQ}–0.2V, V_{LD} = 0.2V)

Symbol	Parameter	Test Condition	133MHz	125MHz	100MHz	75MHz	66MHz	Unit
I_{DD}	Operating Core Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	290	280	270	260	210	mA
I_{DDQ}	Operating I/O Power Supply Current	Device Selected, Outputs Open, V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	20	20	20	15	15	mA
I_{SB}	Standby Core Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	70	65	60	55	47	mA
I_{SBQ}	Standby I/O Power Supply Current	Device Deselected, Outputs Open, V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	3	3	3	3	3	mA
I_{SB1}	Full Standby Core Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2]	13	13	13	13	13	mA
I_{SB1Q}	Full Standby I/O Power Supply Current	Device Deselected, Outputs Open, V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2]	2	2	2	2	2	mA
I_{ZZ}	Full Sleep Mode Core Power Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	9	9	9	9	9	mA
I_{ZZQ}	Full Sleep Mode I/O Power Supply Current	ZZ $\geq V_{HD}$, V_{DDQ} = Max.	1	1	1	1	1	mA

NOTES:

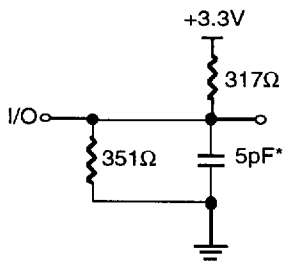
3616 tbl 08

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.



3616 drw 03

Figure 1. Lumped Capacitive Load, Typical Derating



3616 drw 04

Figure 2. High Impedence Test Load (for t_{OHZ}, t_{CHZ}, t_{OLZ}, and t_{DC1})

*** Including scope and jig**

SYNCHRONOUS TRUTH TABLE(1, 2)

Operation	Address Used	$\overline{CE}$	CS_0	$\overline{CS_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BWx}$	$\overline{OE}$ (3)	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	↑	DOUT
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	↑	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	↑	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	↑	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	↑	DIN
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	↑	DIN
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	↑	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	↑	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	↑	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	↑	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	↑	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	↑	DIN
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	↑	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	↑	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	↑	DIN
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	↑	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	↑	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	↑	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	↑	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	↑	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	↑	DIN
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	↑	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	↑	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	↑	DIN

NOTES:
1. L = VIL, H = VIH, X = Don't Care.
2. ZZ = LOW for this table.
3. $\overline{OE}$ is an asynchronous input.

3616 tbl 09

SYNCHRONOUS WRITE FUNCTION TRUTH TABLE(1)

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1 (2)	H	L	L	H	H	H
Write Byte 2 (2)	H	L	H	L	H	H
Write Byte 3 (2)	H	L	H	H	L	H
Write Byte 4 (2)	H	L	H	H	H	L

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.

3616 tbl 10

ASYNCHRONOUS TRUTH TABLE(1)

Operation(2)	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out (I/O_0 – I/O_{31})	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z — Data In (I/O_0 – I/O_{31})	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

3616 tbl 11

INTERLEAVED BURST SEQUENCE TABLE ($\overline{LBO}$=V_{DD})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

3616 tbl 12

LINEAR BURST SEQUENCE TABLE ($\overline{LBO}$=V_{SS})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

3616 tbl 13

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V +10/-5% & V_{DDQ} = 3.3V +10/-5% OR V_{DD} = 3.3V +5/-5% & V_{DDQ} = 2.5V +0.4V/-0.2V, T_A = 0 to 70°C)

Symbol	Parameter	133 MHz		120 MHz		100 MHz		75 MHz		66 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Parameter												
t_{CYC}	Clock Cycle Time	7.5	—	8.3	—	10	—	13	—	15	—	ns
t_{CH}(1)	Clock High Pulse Width	2.1	—	2.5	—	3.7	—	4.5	—	5	—	ns
t_{CL}(1)	Clock Low Pulse Width	2.1	—	2.5	—	3.7	—	4.5	—	5	—	ns
Output Parameters												
t_{CD}	Clock High to Valid Data	—	4.5	—	5	—	5.5	—	6	—	7	ns
t_{CDC}	Clock High to Data Change	2	—	2	—	2	—	2	—	2	—	ns
t_{CLZ}(2)	Clock High to Output Active	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}(2)	Clock High to Data High-Z	2	4	2	4.5	2	5	2	5	2	6	ns
t_{OE}	Output Enable Access Time	—	4	—	4.5	—	5	—	5	—	5	ns
t_{OLZ}(2)	Output Enable Low to Data Active	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}(2)	Output Enable High to Data High-Z	—	3	—	4	—	5	—	5	—	5	ns
Set Up Times												
t_{SA}	Address Setup Time	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_{SS}	Address Status Setup Time	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_{SD}	Data In Setup Time	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_{SW}	Write Setup Time	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_{SAV}	Address Advance Setup Time	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_{SC}	Chip Enable/Select Setup Time	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Times												
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
Sleep Mode and Config. Parameters												
t_{ZZPW}	ZZ Pulse Width	100	—	100	—	100	—	100	—	100	—	ns
t_{ZZR}(3)	ZZ Recovery Time	100	—	100	—	100	—	100	—	100	—	ns
t_{CFG}(4)	Configuration Set-up Time	30	—	32	—	40	—	48	—	60	—	ns

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NOTES:
1. Measured as HIGH above 2.0V and LOW below 0.8V.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.

AC TEST LOAD

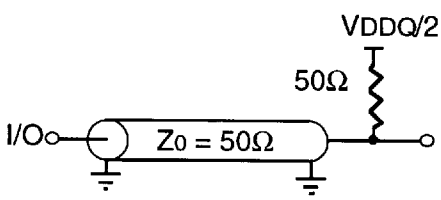

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Figure 3. AC Test Load

AC TEST CONDITIONS (V_{DDQ} = 3.3V / 2.5V)

Input Pulse Levels	0 to 3V / 0 to 2.5V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V / 1.25V
Output Timing Reference Levels	1.5V / 1.25V
AC Test Load	See Figures 2 and 3

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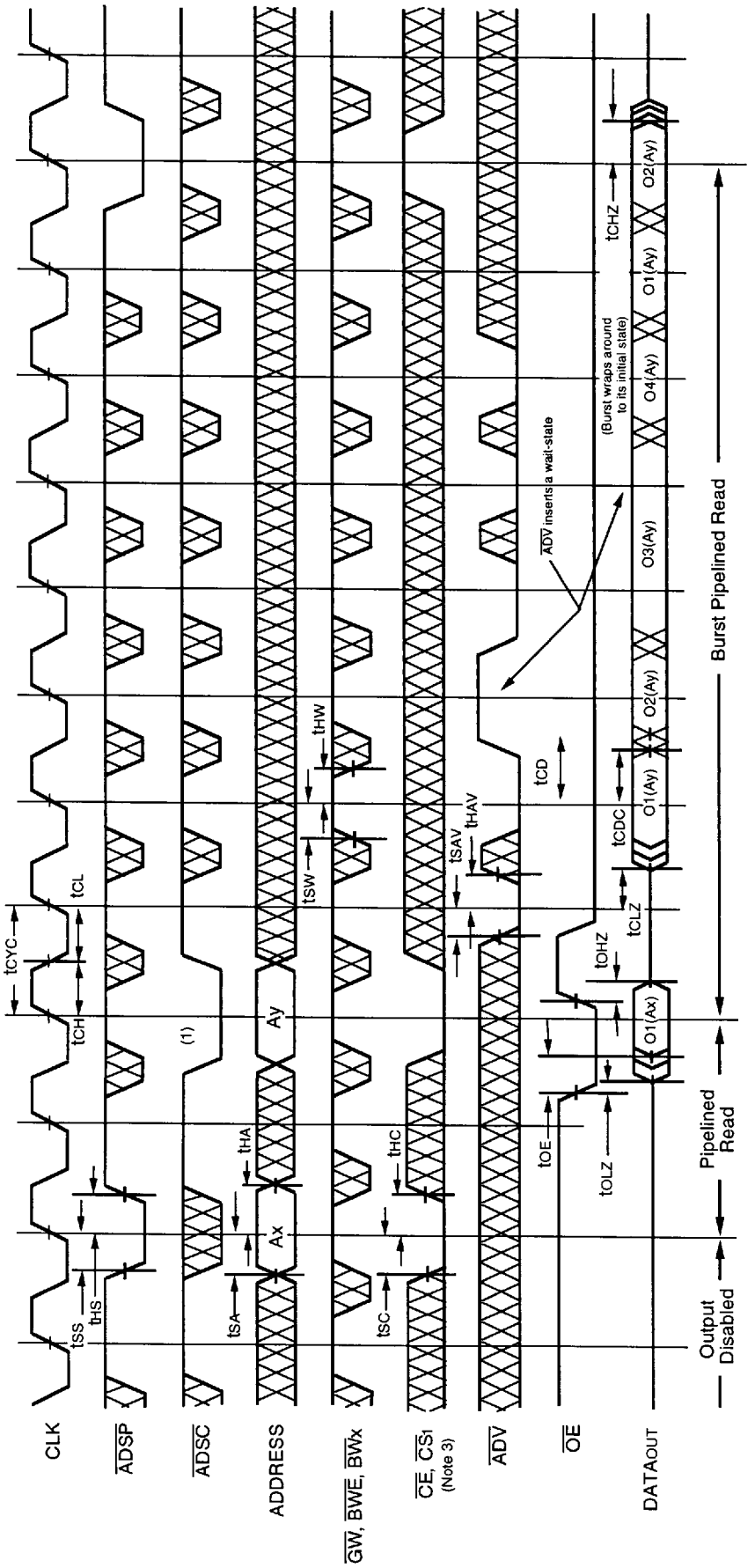
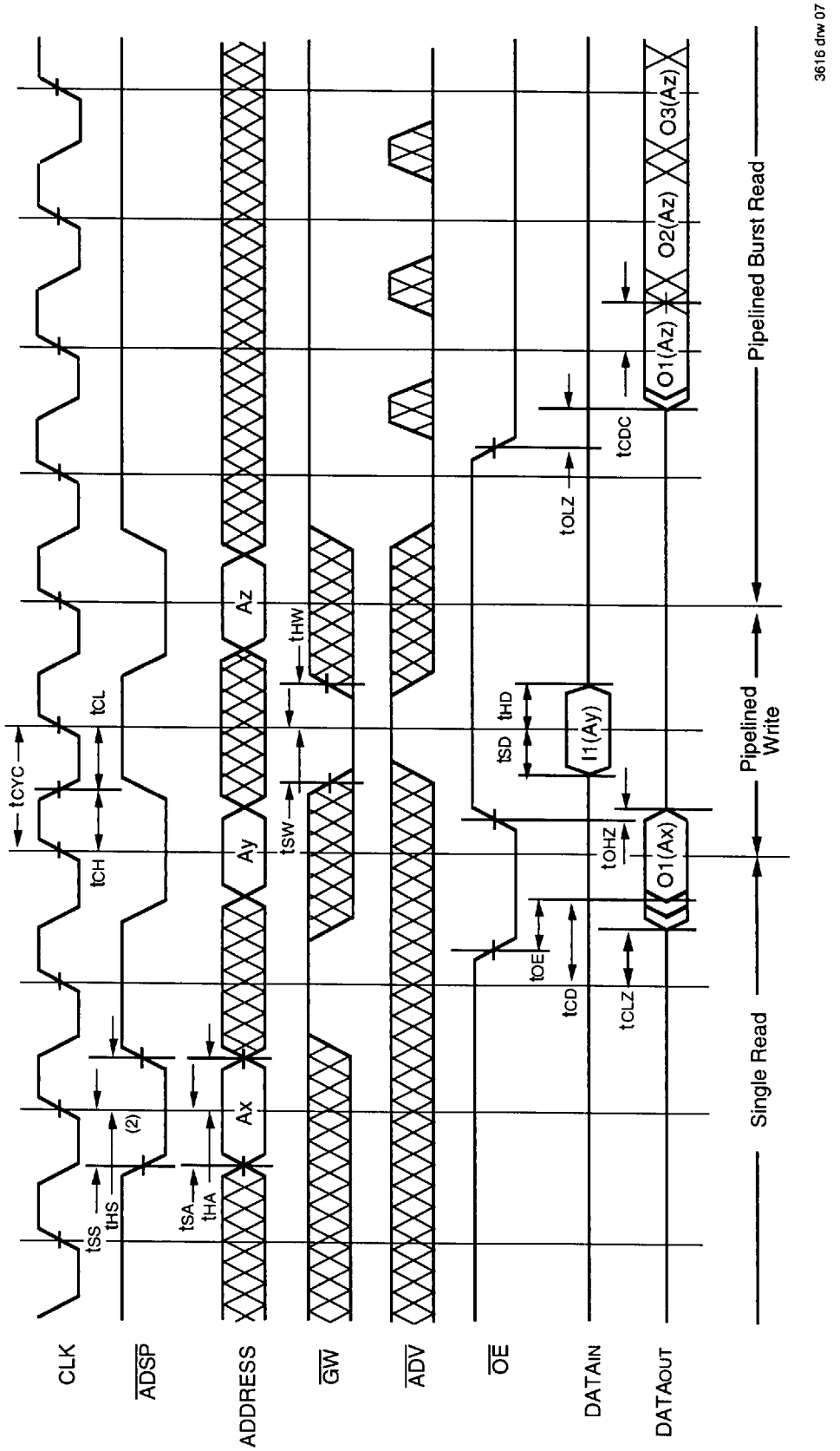
TIMING WAVEFORM OF PIPELINED READ CYCLE(1, 2)



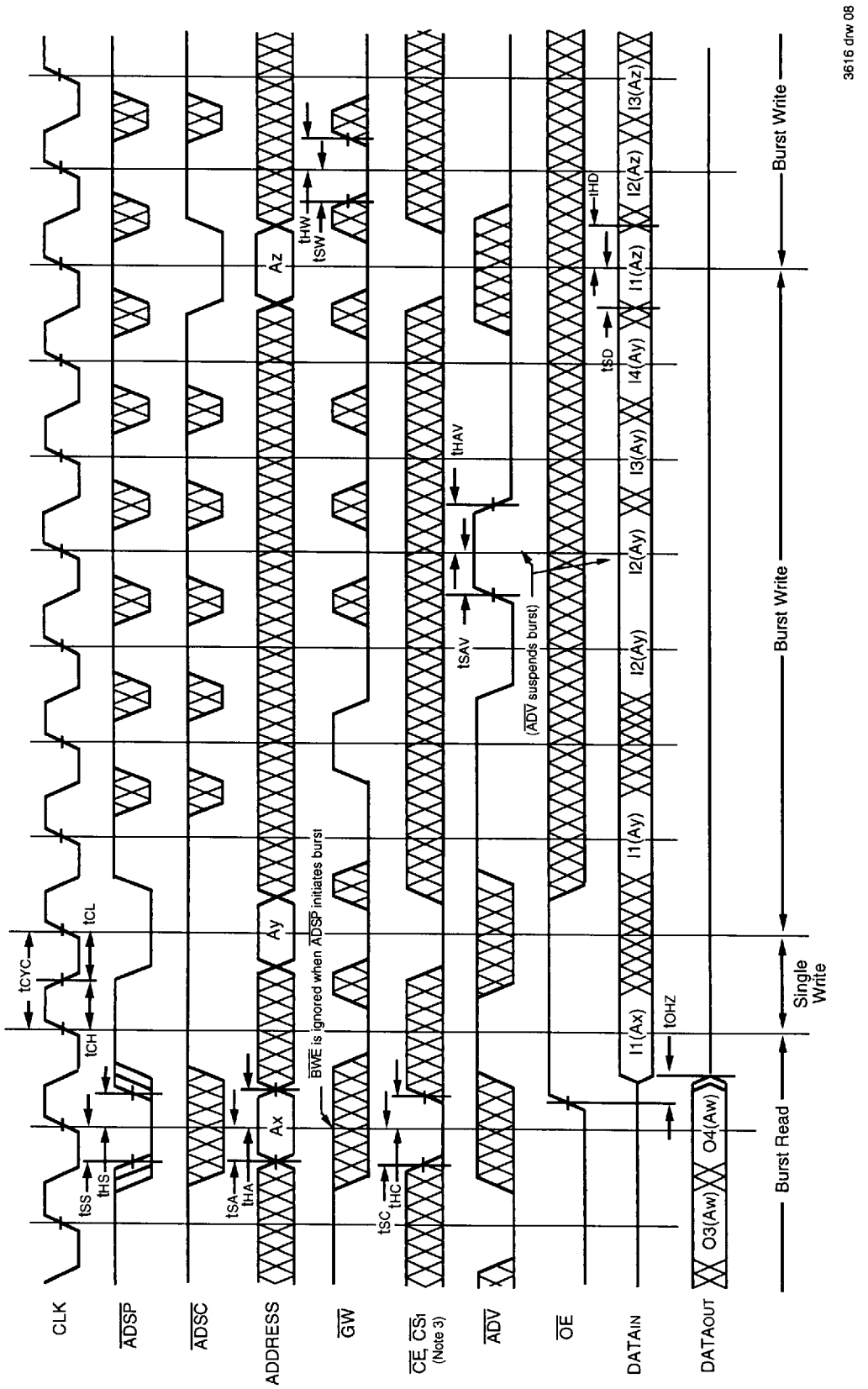
NOTES:
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS_1}$ signals. For example, when $\overline{CE}$ and $\overline{CS_1}$ are LOW on this waveform, CS_0 is HIGH.

TIMING WAVEFORM OF COMBINED PIPELINED READ AND WRITE CYCLES(1, 2, 3)



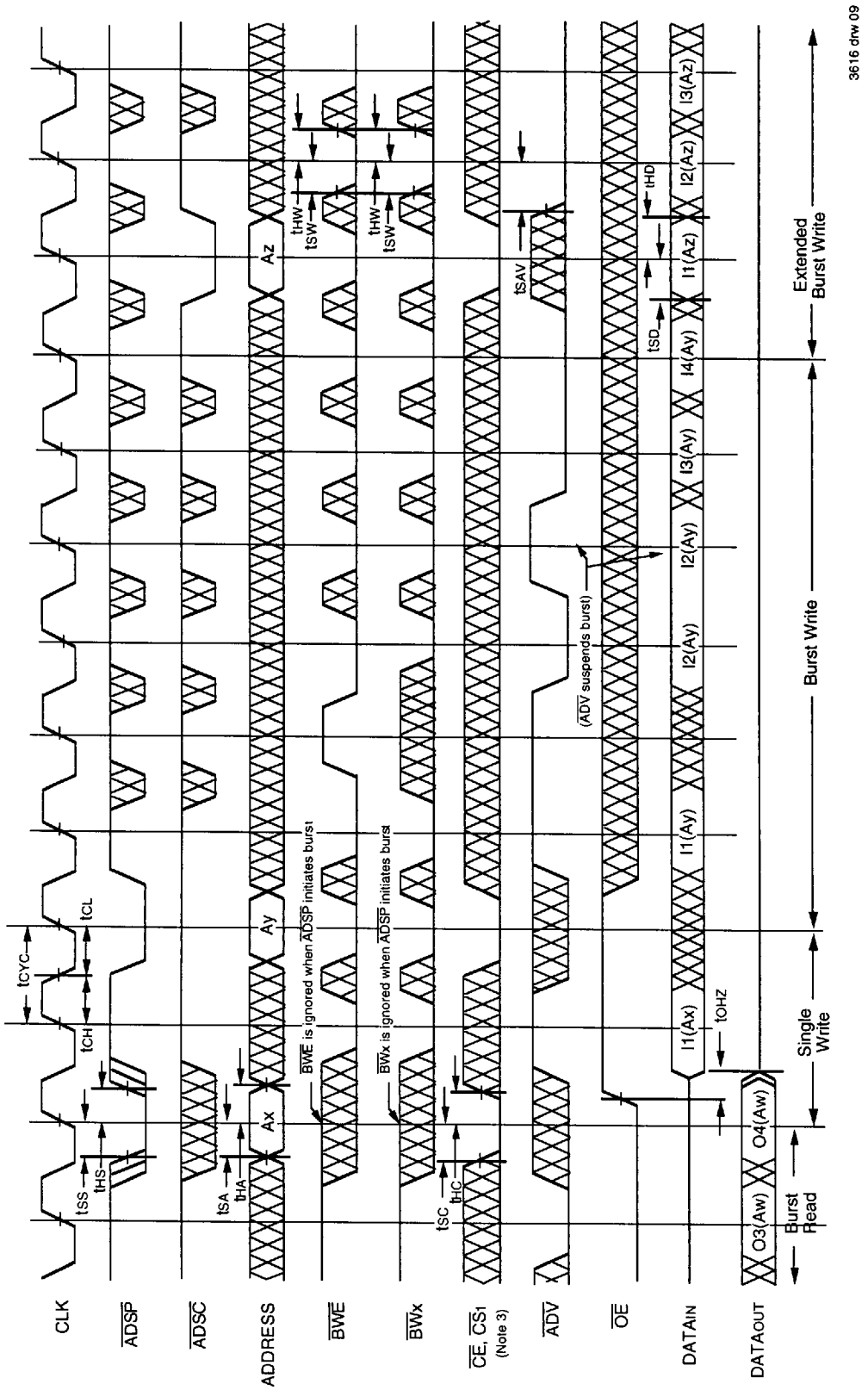
NOTES:
1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS_1}$ are LOW, CS_0 is HIGH.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 - $\overline{GW}$ CONTROLLED(1, 2, 3)



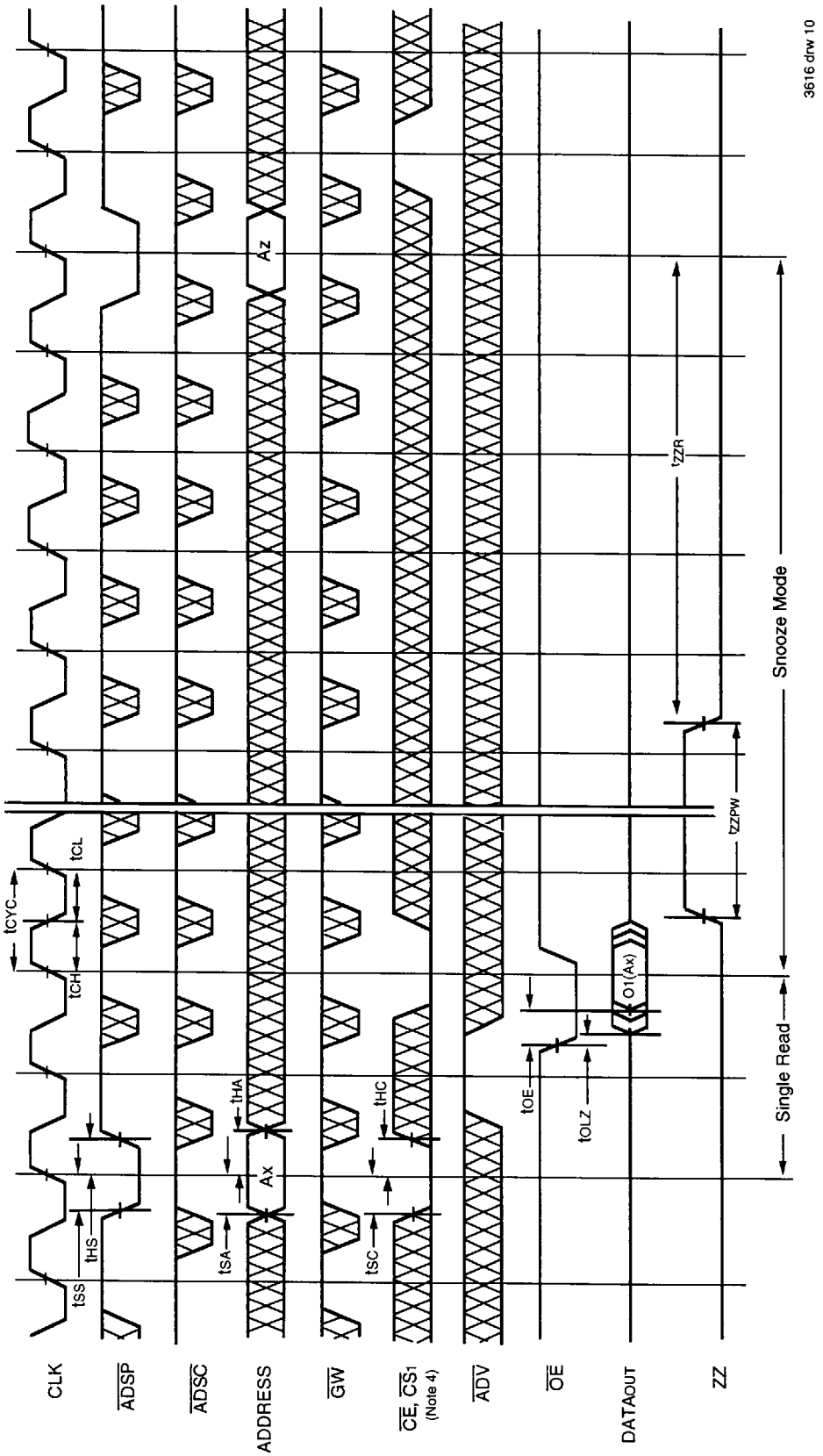
NOTES:
1. ZZ input is LOW, $\overline{BWE}$ is HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, CS0 is HIGH.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 - BYTE CONTROLLED(1, 2, 3)



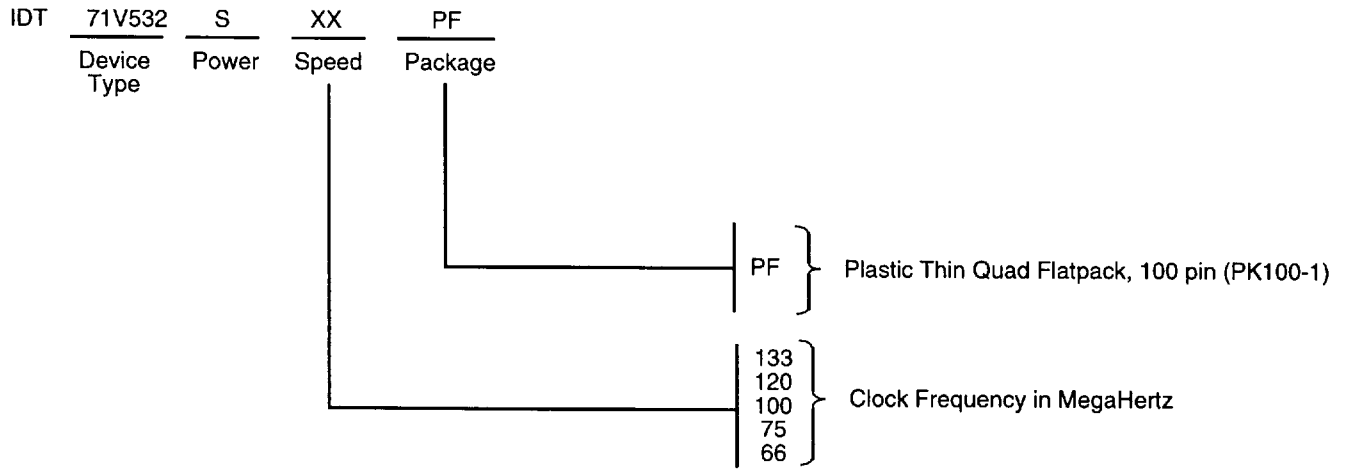
NOTES:
1. ZZ input is LOW, $\overline{GW}$ is HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, CS0 is HIGH.

TIMING WAVEFORM OF SLEEP (ZZ) AND POWER-DOWN MODES(1, 2, 3)



NOTES:
1. Device must power up in deselected Mode ($\overline{CE}$ and $\overline{CS}_1$ are HIGH, CS_0 is LOW).
2. $\overline{LBO}$ input is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, CS_0 is HIGH.

ORDERING INFORMATION



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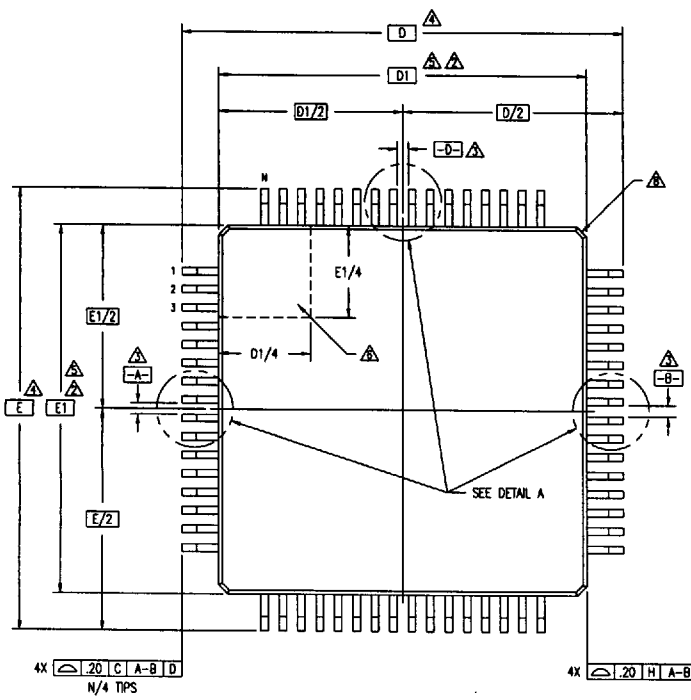
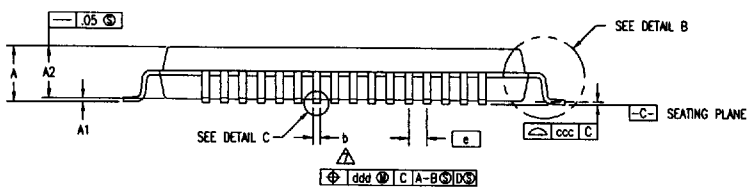
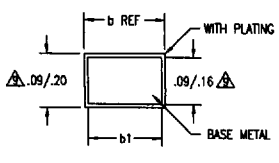
PACKAGE DIAGRAM OUTLINES

TQFP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	12/10/94	

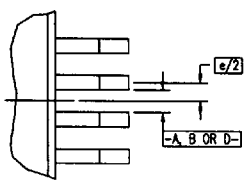




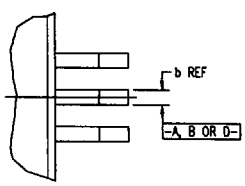


DETAIL C

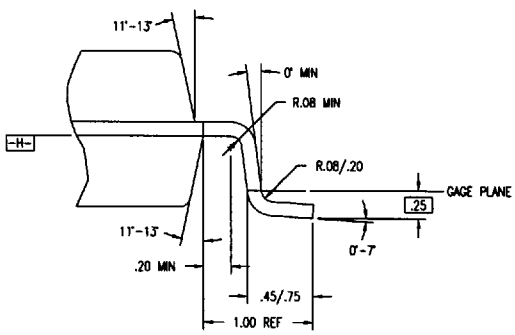
EVEN LEAD SIDES



ODD LEAD SIDES



DETAIL A



DETAIL B

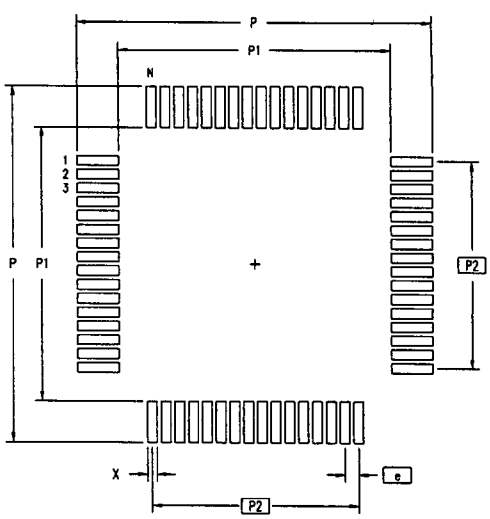
TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±	Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS / DRAWN AA 03/12/92 / CHECKED	TITLE: PN PACKAGE OUTLINE 14.0 X 14.0 X 1.4 mm TQFP 1.00/.10 FORM	
	SIZE C	DRAWING No. PSC-4036 REV 03
	DO NOT SCALE DRAWING	

TQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	11/18/94	

DWG #	PN64-1				PN80-1				PN100-1				PN120-1			
SYMBOL	JEDEC VARIATION BP			NOTE	JEDEC VARIATION BQ			NOTE	JEDEC VARIATION BR			NOTE	JEDEC VARIATION BS			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.60		–	–	1.60		–	–	1.60		–	–	1.60	
A1	.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15	
A2	1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45	
D	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
D1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
E	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
E1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
N	64				80				100				120			
e	.80 BSC				.65 BSC				.50 BSC				.40 BSC			
b	.30	.37	.45	7	.22	.32	.38	7	.17	.22	.27	7	.13	.18	.23	7
b1	.30	.35	.40		.22	.30	.33		.17	.20	.23		.13	.16	.19	
ccc	–	–	.10		–	–	.10		–	–	.08		–	–	.08	
ddd	–	–	.20		–	–	.13		–	–	.08		–	–	.07	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	16.80	17.00	16.80	17.00	16.80	17.00	16.80	17.00
P1	13.80	14.00	13.80	14.00	13.80	14.00	13.80	14.00
P2	12.00 BSC		12.35 BSC		12.00 BSC		11.60 BSC	
X	.40	.60	.30	.50	.30	.40	.20	.30
e	.80 BSC		.65 BSC		.50 BSC		.40 BSC	
N	64		80		100		120	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BP, BQ, BR & BS

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
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APPROVALS	DATE
DRAWN AA	03/12/92
CHECKED	

TITLE PN PACKAGE OUTLINE
14.0 X 14.0 X 1.4 mm TQFP
1.00/.10 FORM

SIZE C | DRAWING No. PSC-4036 | REV 03

DO NOT SCALE DRAWING