CMOS LSI

LC382161AT -10/12/15
2 MEG(65536 Words X 16 Bits X 2 Banks) Synchronous DRAM

Target Specifications

Overview

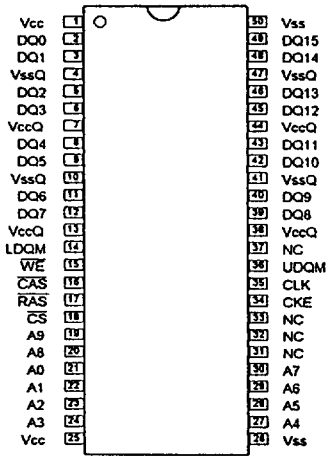
The LC382161AT product is a 3.3V single-voltage power supply Synchronous DRAM (SDRAM) with a 65536-word × 16-bit × 2-bank organization. This SDRAM features a large capacity, high speed, and low power due to the provision of synchronization circuits and the use of CMOS peripheral circuits. Thus this is optimal for use in a wide range of applications, from main and graphic memories in computers to consumer products. The LC382161AT SDRAM uses multiplexed address inputs and is packaged in a 50-pin TSOP Type II (400 mil) package that supports high-density mounting. This SDRAM uses auto-refresh (CBR refresh) performed 512 times every 8 ms as the refresh technique, and it can perform self-refresh completely automatically within the chip itself.

Features

- Organization: 65536 words × 16 bits × 2 banks
- All I/O signals (except CKE) are synchronized with the rising edge of the system clock.
- Basic specifications conform to the JEDEC standards for 16 Mbit synchronous DRAM.
- A pulse $\overline{RAS}$ scheme is used.
- Two bank internal structure (2 Banks × 65536 words × 16 bits). Continuous operation across the two banks is supported via the A9 pin.
- Burst length setting
  ·····(1, 2, 4, 8, or full page)
- Burst type setting (sequential or interleaved)
- Burst output operations are interruptible.
- The $\overline{CAS}$ latency can be set using an address key.
  ·····($\overline{CAS}$ latency : 1, 2, 3)
- Auto-refresh and self refresh functions
- Power-down and suspend operations can controlled from the CKE pin.
- I/O byte order is controlled by the DQM pin.
- Fabrication in a CMOS process
- 3.3V single-voltage power supply
- LVTTL compatible
- Low power
  Standby : 7.2mW
  Operating : 576mW
- Package: 400 mil 50 -pin TSOP Type II

Pin Assignments

400 mil 50 pin-TSOP II



Top View

Pin Description

Pin	Function
A0 to A7, A9	Address input
A8	Row address, auto-precharge input
DQ0 to DQ15	Data I/O
CLK	System clock input
CKE	Clock enable
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable
LDQM, UDQM	Data mask enable
Vcc	Power supply
Vss	Ground
VccQ	Data output power supply
VssQ	Data output ground
NC	No connection

Specifications and information herein are subject to change without notice.

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Pin Functions

Pin No.	Symbol	Type	Function (in detail)
35	CLK	Input	CLK is the master clock input for this device. Except for CKE, all input to this device are acquired in synchronization with the rising edge of this pin.
34	CKE	Input	The CKE input determines whether the CLK input is enabled within the device. When is CKE high, the next rising edge of the CLK signal will be valid, and when low, invalid. When CKE is low, the device will be in either the power-down mode, the clock suspend mode, or the self refresh mode. The CKE signal must remain low for these modes to remain in effect. CKE is an asynchronous input.
18	$\overline{CS}$	Input	The $\overline{CS}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{CS}$ is low, and disabled when $\overline{CS}$ is high. The device remains in the previous state when $\overline{CS}$ is high.
17	$\overline{RAS}$	Input	$\overline{RAS}$, in conjunction with $\overline{CAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
16	$\overline{CAS}$	Input	$\overline{CAS}$, in conjunction with $\overline{RAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
15	$\overline{WE}$	Input	$\overline{WE}$, in conjunction with $\overline{RAS}$ and $\overline{CAS}$, forms the device command. See the "Command Truth Table" item for details on device commands.
14,36	LDQM, UDQM	Input	LDQM and UDQM control the lower and upper bytes of the I/O buffers. In read mode, LDQM and UDQM control the output buffer. When LDQM or UDQM is Low, the corresponding buffer byte is enabled, and when high, disabled. The outputs go to the high impedance state when LDQM/UDQM is high. This function corresponds to $\overline{OE}$ in conventional DRAMs In write mode, LDQM and UDQM control the input buffer. When LDQM or UDQM is low, the corresponding buffer byte is enabled, and data can be written to the device. When LDQM or UDQM is high, input data is masked and cannot be written to the device.
19	A9	Input	A9 is the bank selection signal. When A9 is low, bank 0 is selected and when high, bank 1 is selected.This signal becomes part of the opcode during mode register set command input.
20	A8	Input	A8 is used as a row address during active command input, and is used to determine the precharge mode during other commands. If A8 is low during precharge command input, the bank selected by A9 is precharged, but if A8 is high, both banks will be precharged. This signal becomes part of the opcode during mode register set command input.
30	A7	Input	A7 is a column address. This signal becomes part of the opcode during mode register set command input.
21 to 24, 27 to 29	A0-A6	Input	A0 to A6 are address inputs. They are used as row address inputs during active command input and as column address inputs during read or write command input. These signals become part of the opcode during mode register set command input.
2,3,5,6,8,9,11, 12,39,40,42,43, 45,46,48,49	DQ0 to DQ15	Input / Output	DQ0 to DQ15 are I/O pins. I/O through these pins can be controlled in byte units using the LDQM and UDQM pins.
7,13,38,44	VccQ	Power supply	VccQ is the output buffer power supply.
4,10,41,47	VssQ	Power supply	VssQ is the output buffer ground.
1,25	Vcc	Power supply	Vcc is the device internal power supply.
26,50	Vss	Power supply	Vss is the device internal ground.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	unit	Note
Maximum supply voltage	Vcc max	-1.0 to +4.6	V	1
Maximum output supply voltage	VccQ max	-1.0 to +4.6	V	1
Input voltage	V_{IN}	-1.0 to +4.6	V	1
Output voltage	V_{OUT}	-1.0 to +4.6	V	1
Allowable power dissipation	Pd max	1	W	1
Output shorted current	I_{CS}	50	mA	1
Operating temperature	Topr	0 to +70	℃	1
Storage temperature	Tstg	-55 to +150	℃	1

Note: 1. This device may be destroyed if stresses in excess of the absolute maximum ratings are applied.

DC Recommended Operating Conditions at Ta = 0 to + 70℃

Parameter	Symbol	min.	typ.	max.	unit	Note
Supply voltage	Vcc, VccQ	3.0	3.3	3.6	V	2
Input high level voltage	V_{IH}	2.0	-	4.6	V	2
Input low level voltage	V_{IL}	-0.3	-	+0.8	V	2

Note: 2. All voltages are referenced to Vss.

DC Electrical Characteristics at Ta = 0 to + 70℃, Vcc = VccQ = 3.3 ± 0.3V

Parameter	Symbol	Conditions		Grade	min.	max.	unit	Note
Operating current	ICC1	One bank operation Burst length=1 tRC≧tRC (min.), I_{OUT} = 0mA		-10	-	120	mA	3,4
				-12	-	110		
				-15	-	100		
Precharge standby current (in power-down mode)	ICC2P	CKE≦V_{IL} (max.)	tCK = tCK(min.)	-	-	3	mA	
	ICC2PS		tCK = ∞	-	-	2	mA	
Precharge standby current (in non power-down mode)	ICC2N	CKE≧V_{IH} (min.)	tCK = tCK(min.)	-	-	30	mA	
	ICC2NS		tCK = ∞	-	-	15	mA	
Active standby current (in power-down mode)	ICC3P	CKE≦V_{IL} (max.)	tCK = tCK(min.)	-	-	3	mA	
	ICC3PS		tCK = ∞	-	-	2	mA	
Active standby current (in non power-down mode)	ICC3N	CKE≧V_{IH} (min.)	tCK = tCK(min.)	-	-	30	mA	
	ICC3NS		tCK = ∞	-	-	15	mA	
Operating current (in burst mode)	ICC4	tCK≧tCK (min.) I_{OUT} = 0mA	$\overline{CAS}$ latency = 3	-10	-	160	mA	3,4
				-12	-	140		
				-15	-	120		
			$\overline{CAS}$ latency = 2	-10	-	120		
				-12	-	110		
				-15	-	110		
			$\overline{CAS}$ latency = 1	-10	-	60		
				-12	-	55		
				-15	-	55		
Auto-refresh current	ICC5	tRC≧tRC (min.)		-10	-	100	mA	
				-12	-	90		
				-15	-	80		
Self-refresh current	ICC6	CKE≦0.2V		-	-	2	mA	
Input leakage current	I_{IL}	0V≦V_{IN}≦Vcc, with pins other than the tested pin at 0V		-	-10	+10	μA	
Output leakage current	I_{OL}	Output disabled, 0V≦V_{OUT}≦Vcc		-	-10	+10	μA	
High level output voltage	V_{OH}	I_{OUT} = -2mA		-	2.4	-	V	
Low level output voltage	V_{OL}	I_{OUT} = 2mA		-	-	0.4	V	

Note: 3. These are the values at the minimum cycle time. Since the currents are transient, these values decrease as the cycle time increases. Also note that a bypass capacitor of at least 0.01 μF should be inserted between Vcc and Vss for each memory chip to suppress power supply voltage noise (voltage drops) due to these transient currents.

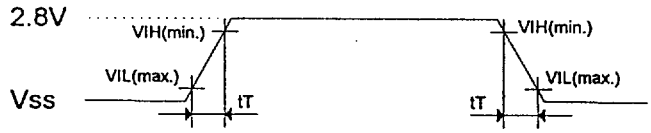
4. ICC1 and ICC4 depend on the output load. The maximum values for ICC1 and ICC4 are obtained with the output open state.

Operating Frequency / Latency Relationships

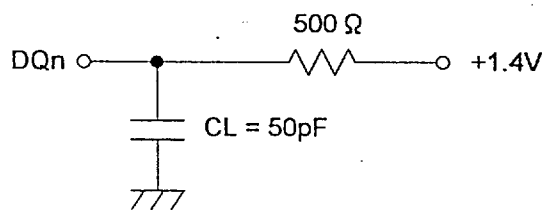
Parameter	Symbol	-10			-12			-15			unit
Clock cycle time	-	10	15	30	12	17	34	15	17	34	ns
Operating frequency	-	100	66	33	83	58	29	66	58	29	MHz
$\overline{CAS}$ latency	tCAC	3	2	1	3	2	1	3	2	1	cycle
Active command to read / write command delay time	tRCD	3	2	1	3	2	1	3	2	1	cycle
$\overline{RAS}$ latency (tRCD + tCAC)	tRAC	6	4	2	6	4	2	6	4	2	cycle
Command period (REF to REF / ACT to ACT)	tRC	9	6	3	9	7	4	9	7	4	cycle
Command period (ACT to PRE)	tRAS	6	4	2	6	5	3	6	5	3	cycle
Command period (PRE to ACT)	tRP	3	2	1	3	2	1	3	2	1	cycle
Command period (ACT(0) to ACT(1))	tRRD	3	2	1	3	2	1	3	2	1	cycle
Column command delay time (READ, READA, WRIT, WRITA)	tCCD	1	1	1	1	1	1	1	1	1	cycle
Input data to precharge command delay time	tDPL	2	1	1	2	1	1	2	1	1	cycle
Input data to active/refresh command delay time(during auto-precharge)	tDAL	5	3	2	5	3	2	5	3	2	cycle
Burst stop command to output in Hi-Z delay time (read)	tRBD	3	2	1	3	2	1	3	2	1	cycle
Burst stop command to input in invalid delay time (write)	tWBD	0	0	0	0	0	0	0	0	0	cycle
Precharge command to output in Hi-Z delay time (read)	tRQL	2	2	1	2	2	1	2	2	1	cycle
Precharge command to input in invalid delay time (write)	tWDL	-1	0	0	-1	0	0	-1	0	0	cycle
Last output to auto-precharge start time (read)	tPQL	-1	-1	0	-1	-1	0	-1	-1	0	cycle
DQM to output delay time (read)	tQMD	2	2	2	2	2	2	2	2	2	cycle
DQM to input delay time (write)	tDMD	0	0	0	0	0	0	0	0	0	cycle
Mode register set to command delay time	tMCD	2	2	2	2	2	2	2	2	2	cycle

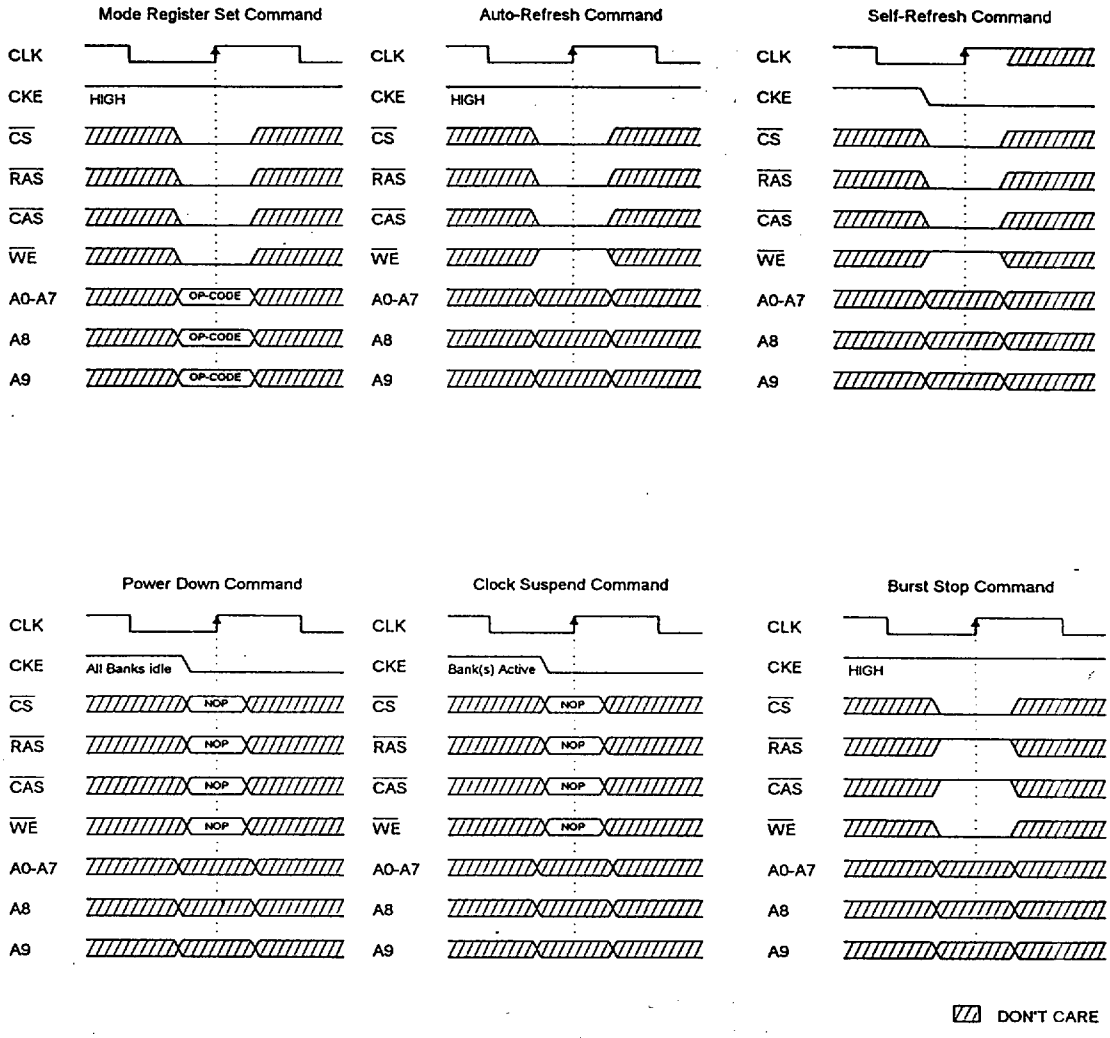
AC Test Conditions (Input / Output reference level :1.4V)

Input



Output Load





Self-Refresh Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$,CKE=Low, $\overline{WE}$ =High)

This command executes the self-refresh operation. The row address to be refreshed, the bank, and the refresh interval are generated automatically internally during this operation. The self-refresh operation is started by dropping the CKE pin from high to low. The self-refresh operation continues as long as the CKE pin remains low and there is no need for external control of any other pins. The self-refresh operation is terminated by raising the CKE pin from low to high. The next command cannot be executed until the device internal recovery period (tRC) has elapsed. After the self-refresh, since it is impossible to determine the address of the last row to be refreshed, an auto-refresh should immediately be performed for all addresses(512 cycles).
Both banks must be placed in the idle state before executing this command.

Burst Stop Command ($\overline{CS}$, $\overline{WE}$ =Low, $\overline{RAS}$, $\overline{CAS}$ =High)

The command forcibly terminates burst read and write operations. When this command is executed during a burst read operation, data output stops after the $\overline{CAS}$ latency period has elapsed.

No Operation ($\overline{CS}$ =Low, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ =High)

This command has no effect on the device.

Device Deselect Command ($\overline{CS}$ =High)

This command dose not select the device for an object of operation. In other words, it performs no operation with respect to the device.

Power-Down Command (CKE=Low)

When both banks are in the idle (inactive) state, or when at least one of the banks is not in the idle state (inactive) state, this command can be used to suppress device power dissipation by reducing device internal operations to the absolute minimum. Power-down mode is started by dropping the CKE pin from high to low. Power-down mode continues as long as the CKE pin is held low. All pins other than the CKE pin are invalid and none of the other commands can be executed in this mode. The power-down operation is terminated by raising the CKE pin from low to high. The next command cannot be executed until the recovery period (tCKA) has elapsed.
Since this command differs from the self-refresh command described above in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (tREF). Thus the maximum time that power-down mode can be held is just under the refresh cycle time.

Clock Suspend (CKE=Low)

This command can be used to stop the device internal clock temporarily during a read or write cycle. Clock suspend mode is started by dropping the CKE pin from high to low. Clock suspend mode continues as long as the CKE pin is held low. All input pins other than the CKE pin are invalid and none of the other commands can be executed in this mode. Also note that the device internal state is maintained. Clock suspend mode is terminated by raising the CKE pin from low to high, at which point device operation restarts. The next command cannot be executed until the recovery period (tCKA) has elapsed.
Since this command differs from the self-refresh command described above in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (tREF). Thus the maximum time that clock suspend mode can be held is just under the refresh cycle time.

Operation Command Table (Note 10,11)

Current state	CS	RAS	CAS	WE	A9	A8	A7-A0	Command	Operation	Note
Idle	H	X	X	X	X	X	X	DESL	No operation or power-down	21
	L	H	H	H	X	X	X	NOP	No operation or power-down	21
	L	H	H	L	X	X	X	BST	No operation or power-down	
	L	H	L	H	V	V	V	READ/READA	Illegal	
	L	H	L	L	V	V	V	WRIT/WRITA	Illegal	
	L	L	H	H	V	V	V	ACT	Row active	
	L	L	H	L	V	V	X	PRE/PALL	No operation	
	L	L	L	H	X	X	X	REF/SELF	Auto-refresh or self-refresh	22
	L	L	L	L	OP CODE			MRS	Mode register set	
Row active	H	X	X	X	X	X	X	DESL	No operation	
	L	H	H	H	X	X	X	NOP	No operation	
	L	H	H	L	X	X	X	BST	No operation	
	L	H	L	H	V	V	V	READ/READA	Read start	26
	L	H	L	L	V	V	V	WRIT/WRITA	Write start	26
	L	L	H	H	V	V	V	ACT	Illegal	19
	L	L	H	L	V	V	X	PRE/PALL	Precharge	24
	L	L	L	H	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE			MRS	Illegal	
Read	H	X	X	X	X	X	X	DESL	Burst read continues, row active when done	
	L	H	H	H	X	X	X	NOP	Burst read continues, row active when done	
	L	H	H	L	X	X	X	BST	Burst interrupted, row active after interrupt	
	L	H	L	H	V	V	V	READ/READA	Burst interrupted, read restart after interrupt	25
	L	H	L	L	V	V	V	WRIT/WRITA	Burst interrupted, write start after interrupt	20,25
	L	L	H	H	V	V	V	ACT	Illegal	19
	L	L	H	L	V	V	X	PRE/PALL	Burst read interrupted, precharge after interrupt	
	L	L	L	H	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE			MRS	Illegal	
Write	H	X	X	X	X	X	X	DESL	Burst write continues, write recovery when done	
	L	H	H	H	X	X	X	NOP	Burst write continues, write recovery when done	
	L	H	H	L	X	X	X	BST	Burst write interrupted, row active after interrupt	
	L	H	L	H	V	V	V	READ/READA	Burst write interrupted, read start after interrupt	20,25
	L	H	L	L	V	V	V	WRIT/WRITA	Burst write interrupted, write restart after interrupt	25
	L	L	H	H	V	V	V	ACT	Illegal	19
	L	L	H	L	V	V	X	PRE/PALL	Burst write interrupted, precharge after interrupt	
	L	L	L	H	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE			MRS	Illegal	
Read with auto-precharge	H	X	X	X	X	X	X	DESL	Burst read continues, precharge when done	
	L	H	H	H	X	X	X	NOP	Burst read continues, precharge when done	
	L	H	H	L	X	X	X	BST	Illegal	
	L	H	L	H	V	V	V	READ/READA	Illegal	
	L	H	L	L	V	V	V	WRIT/WRITA	Illegal	
	L	L	H	H	V	V	V	ACT	Illegal	19
	L	L	H	L	V	V	X	PRE/PALL	Illegal	19
	L	L	L	H	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE			MRS	Illegal	

Continued from preceding page.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7-A0	Command	Operation	Note
Write recovery with auto-precharge	H	X	X	X	X	X	X	DESL	No operation, idle state after tDAL has elapsed	
	L	H	H	H	X	X	X	NOP	No operation, idle state after tDAL has elapsed	
	L	H	H	L	X	X	X	BST	No operation, idle state after tDAL has elapsed	
	L	H	L	H	V	V	V	READ/READA	Illegal	19
	L	H	L	L	V	V	V	WRIT/WRITA	Illegal	19
	L	L	H	H	V	V	V	ACT	Illegal	19
	L	L	H	L	V	V	X	PRE/PALL	Illegal	19
	L	L	L	H	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE			MRS	Illegal	
Refresh	H	X	X	X	X	X	X	DESL	No operation, idle state after tRP has elapsed	
	L	H	H	H	X	X	X	NOP	No operation, idle state after tRP has elapsed	
	L	H	H	L	X	X	X	BST	No operation, idle state after tRP has elapsed	
	L	H	L	H	V	V	V	READ/READA	Illegal	
	L	H	L	L	V	V	V	WRIT/WRITA	Illegal	
	L	L	H	H	V	V	V	ACT	Illegal	
	L	L	H	L	V	V	X	PRE/PALL	Illegal	
	L	L	L	H	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE			MRS	Illegal	
Mode register set	H	X	X	X	X	X	X	DESL	No operation, idle state after tMCD has elapsed	
	L	H	H	H	X	X	X	NOP	No operation, idle state after tMCD has elapsed	
	L	H	H	L	X	X	X	BST	No operation, idle state after tMCD has elapsed	
	L	H	L	H	V	V	V	READ/READA	Illegal	
	L	H	L	L	V	V	V	WRIT/WRITA	Illegal	
	L	L	H	H	V	V	V	ACT	Illegal	
	L	L	H	L	V	V	X	PRE/PALL	Illegal	
	L	L	L	H	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE			MRS	Illegal	

Note: 10. H: High level input, L: Low level input, X: High or low level input, V: Valid data input
11. All input signals are latched on the rising edge of the CLK signal.
12. Both banks must be placed in the inactive (idle) state in advance.
13. The state of the A0 to A9 pins is loaded into the mode register as an OP code.
14. The row address is generated automatically internally at this time. The DQ pin and the address pin data is ignored.
15. During a self-refresh operation, all pin data (states) other than CKE is ignored.
16. The selected bank must be placed in the inactive (idle) state in advance.
The row address A7 is invalid during the active command input.
17. The selected bank must be placed in the active state in advance.
18. This command is valid only when the burst length set to full page.
19. This is possible depending on the state of the bank selected by the A9 pin.
20. Time to switch internal busses is required.
21. The LC382161AT can be switched to power-down mode by dropping the CKE pin low when both banks in the idle state.
Input pins other than CKE are ignored at this time.
22. The LC382161AT can be switched to self-refresh mode by dropping the CKE pin low when both banks in the idle state.
Input pins other than CKE are ignored at this time.
23. Possible if tRRD is satisfied.
24. Illegal if tRAS is not satisfied.
25. The conditions for burst interruption must be observed.
Also note that the LC382161AT will enter the precharged state immediately after the burst operation completes if auto-precharge is selected.
26. Command input becomes possible after the period tRCD has elapsed.
Also note that the LC382161AT will enter the precharged state immediately after the burst operation completes if auto-precharge is selected.

Two Banks Operation Command Truth Table (Note 31,32)

$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7-A0	Operation	Previous state		Next state	
								BANK 0	BANK 1	BANK 0	BANK 1
H	X	X	X	X	X	X	DESL	Any	Any	Any	Any
L	H	H	H	X	X	X	NOP	Any	Any	Any	Any
L	H	H	L	X	X	X	BST	R/W/A	I/A	A	I/A
								I	I/A	I	I/A
								I/A	R/W/A	I/A	A
								I/A	I	I/A	I
L	H	L	H	H	H	CA	READ	I/A	R/W/A	I/A	RP
				H	H	CA	READA	R/W	A	A	RP
				H	L	CA		I/A	R/W/A	I/A	R
				H	L	CA		R/W	A	A	R
				L	H	CA		R/W/A	I/A	RP	I/A
				L	H	CA		A	R/W	RP	A
				L	L	CA		R/W/A	I/A	R	I/A
				L	L	CA		A	R/W	R	A
L	H	L	L	H	H	CA	WRIT	I/A	R/W/A	I/A	WP
				H	H	CA	WRITA	R/W	A	A	WP
				H	L	CA		I/A	R/W/A	I/A	W
				H	L	CA		R/W	A	A	W
				L	H	CA		R/W/A	I/A	WP	I/A
				L	H	CA		A	R/W	WP	A
				L	L	CA		R/W/A	I/A	W	I/A
				L	L	CA		A	R/W	W	A
L	L	H	H	H	RA	RA	ACT	Any	I	Any	A
				L	RA	RA		I	Any	A	Any
L	L	H	L	X	H	X	PRE	R/W/A/I	I/A	I	I
				X	H	X	PALL	I/A	R/W/A/I	I	I
				H	L	X		I/A	R/W/A/I	I/A	I
				H	L	X		R/W/A/I	I/A	R/W/A/I	I
				L	L	X		R/W/A/I	I/A	I	I/A
				L	L	X		I/A	R/W/A/I	I	R/W/A/I
L	L	L	H	X	X	X	REF	I	I	I	I
L	L	L	L	OP CODE			MRS	I	I	I	I

Note: 31. H: High level input, L: Low level input, X: High or low level input, RA: Row address, CA: Column Address
The row address A7 is invalid during the active command input.

32. The device state symbols are interpreted as follows.

I	: Idle (inactive) state
A	: Row active state
R	: Read
W	: Write
RP	: Read with auto-precharge
WP	: Write with auto-precharge
Any	: Any state

Device Initialization at Power-on (power-on sequence)

As is the case with conventional DRAMs, the LC382161AT product must be initialized by executing a stipulated power-on sequence after power is applied.
After power is applied and Vcc and VccQ reach their stipulated voltages, set and hold the CKE and DQM pins high for 100μs. Then, execute the precharge command to precharge both bank. Next, execute the auto-refresh command twice or more and define the device operation mode by executing a mode register set command.
The mode register set command can be also set before auto-refresh command.

Mode Register Settings

The mode register set command sets the mode register. When this command is executed, pins A0 to A7, A8, and A9 function as data input pins for setting the register, and this data becomes the device internal OP code. This OP code has four fields as listed in the table below.

Input pin	Field
A9, A8, A7	Option
A6 ,A5, A4	$\overline{\text{CAS}}$ latency
A3	Burst type
A2 ,A1, A0	Burst length

Note that the mode register set command can be executed only when both banks are in the idle (inactive) state. Wait at least two cycle after executing a mode register set command before executing the next command.

$\overline{\text{CAS}}$ Latency

During a read operation, the between the execution of the read command and data output is stipulated as the $\overline{\text{CAS}}$ latency. This period can be set using the mode register set command. The optimal $\overline{\text{CAS}}$ latency is determined by the clock frequency and device speed grade(-10/12/15). See the "Operating Frequency / Latency Relationships" item on page 7 for details on the relationship between the clock frequency and the $\overline{\text{CAS}}$ latency. See the table on the next page for details on setting the mode register.

Burst Length

When writing or reading, data can be input or output data continuously. In these operations, an address is input only once and that address is taken as the starting address internally by the device. The device then automatically generates the following address. The burst length field in the mode register stipulates the number of data items input or output in sequence. In the LC382161AT product, a burst length of 1, 2, 4, 8, or full page can be specified. See the Table on the next page for details on setting the mode register.

Burst Type

The burst data order during a read or write operation is stipulated by the burst type, which can be set by the mode register set command. The LC382161AT product supports sequential mode and interleaved mode burst type settings. See the table on the next page for details on setting the mode register. See the "Burst Length and Column Address Sequence" item on page 21 for details on I/O data orders in these modes.

Burst Length and Column Address Sequence

Burst length	Column address A2 A1 A0	Address sequence	
		Sequential	Interleaved
2	x x 0	0-1	0-1
	x x 1	1-0	1-0
4	x 0 0	0-1-2-3	0-1-2-3
	x 0 1	1-2-3-0	1-0-3-2
	x 1 0	2-3-0-1	2-3-0-1
	x 1 1	3-0-1-2	3-2-1-0
8	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n n n	Cn,Cn+1,Cn+2, Cn+3,Cn+4..... ...Cn-1(Cn+255), Cn(Cn+256).....	None

Note: The burst length in full page mode is 256.

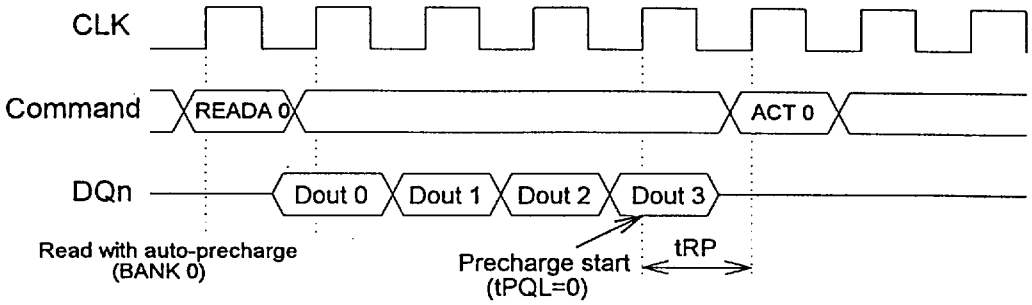
Bank Select and Precharge Address Allocation

Row	X0	-	Row address	
	X1	-	Row address	
	X2	-	Row address	
	X3	-	Row address	
	X4	-	Row address	
	X5	-	Row address	
	X6	-	Row address	
	X7	-	Invalid	
	X8	0	Precharge of the selected bank (Precharge command)	Row address (active command)
		1	Precharge of both banks (precharge command)	
	X9	0	Bank 0 selected (precharge and active command)	
		1	Bank 1 selected (precharge and active command)	
Column	Y0	-	Column address	
	Y1	-	Column address	
	Y2	-	Column address	
	Y3	-	Column address	
	Y4	-	Column address	
	Y5	-	Column address	
	Y6	-	Column address	
	Y7	-	Column address	
	Y8	0	Auto-precharge not performed	
		1	Auto-precharge performed	
	Y9	0	Bank 0 selected (read and write commands)	
		1	Bank 1 selected (read and write commands)	

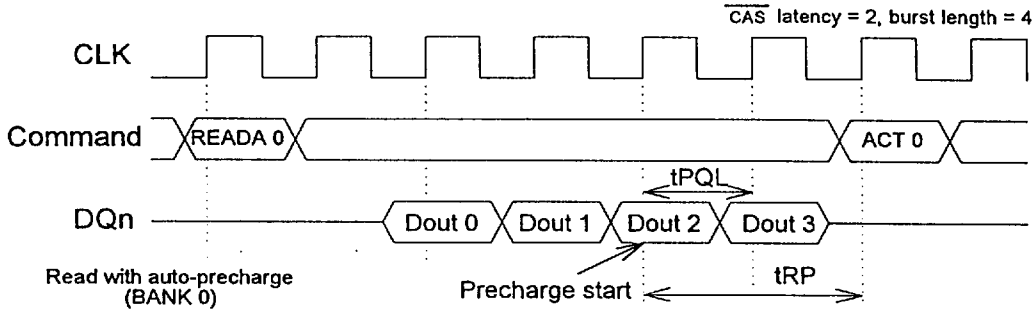
Read with Auto-Precharge

The read with auto-precharge command first executes a burst read operation and then puts the selected bank in the precharged state automatically. After the precharge completes, the bank goes to the idle state. Thus this command performs a read command and a precharge command in a single operation.
During this operation, the delay period (tPQL) between the last burst data output and the start of the precharge operation differs depending on the $\overline{CAS}$ latency setting. When the $\overline{CAS}$ latency setting is one, the precharge operation starts at the same time as the last burst data is output (tPQL = 0), and when the $\overline{CAS}$ latency setting is two or three, the precharge operation starts on one clock cycle before the last burst data is output (tPQL = -1). Therefore, the selected bank can be made active after a delay of tRP from the start position of this precharge operation.
The selected bank must be set to the active state before executing this command.
The auto-precharge function is invalid if the burst length is set to full page.

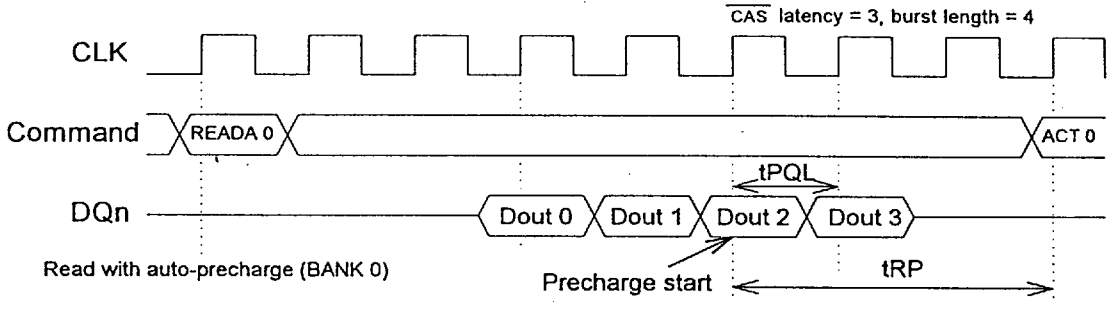
$\overline{CAS}$ latency = 1, burst length = 4



$\overline{CAS}$ latency = 2, burst length = 4



$\overline{CAS}$ latency = 3, burst length = 4

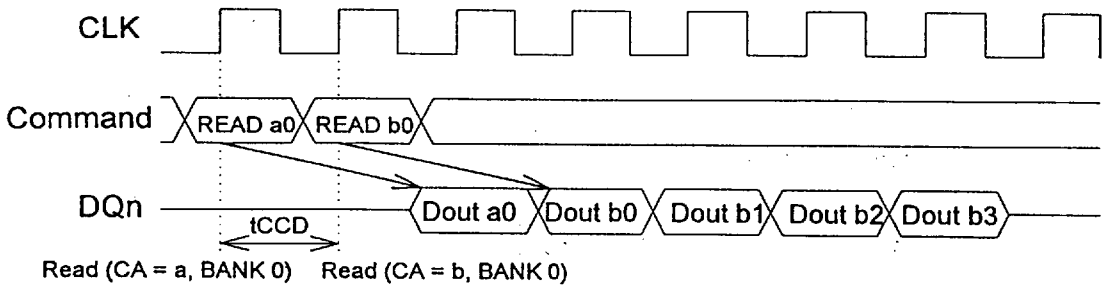


$\overline{CAS}$ latency	3	2	1
tPQL	-1	-1	0

Interval between Read Command

A new command can be executed while a read cycle is in progress, i.e., before that cycle completes. When the second read command is executed, after the $\overline{CAS}$ latency has elapsed, data corresponding to the new read command is output in place of the data due to the previous read command.
The interval between two read command (tCCD) must be at least one clock cycle.
The selected bank must be set to the active state before executing this command.

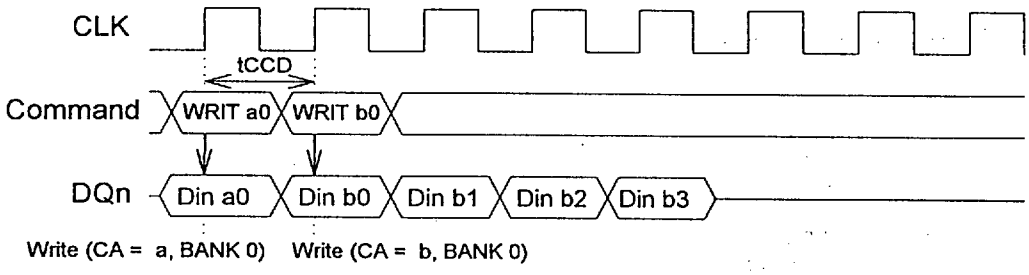
$\overline{CAS}$ latency = 2, burst length = 4



Interval between Write Command

A new write command can be executed while a write cycle is in progress, i.e., before that cycle completes. At the point the second write command is executed, data corresponding to the new write command can be input in place of the data for the previous write command.
The interval between two write commands (tCCD) must be at least one clock cycle.
The selected bank must be set to the active state before executing this command.

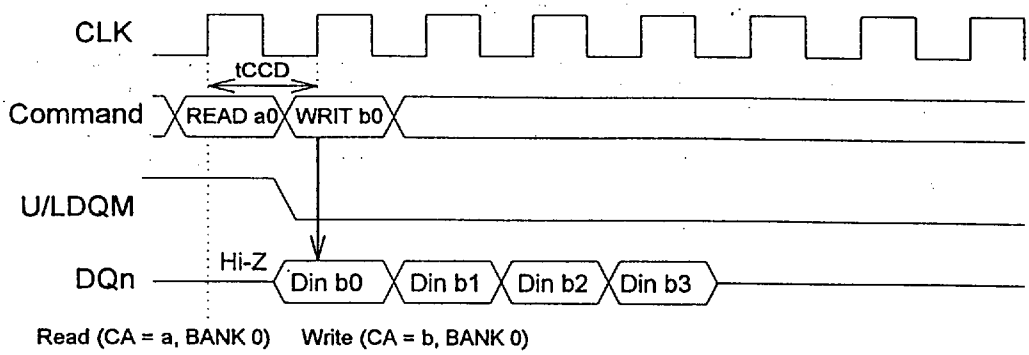
$\overline{CAS}$ latency = 2, burst length = 4



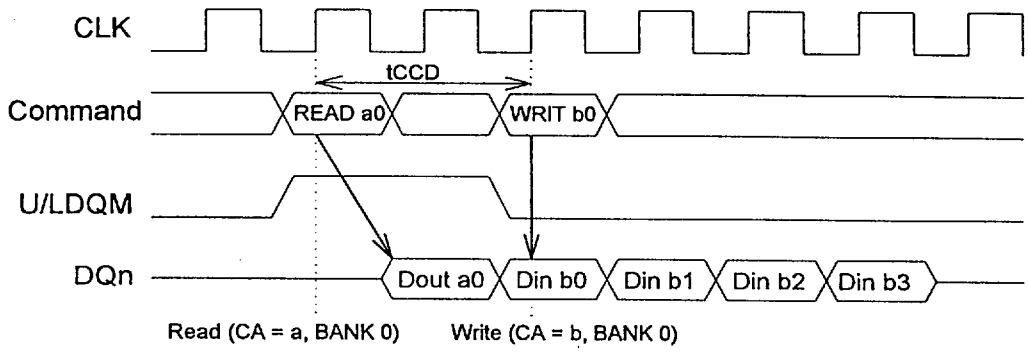
Interval between Read and Write Commands

A read command can be interrupted and a new write command executed while the read cycle is in progress, i.e., before that cycle completes. Data corresponding to the new write command can be input at the point new write command is executed. To prevent collision between input and output data at the DQn pins during this operation, the output data must be masked using the U/LDQM pins. The interval (tCCD) between these commands must be at least 1 clock cycle. The selected bank must be set to the active state before executing this command.

$\overline{CAS}$ latency = 1, 2, 3, burst length = 4

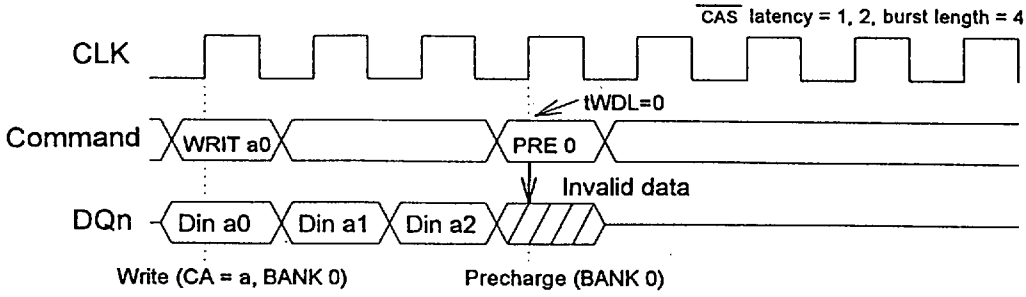


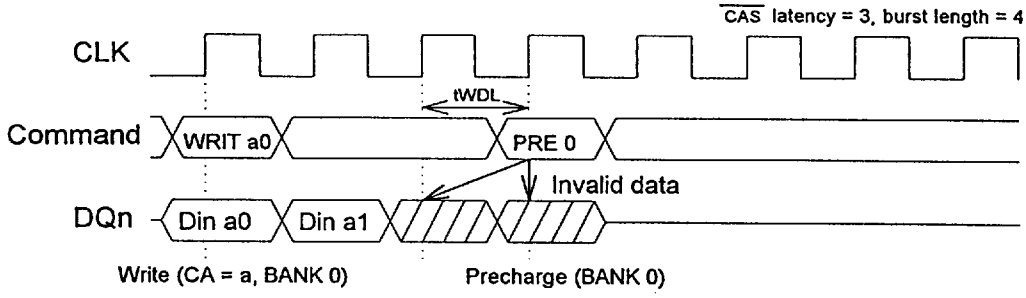
$\overline{CAS}$ latency = 1, burst length = 4

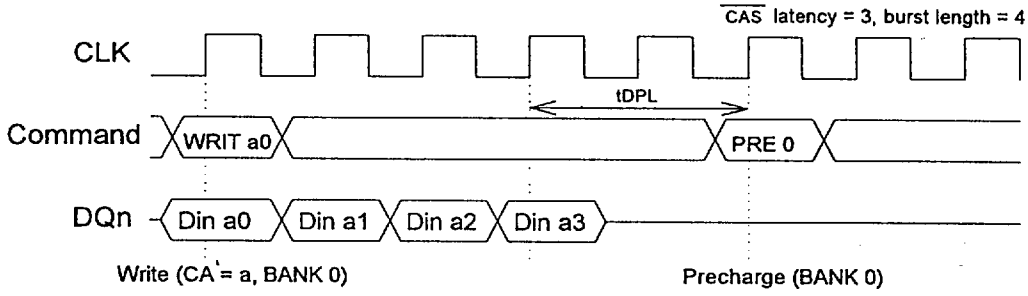


Write Cycle Interruption Using the Precharge Command

A write cycle can be interrupted by the execution of the precharge command before that cycle completes. The delay time (tWDL) from the precharge command to the point where burst input is invalid, i.e., the point where input data is no longer written to device internal memory is zero clock cycles, when the $\overline{CAS}$ latency is one or two, and minus one clock cycle when the $\overline{CAS}$ latency is three.
Inversely, to write all the burst data to the device, the precharge command must be executed after the write data recovery period (tDPL) has elapsed. Therefore, when the $\overline{CAS}$ latency setting is one or two, the precharge command must be executed on one clock cycle that follows the input of the last burst data item. When the $\overline{CAS}$ latency setting is three, the precharge command must be executed on two clock cycle that follows the input of the last burst data item.



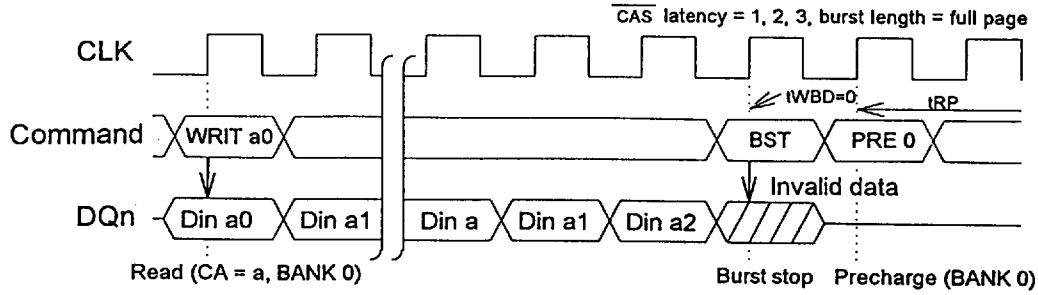




$\overline{CAS}$ latency	3	2	1
tWDL	-1	0	0
tDPL	2	1	1

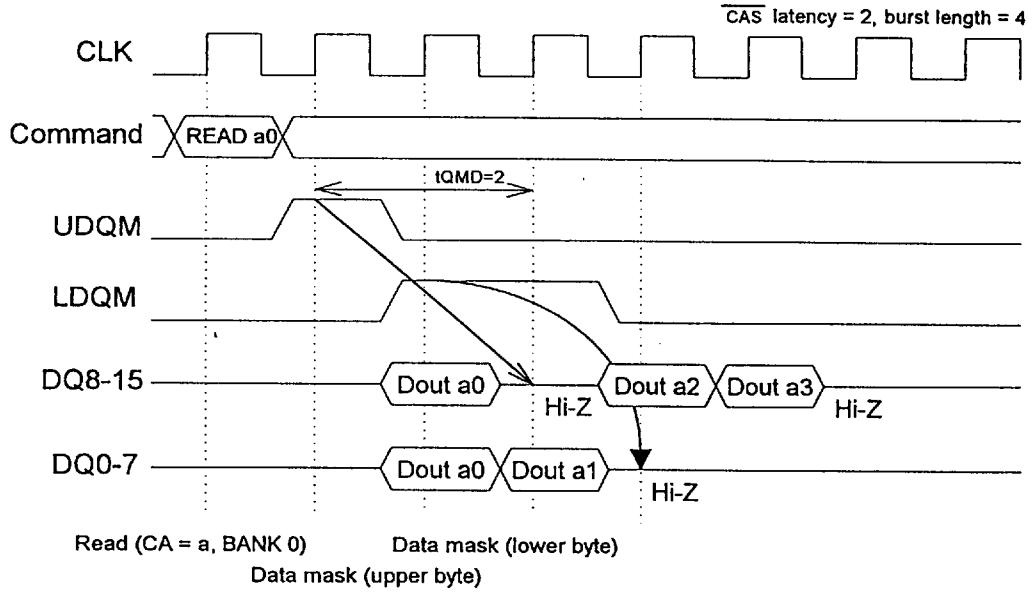
Write Cycle (full page) Interruption Using the Burst Stop Command

The LC382161AT can input data continuously from the burst start address (a) to location a + 255 during a write cycle in which the burst length is set to full page. The LC382161AT repeats the operation starting at the 256th cycle with data input returning to location (a) and continuing with a + 1, a + 2, a + 3, etc. A burst stop command must be executed to terminate this cycle. A precharge command must be executed with the ACT to PRE command period (tRAS max.) following the burst stop command. After the period (tWBD) required for burst data input to stop following the execution of the burst stop command has elapsed, the write cycle terminates. This period (tWBD) is zero clock cycles, regardless of the $\overline{\text{CAS}}$ latency.



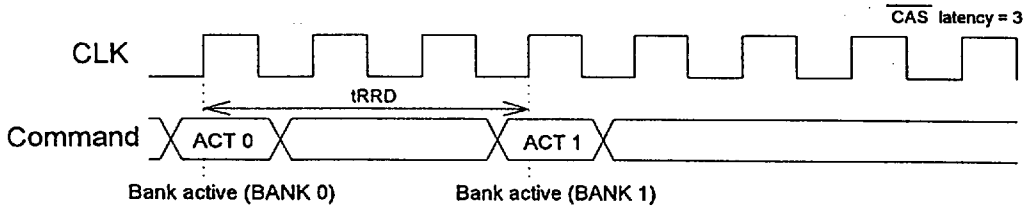
Burst Data Interruption Using the U/LDQM Pins (read cycle)

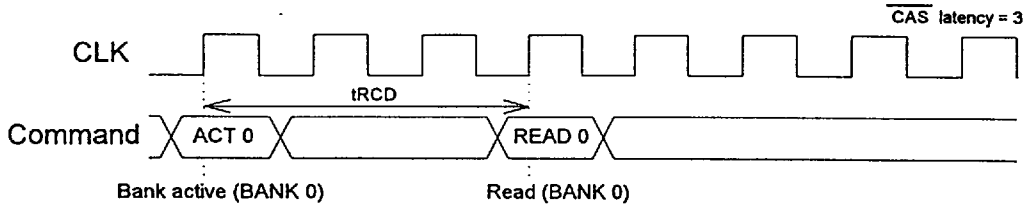
Burst data output can be temporarily interrupted (masked) during a read cycle using the U/LDQM pins. Regardless of the $\overline{\text{CAS}}$ latency, two clock cycles (tQMD) after one of the U/LDQM pins goes high, the corresponding outputs go to the high impedance state. Subsequently, the outputs are maintained in the high impedance state as long as that U/LDQM pin remains high. When the U/LDQM pin goes low, output is resumed at a time tQMD later. This output control operates independently on a byte basis with the UDQM pin controlling upper byte output (pins DQ8 to DQ15) and the LDQM pin controlling lower byte output (pins DQ0 to DQ7).
Since the U/LDQM pins control the device output buffers only, the read cycle continues internally and, in particular, incrementing of the internal burst counter continues.



Bank Active Command Interval

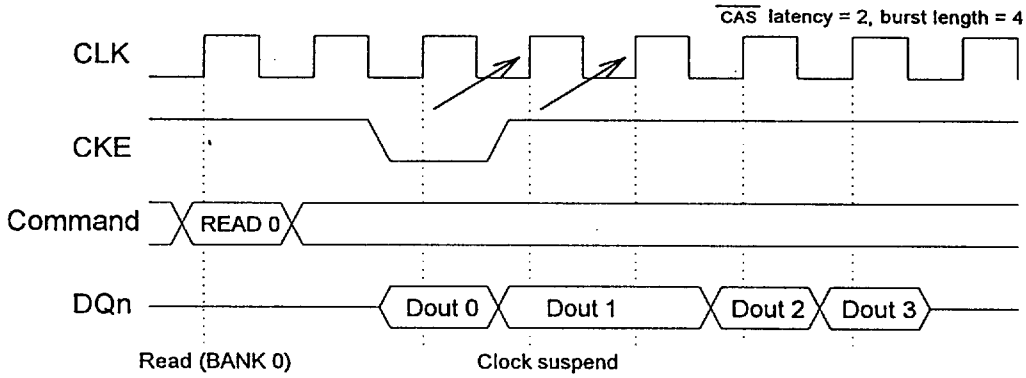
When the selected bank is precharged, the period tRP has elapsed and the bank has entered the idle state, the bank can be activated by executing the active command. If the other bank is in the idle state at that time, the active command can be executed for that bank after the period tRRD has elapsed. At that point both banks will be in the active state. When a bank active command has been executed, a precharge command must be executed for that bank within the ACT to PRE command period (tRAS max.). Also note that a precharge command cannot be executed for an active bank before tRAS(min.) has elapsed.
After a bank active command has been executed and the tRCD period has elapsed, read write (including auto-precharge) commands can be executed for that bank.





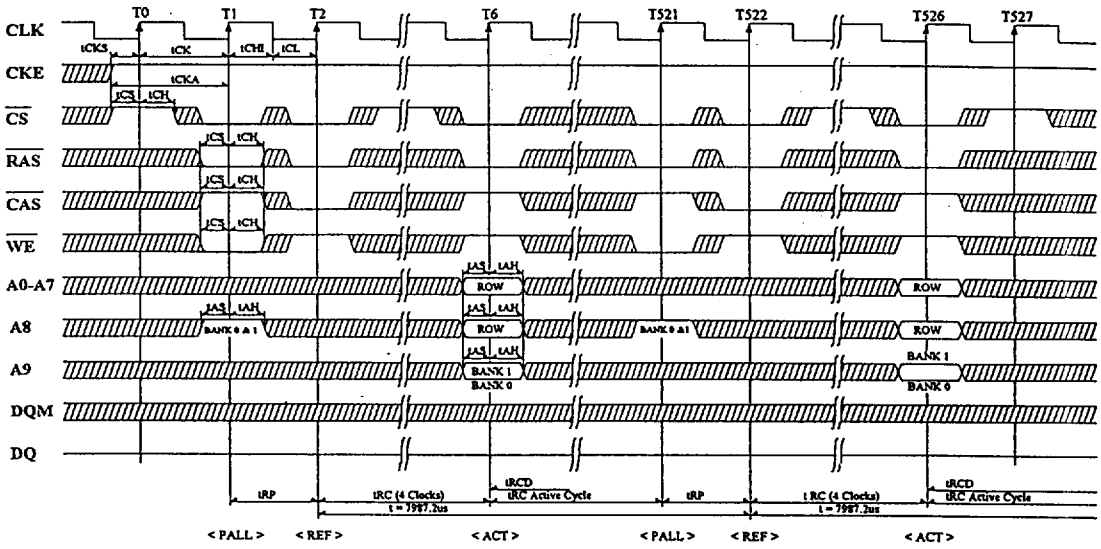
Clock Suspend

When the CKE pin is dropped from high to low during a read or write cycle, the LC382161AT enters clock suspend mode on the next CLK rising edge. This command reduces the device power dissipation by stopping the device internal clock. Clock suspend mode continues as long as the CKE pin remains low. In this state, all inputs other than CKE pin are invalid and no other commands can be executed. Also, the device internal states are maintained. When the CKE pin goes from low to high, clock suspend mode is terminated on the next CLK rising edge and device operation resumes.
The next command cannot be executed until the recovery period (tCKA) has elapsed.
Since this command differs from the self-refresh command described previously in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (tREF). Thus the maximum time that clock suspend mode can be held is just under the refresh cycle time.



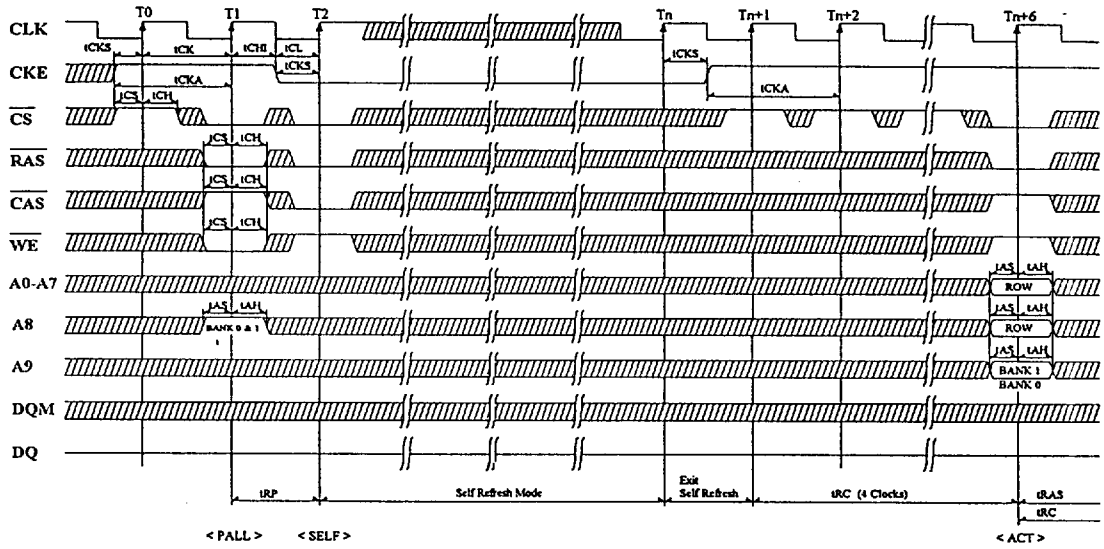
Auto-Refresh Cycle

$\overline{CAS}$ latency = 1



Self-Refresh Cycle

$\overline{CAS}$ latency = 1

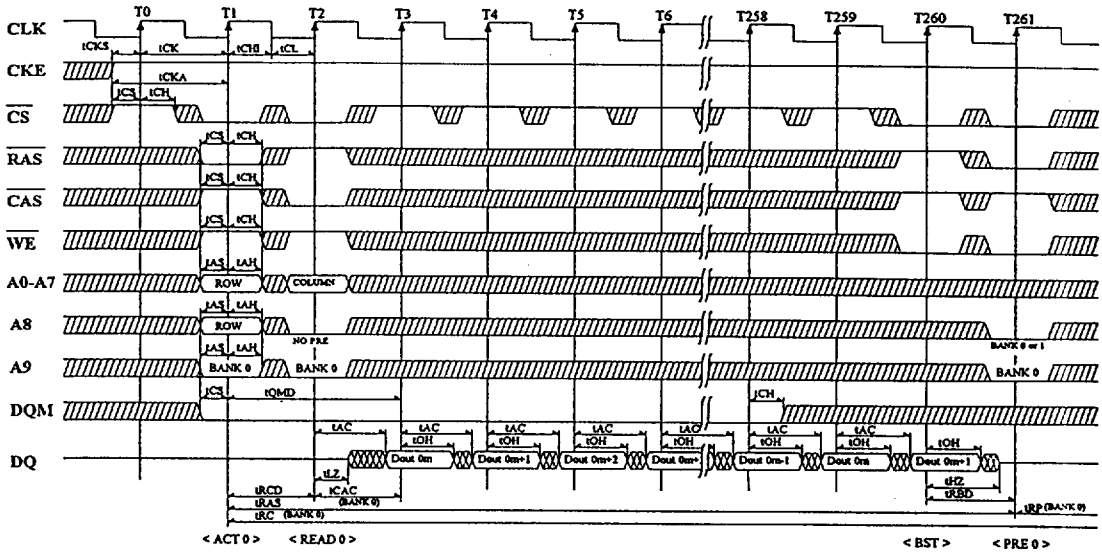


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

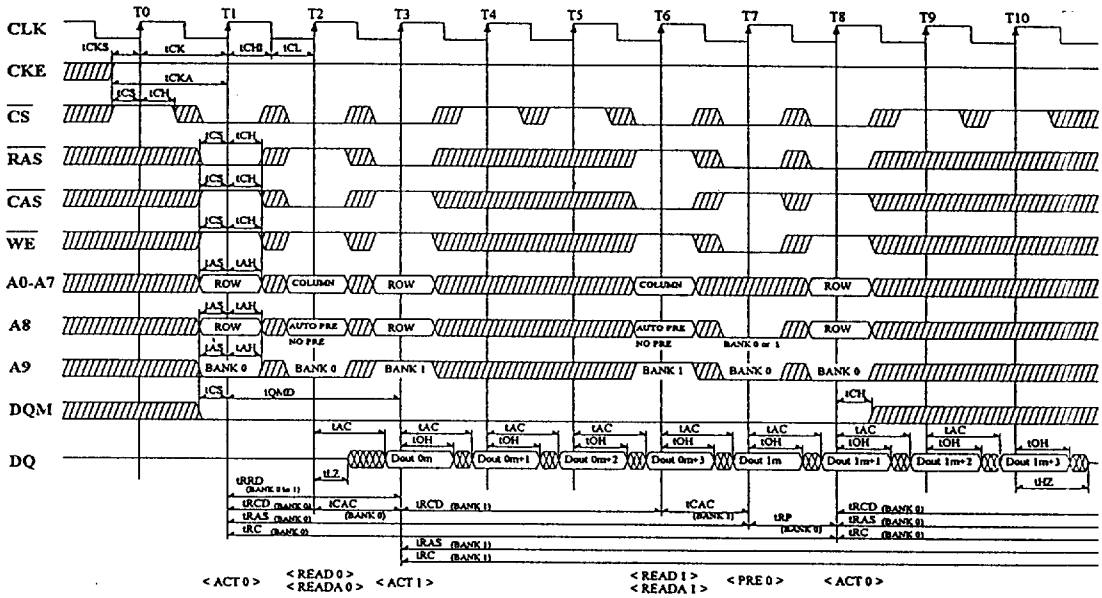
Read Cycle / Full Page

$\overline{CAS}$ latency = 1, burst length = Full Page



Read Cycle / Ping-Pong Operation (bank switching)

$\overline{CAS}$ latency = 1 , burst length = 1

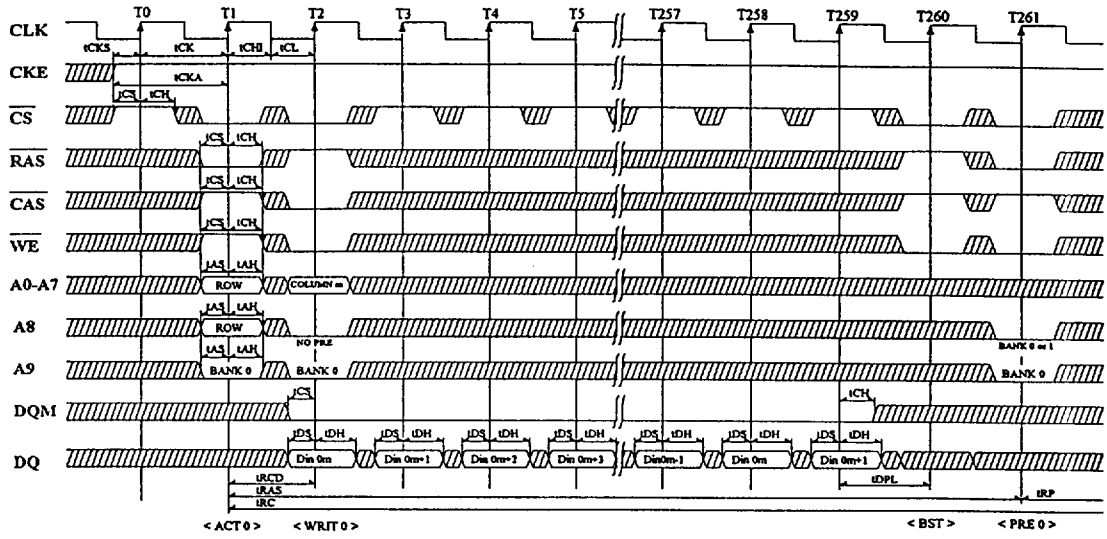


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

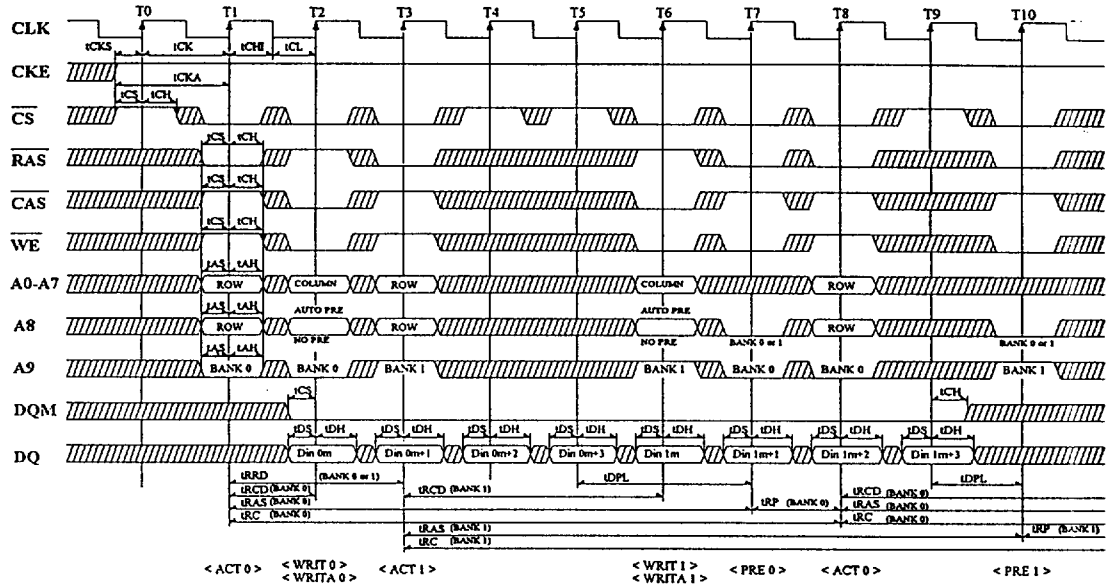
Write Cycle / Full Page

$\overline{CAS}$ latency = 1, burst length = Full Page



Write Cycle / Ping-Pong Operation (bank switching)

$\overline{CAS}$ latency = 1, burst length = 4

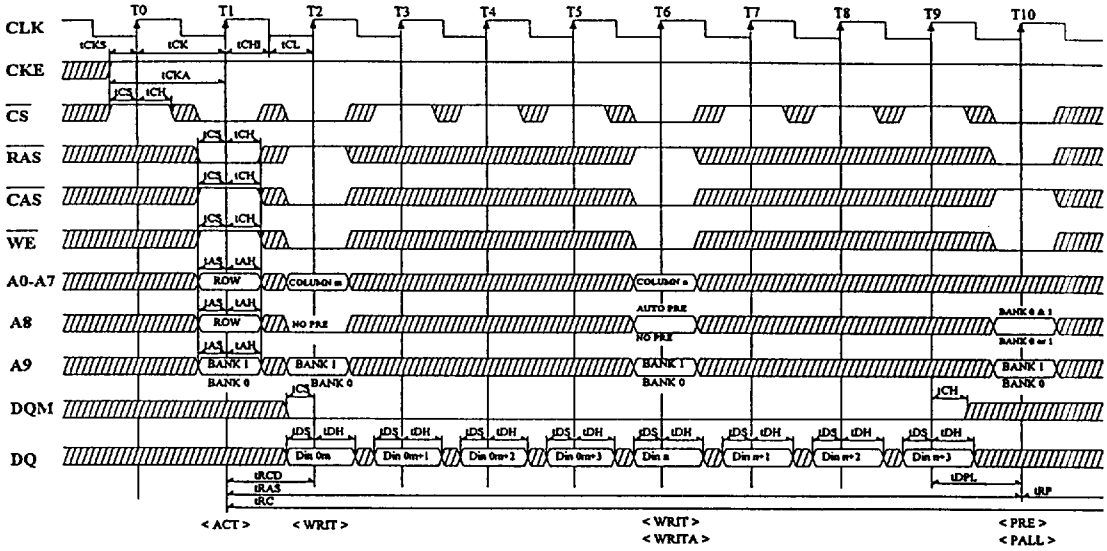


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

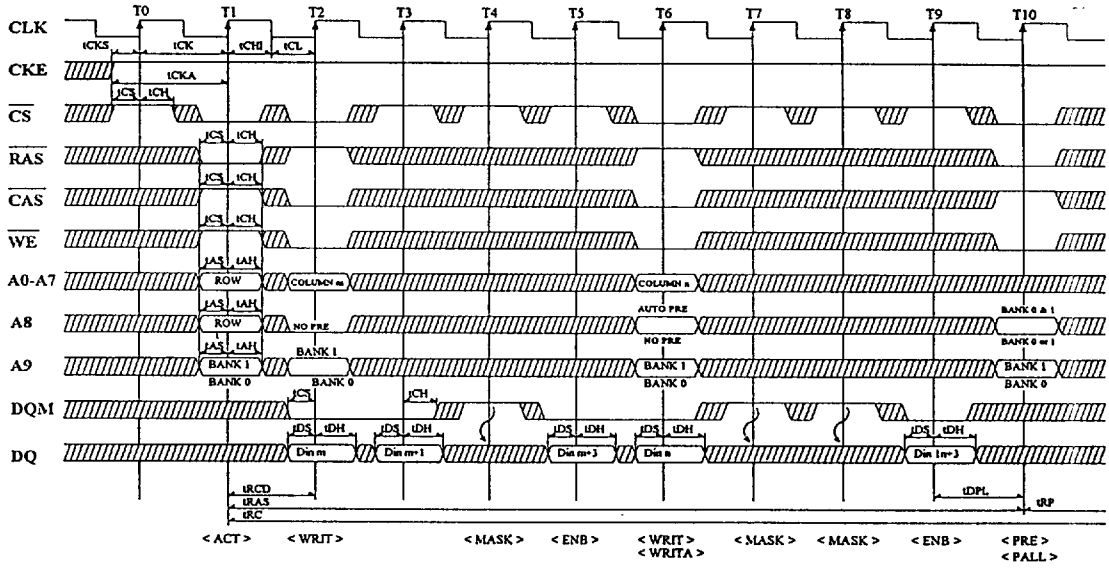
Write Cycle / Page Mode

$\overline{CAS}$ latency = 1, burst length = 4



Write Cycle / Mode ; Data Masking

$\overline{CAS}$ latency = 1 , burst length = 4

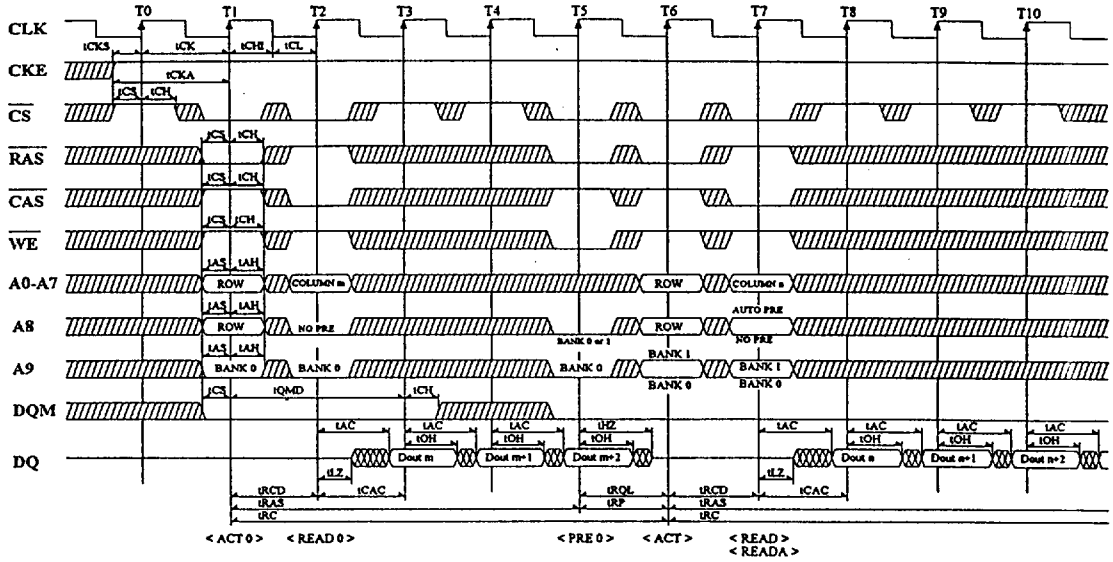


▨ DON'T CARE ▩ INVALID DATA

Note: The row address A7 is invalid during the active command input.

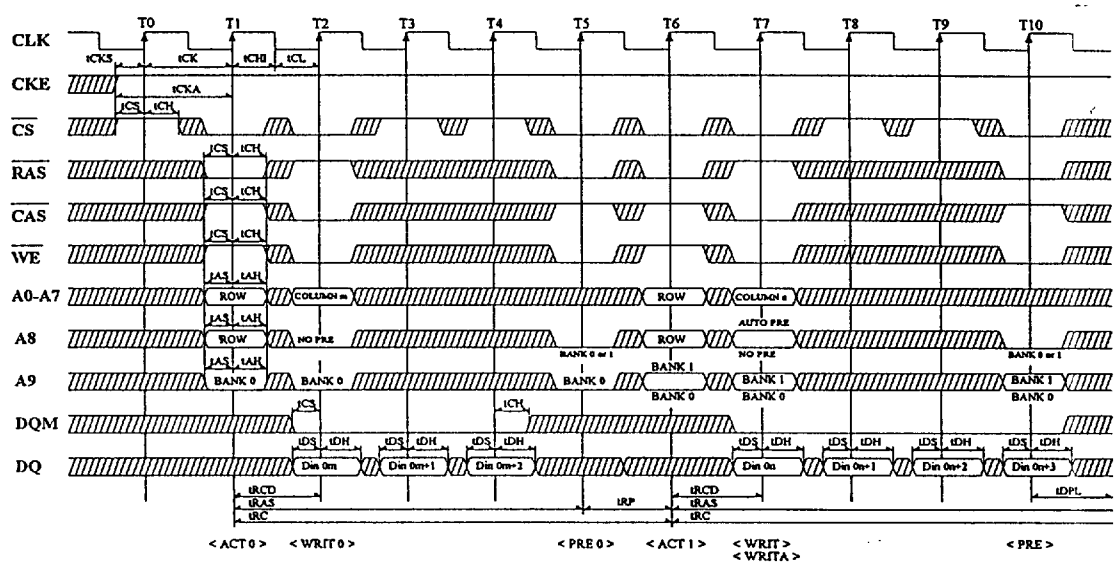
Read Cycle / Precharge Termination

$\overline{CAS}$ latency = 1, burst length = 4



Write Cycle / Precharge Termination

$\overline{CAS}$ latency = 1, burst length = 4

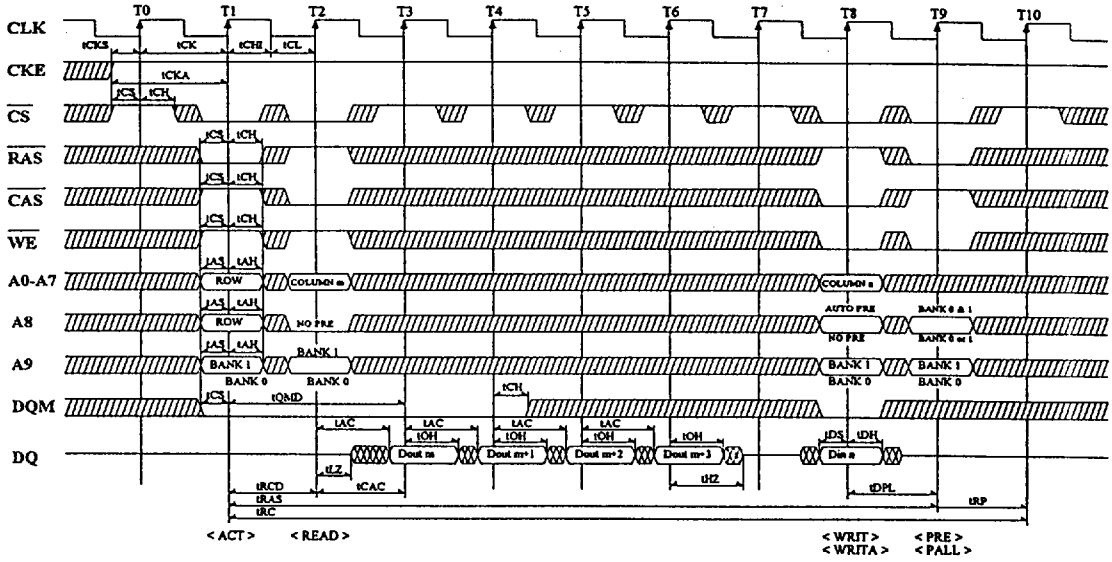


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

Read Cycle, Write Cycle / Burst Read, Single Write

$\overline{CAS}$ latency = 1, burst length = 4

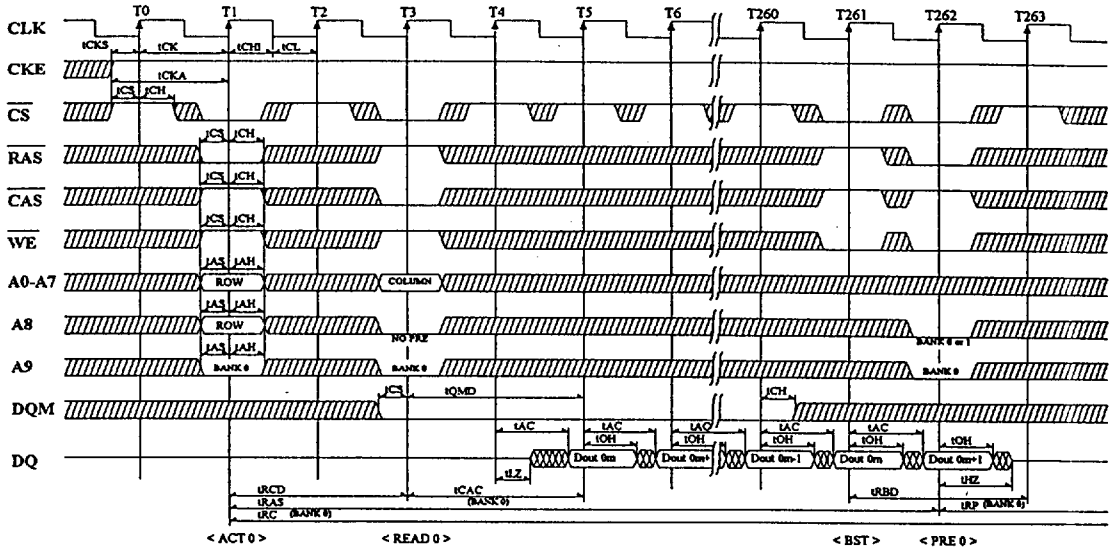


▨ DON'T CARE ▩ INVALID DATA

Note: The row address A7 is invalid during the active command input.

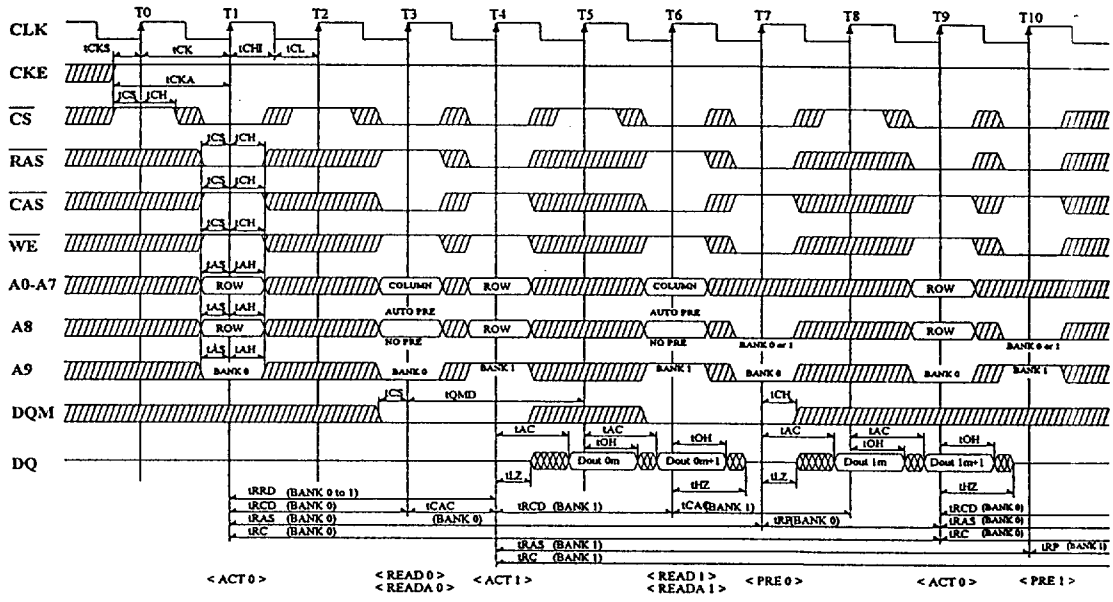
Read Cycle / Full Page

$\overline{CAS}$ latency = 2, burst length = Full Page



Read Cycle / Ping-Pong Operation (bank switching)

$\overline{CAS}$ latency = 2, burst length = 2

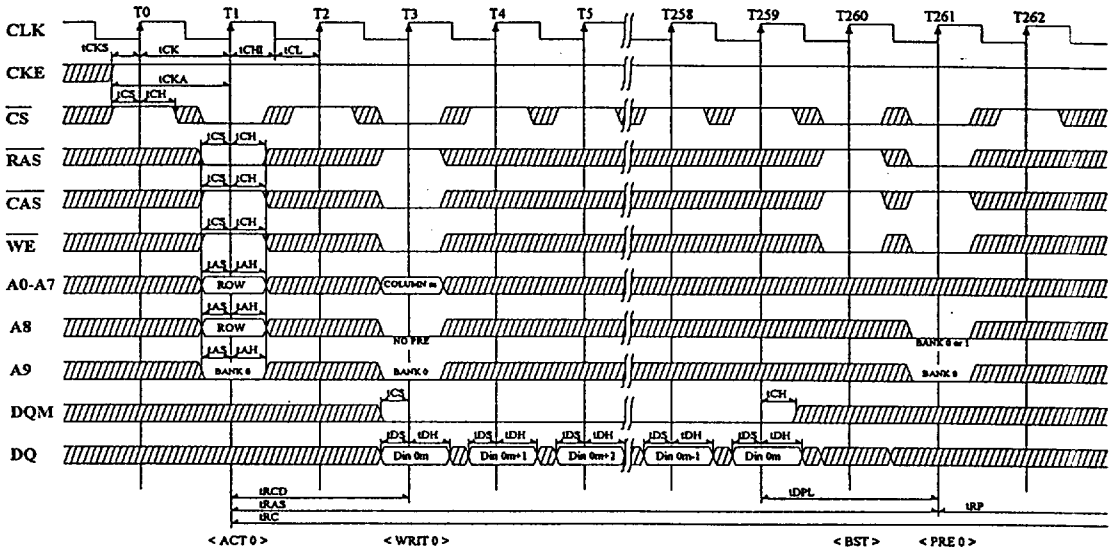


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

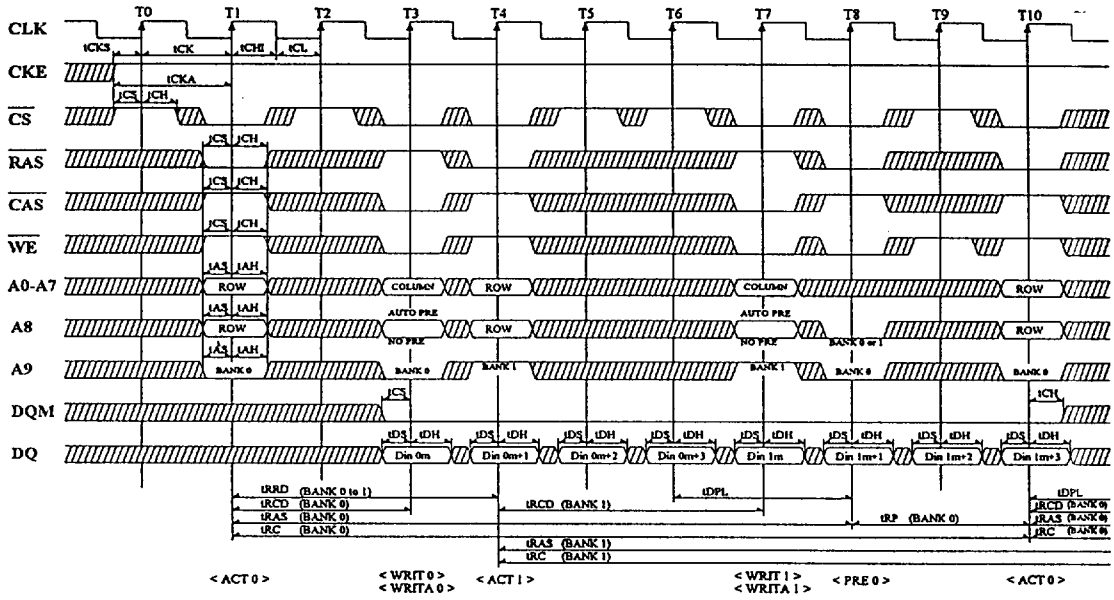
Write Cycle / Full Page

$\overline{CAS}$ latency = 2 ,burst length = Full Page



Write Cycle / Ping-Pong Operation

$\overline{CAS}$ latency = 2 ,burst length = 2

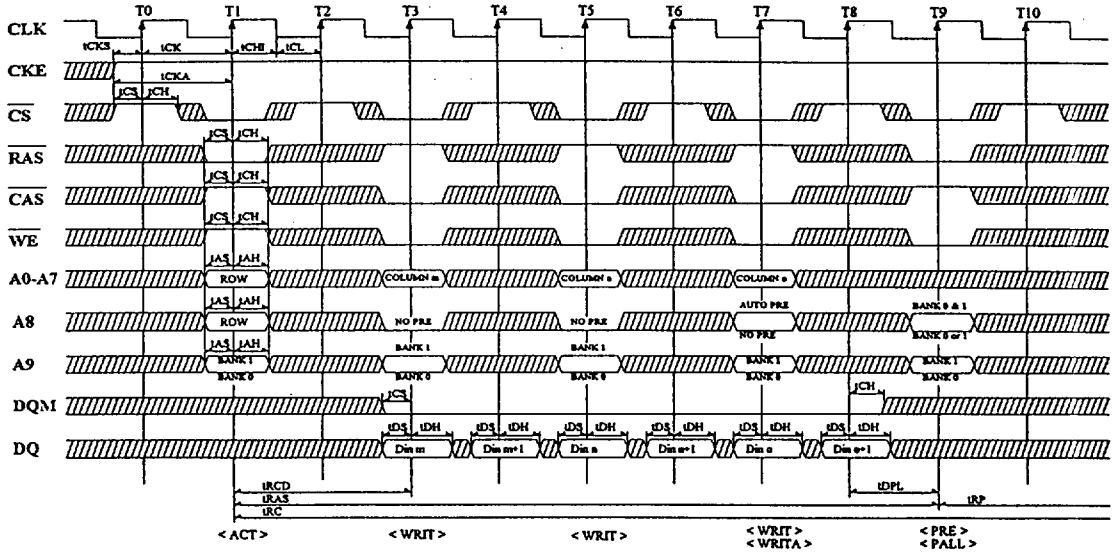


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

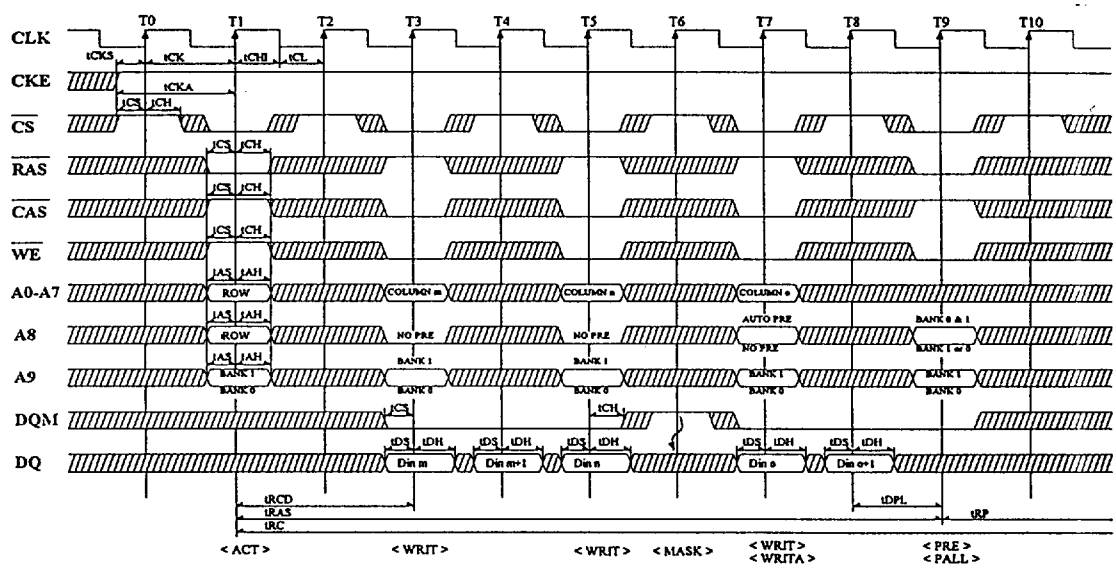
Write Cycle / Page Mode

$\overline{CAS}$ latency = 2 ,burst length = 2



Write Cycle / Page Mode ; Data Masking

$\overline{CAS}$ latency = 2 ,burst length = 2

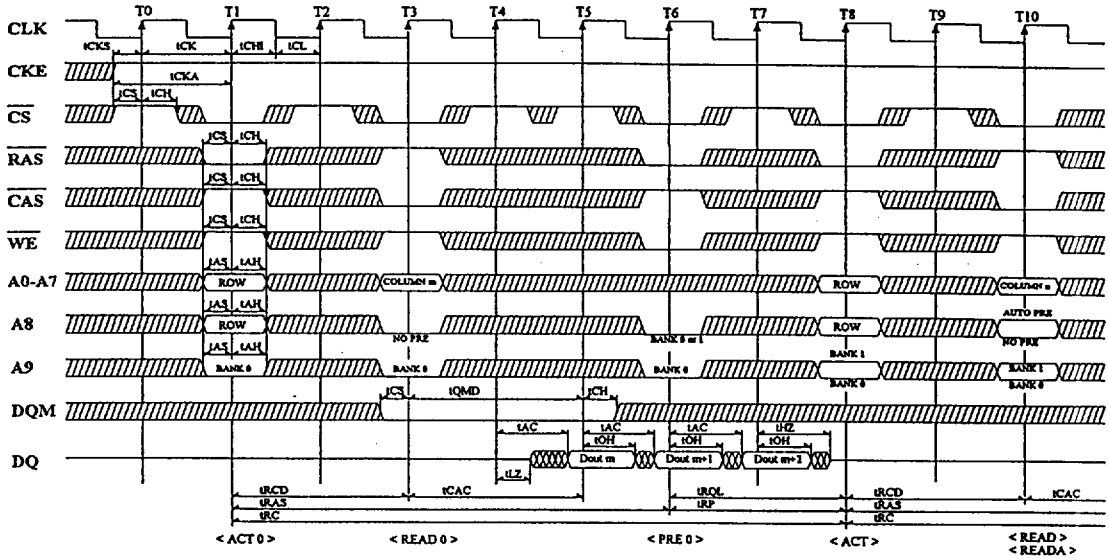


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

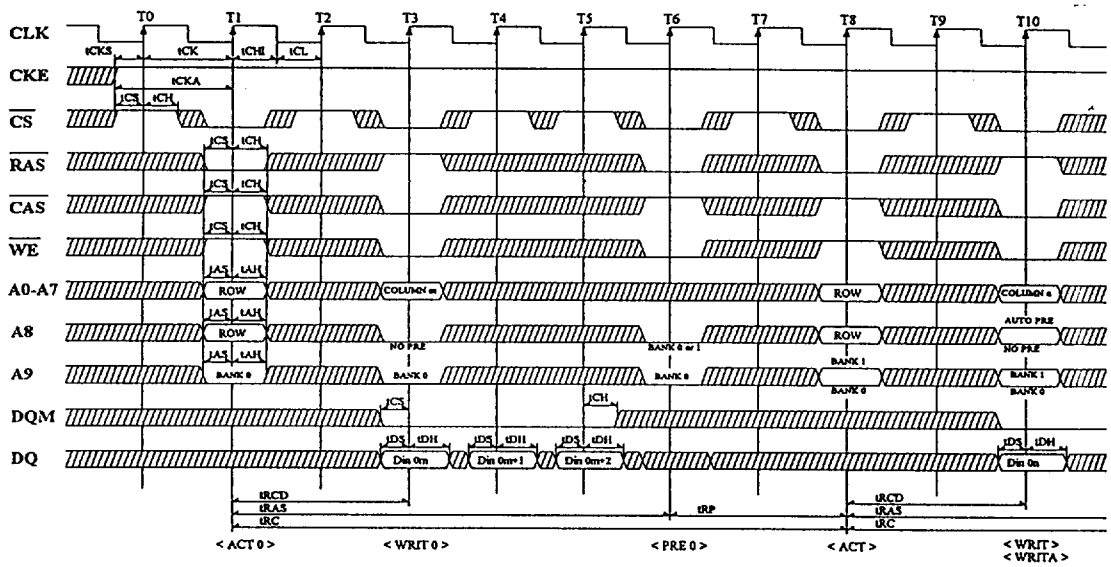
Read Cycle / Precharge Termination

$\overline{CAS}$ latency = 2 ,burst length = 4



Write Cycle / Precharge Termination

$\overline{CAS}$ latency = 2 ,burst length = 4

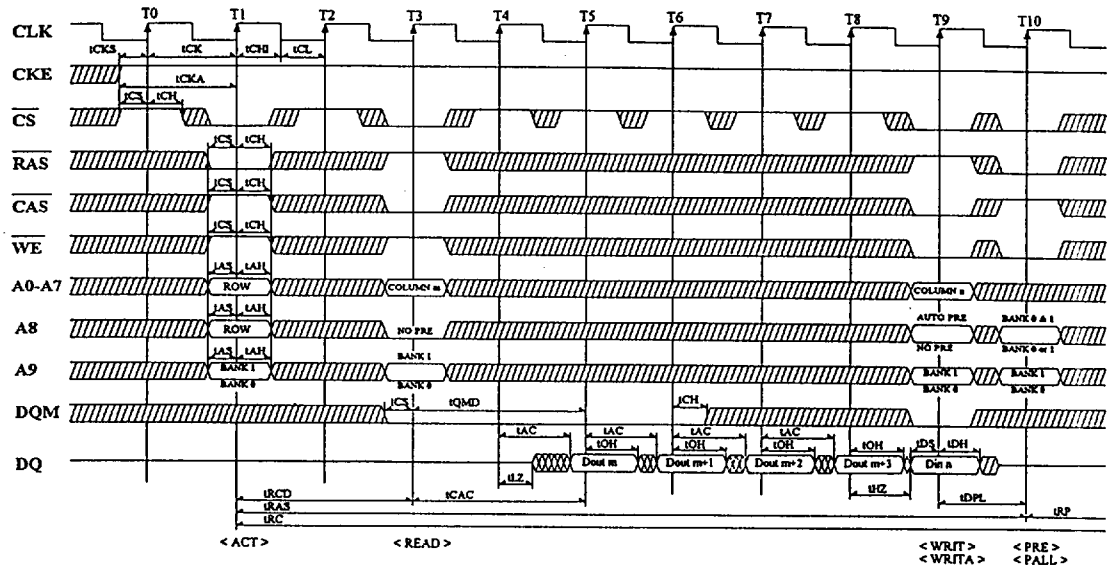


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

Read Cycle, Write Cycle / Burst Read, Single Write

$\overline{CAS}$ latency = 2 ,burst length = 4

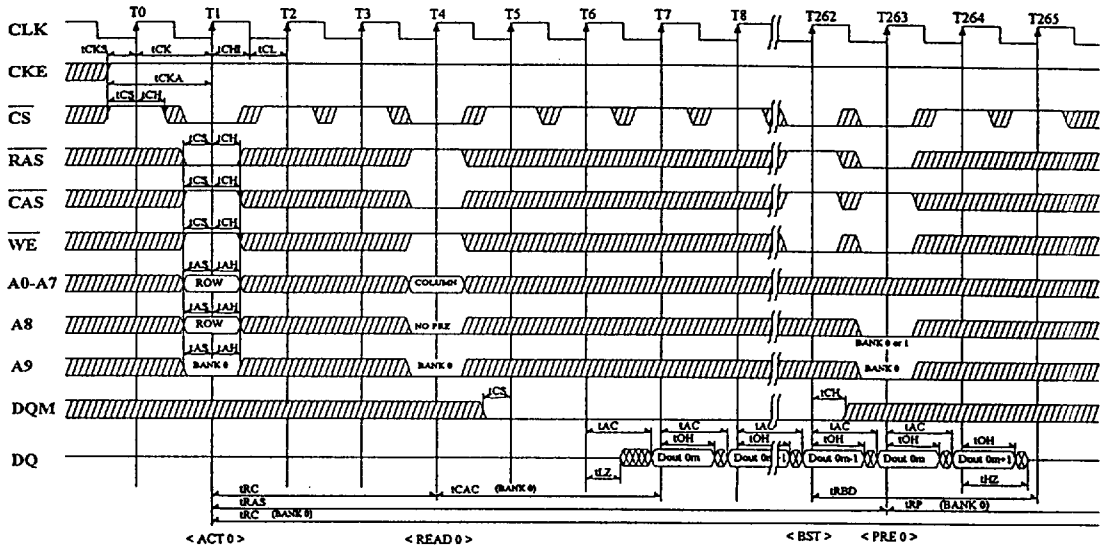


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

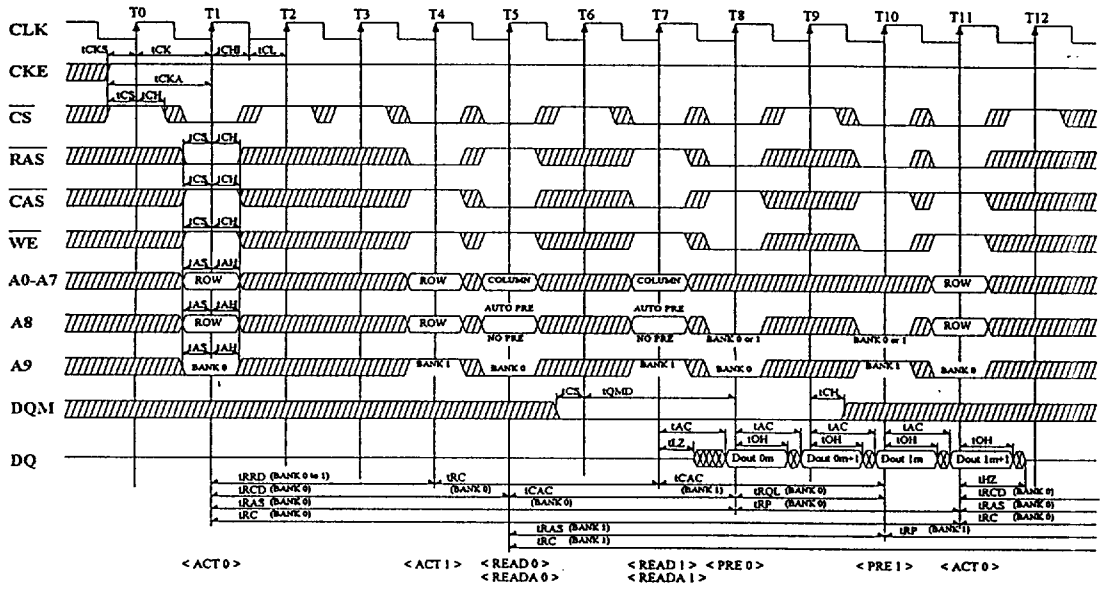
Read Cycle / Full Page

$\overline{CAS}$ latency = 3, burst length = Full Page



Read Cycle / Ping-Pong Operation (bank switching)

$\overline{CAS}$ latency = 3, burst length = 2

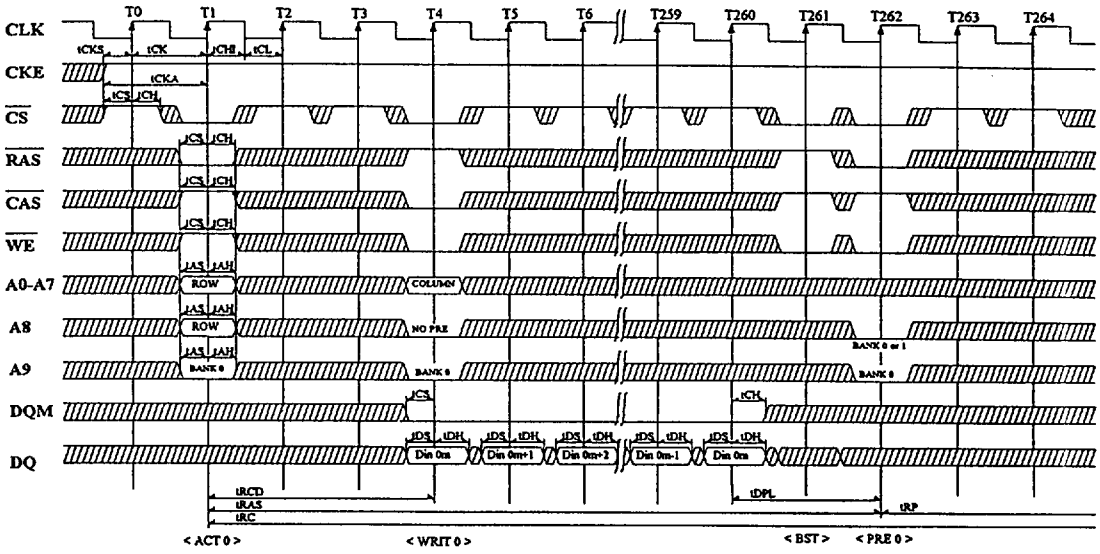


▨ DON'T CARE ▩ INVALID DATA

Note: The row address A7 is invalid during the active command input.

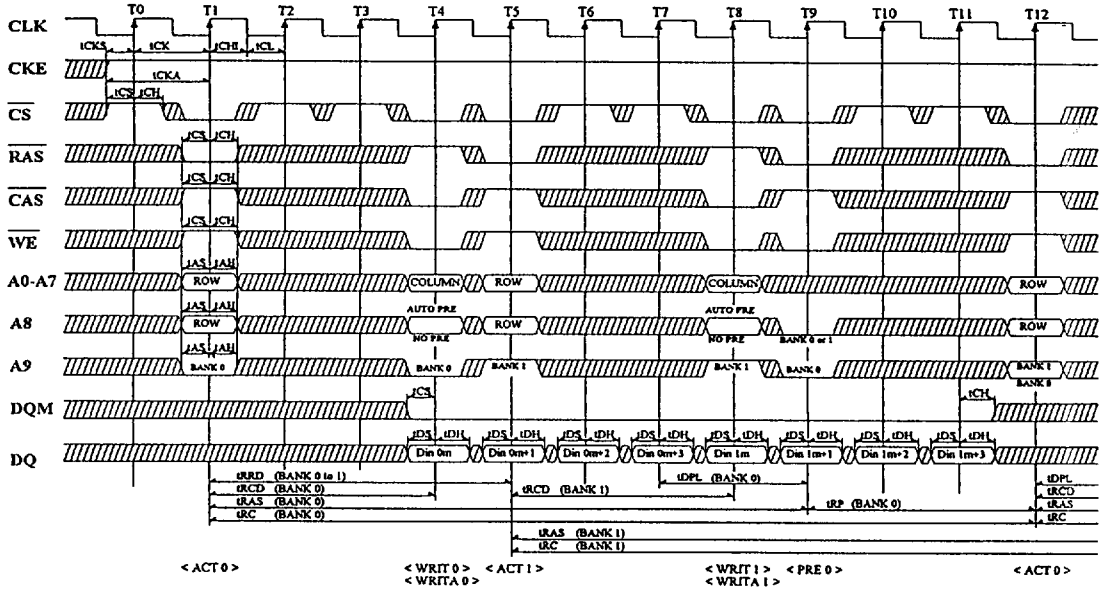
Write Cycle / Full Page

$\overline{CAS}$ latency = 3, bursth length = Full Page



Write Cycle / Ping-Pong Operation (bank switching)

$\overline{CAS}$ latency = 3, burst length =4

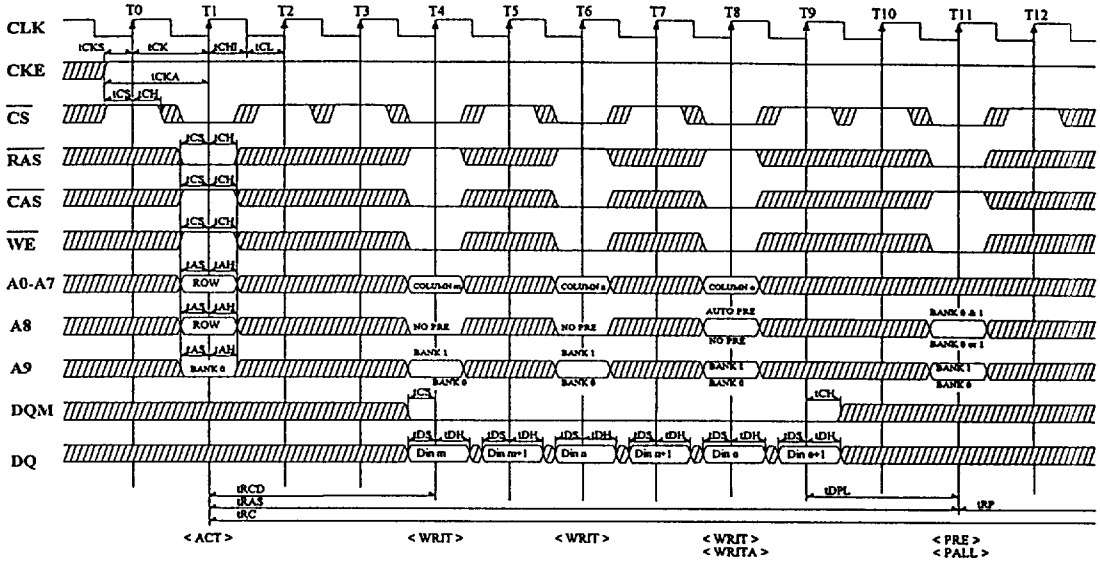


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

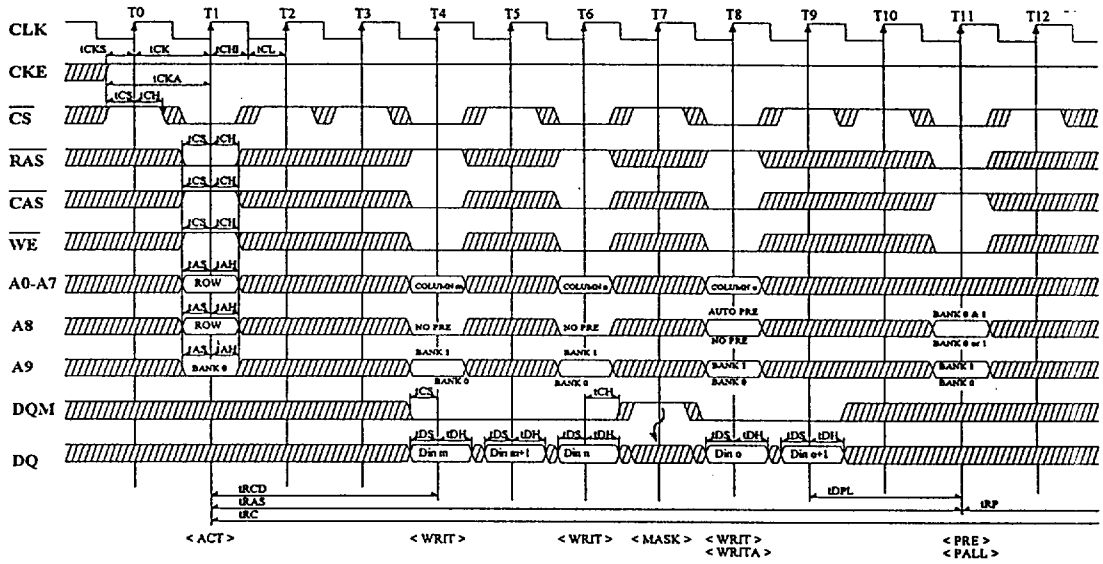
Write Cycle / Page Mode

$\overline{CAS}$ latency = 3, burst length =2



Write Cycle / Page Mode ; Data Masking

$\overline{CAS}$ latency =3, burst length = 2

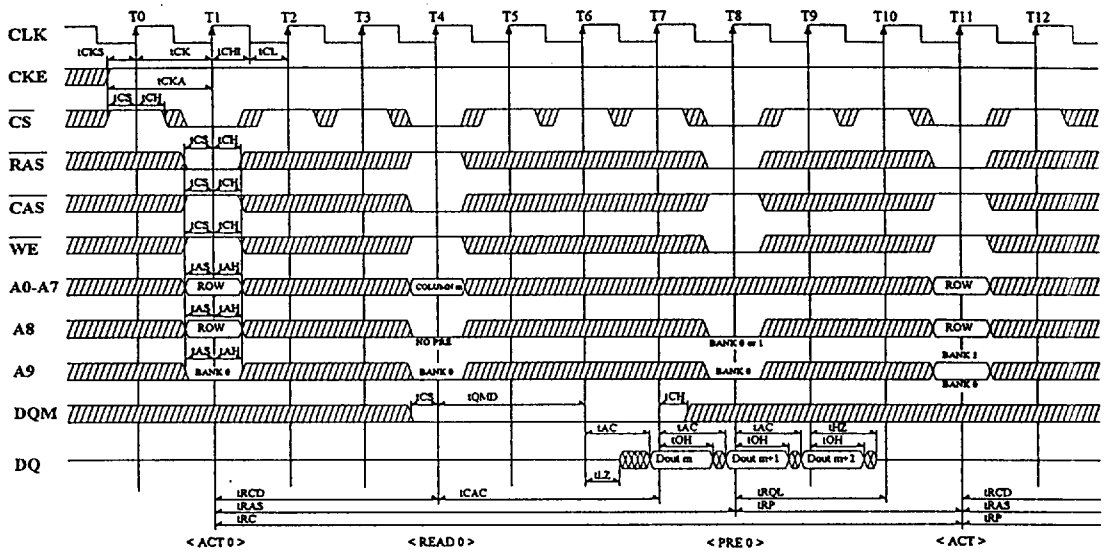


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

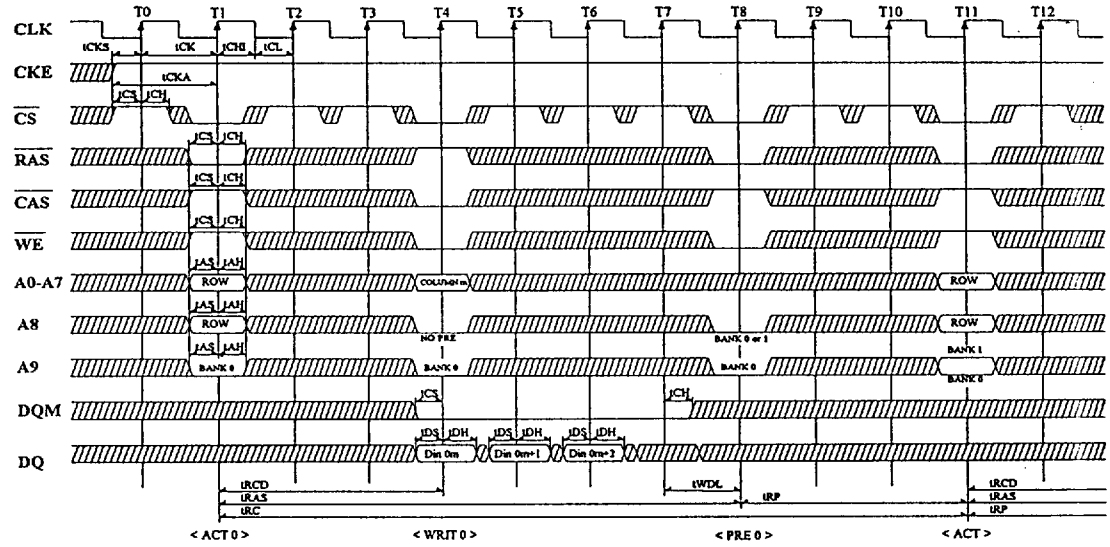
Read Cycle / Precharge Termination

$\overline{CAS}$ latency = 3, burst length =4



Write Cycle / Precharge Termination

$\overline{CAS}$ latency =3, burst length =4

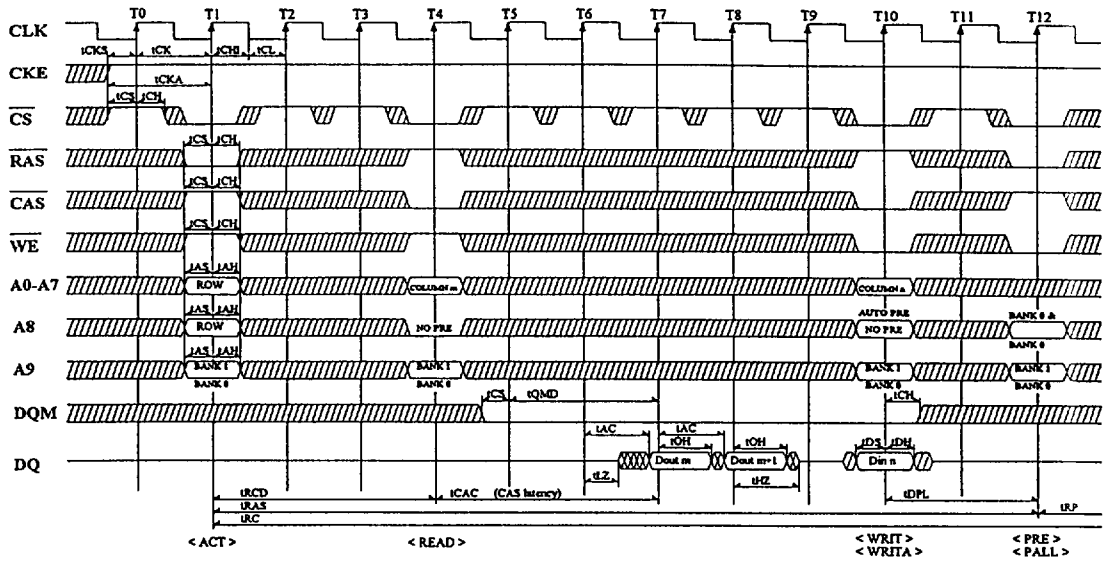


DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.

Read Cycle, Write Cycle / Burst Read, Single Write

$\overline{CAS}$ latency =3, burst length =2



DON'T CARE INVALID DATA

Note: The row address A7 is invalid during the active command input.