

PIC16C65A \rightarrow **PIC16C65B** Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences and the electrical specification differences that are present when migrating from one device to the next.

- Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.
- Note: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

Table 1 shows the considerations that must be taken into account when migrating from the PIC16C65A to the PIC16C65B.

Functional Differences due to Errata or Module Update											
No.	Module	Difference	H/W	S/W	Prog.						
1	ССР	CCP Special Event Trigger clears Timer1.	—	1	_						
2		Compare mode drives pin correctly.	_	1							
3	Timers	Reading or writing TMR1H or TMR1L may affect TMR1H or TMR1L unexpectedly.	_	1							
4		WDT/TMR0 prescaler assignment changes do not affect TMR0 count.	_	1							
5	SSP	TMR2 SPI™ clock synchronized to start of SPI Transmission.	_	1							
6		Can now transmit multiple words in SPI mode.		1	_						
7		Supports all four SPI modes. (Now uses SSP vs BSSP module.) See SSP module in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).	_	1							
8		$I^2 C^{TM}$ no longer generates ACK pulses when module is enabled.	—	1	—						
9	USART	Async receive errors due to BRGH setting corrected.		1	_						
10	Oscillator	TOST delay may be skipped when waking from SLEEP.		1	_						
11	RESET	Short $\overline{\text{MCLR}}$ pulses may cause improper operation on the PIC16C65B.	1	_							
12		Operating voltage and frequency ranges have been redefined.	1	_							
 H/W - Issues may exist with regard to the application circuits. S/W - Issues may exist with regard to the user program. Prog Issues may exist when writing the program to the controller. 											

TABLE 1: $PIC16C65A \rightarrow PIC16C65B DIFFERENCES$

Param		Characteristic		PIC16C65A			PIC16C65B			
No.	Symbol			Min	Тур†	Max	Min	Typ†	Мах	Unit
Core	·					•				
D001 D001A	Vdd	Supply Voltage XT, LP and RC mo HS mode BOR enabled (No	4.0 4.5 —		6.0 5.5 —	4.0 4.0 VBOR		5.5 5.5 5.5	V V V	
D005	VBOR	Brown-out Reset	3.7	4.0	4.3	3.65	—	4.35	V	
D150	Vod	Open Drain High V RA4		_	14.0	_	—	8.5	V	
SSP in S	SPI mode									
71	TscH	SCK input high	Continuous	TCY+20			1.25Tcy + 30	—		ns
71A		time (Slave mode)	Single Byte				40	_	_	ns
72	TscL	SCK input low	Continuous	TCY+20	_	—	1.25Tcy + 30	—	_	ns
72A		time (Slave mode)	Single Byte				40	—		ns
73	TdiV2scH TdiV2scL	Setup time of SDI data input to SCK edge		50	—	—	100	—	—	ns
73A (Note 2)	Тв2в	Last clock edge of Byte1 to the 1st clock edge of Byte2		—	—	—	1.5Tcy + 40	—	—	ns
74	TscH2diL TscL2diL	Hold time of SDI data input to SCK edge		50	_	—	100	—	_	ns
75	TdoR	SDO data output	PIC16CXX	_	10	25	_	10	25	ns
		rise time	PIC16LCXX				—	20	45	ns
78	TscR	SCK output rise	PIC16CXX		10	25	—	10	25	ns
		time (Master mode)	PIC16LCXX				—	20	45	ns
80	TscH2doV	SDO data output	PIC16CXX	_	_	50		—	50	ns
	TscL2doV	valid after SCK edge	PIC16LCXX				—		100	ns
83	TscH2ssH TscL2ssH	SS ↑ after SCK edge			_		1.5Tcy + 40	-	_	ns

TABLE 2: ELECTRICAL SPECIFICATION DIFFERENCES

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When BOR is enabled, the device will operate until VDD drops below VBOR.

2: Specification 73A is only required if specifications 71A and 72A are used.

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