SSI 32R528/528R
8 & 9-Channel Thin Film Read/Write Device
Preliminary Data

1

July, 1990

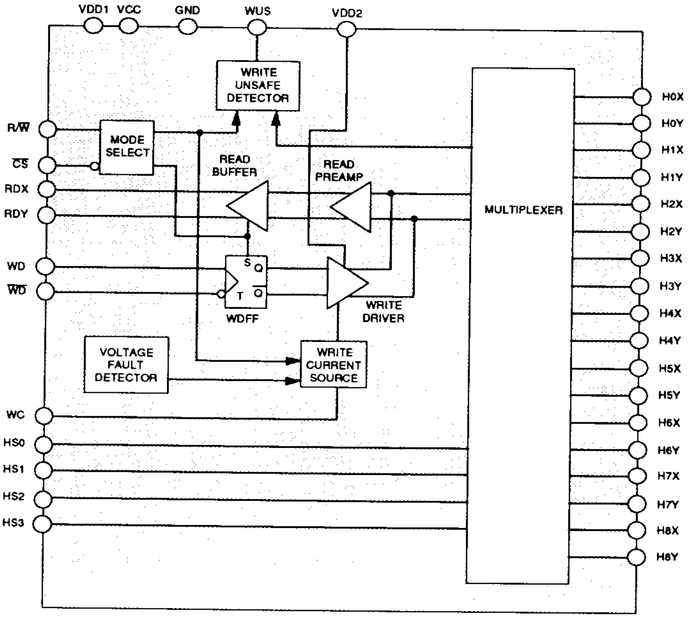
DESCRIPTION

The SSI 32R528/528R Read/Write devices are bipolar monolithic integrated circuits designed for use with two terminal thin film recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for eight or nine channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. They require +5V and +12V power supplies and are available in a variety of package configurations. The SSI 32R528R option provides internal 700Ω damping resistors.

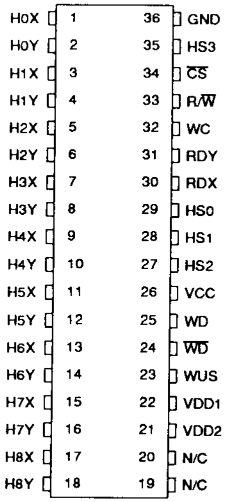
FEATURES

- **High performance:**
  - **Read mode gain = 150 V/V**
  - **Input noise = 0.85 nV/$\sqrt{Hz}$ max.**
  - **Input capacitance = 35 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Differential ECL-like Write Data input**
- **Power supply fault protection**
- **Compatible with two & three terminal TFH**
- **Write unsafe detection**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



36-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R528/528R
8 & 9-Channel Thin Film Read/Write Device

CIRCUIT OPERATION

The SSI 32R528 addresses up to nine two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R528 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each low to high transition of the WD, Write Data Input.

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, i.e. into the X-port.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{RWC}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. In multiple device applications, a single RWC resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

where:

Rh = head resistance + external wire resistance, and

Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on the WD/$\overline{WD}$ lines, after the fault is corrected, are required to clear the WUS flag.

- WD frequency too low
- Device not selected
- Head open
- Device in read mode
- No write current

Power dissipation in Write Mode may be reduced by placing a resistor, Rw, between VDD1 and VDD2. The resistor value should be chosen such that Iw Rw ≤ 3.0V for an accompanying reduction of $(Iw)^2$ Rw in power dissipation. If a resistor is not used, VDD2 should be connected to VDD1. Note that Rw will also provide current limiting in the event of a head short.

READ MODE

The read mode configures the SSI 32R528 as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained at the write mode value, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

0 = Low level 1 = High level

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
HS0 - HS3	I	Head Select: TTL level
$\overline{CS}$	I	Chip Select: a low TTL level enables the device
R/$\overline{W}$	I	Read/Write: a high TTL level selects Read mode
WUS	O*	Write Unsafe: Open collector output, a high level indicates an unsafe writing condition
WD, $\overline{WD}$	I	Differential Write Data inputs: a positive transition on WD toggles the direction of the head current
H0X - H8X H0Y - H8Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD1	-	+12V
VDD2	-	Positive Power Supply for Write current drivers
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may permanently damage the device.

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage		VDD1, 2	-0.3 to +14	VDC
		VCC	-0.3 to +7	VDC
Write Current		Iw	100	mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3	VDC
Head Port Voltage		VH	-0.3 to VDD2 +0.3	VDC
WUS Pin Voltage Range		Vwus	-0.3 to +14	VDC
Output Current	RDX, RDY	Io	-10	mA
	WUS	Iwus	+12	mA
Storage Temperature		Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD1	12 ± 10%	VDC
	VDD2	VDD1 - 3.0 to VDD1	VDC
	VCC	5 ± 10%	VDC
Operating Temperature	Tj	0 to +135	°C

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD1 Supply Current	Read Mode	-	-	42	mA
	Write Mode	-	-	50	mA
	Idle Mode	-	-	22	mA
VDD2 Supply Current	Read Mode	-	-	200	µA
	Write Mode	-	-	Iw + 0.4	mA
	Idle Mode	-	-	200	µA
VCC Supply Current	Read Mode	-	-	68	mA
	Write Mode	-	-	48	mA
	Idle Mode	-	-	55	mA
Power Dissipation (Tj = +135°C)	Read Mode	-	-	850	mW
	Write Mode: Iw = 20 mA, VDD2 = VDD1	-	-	1100	mW
	Write Mode: Iw = 40 mA, VDD1 - VDD2 = 3.0V	-	-	1200	mW
	Idle Mode	-	-	550	mW
WD, $\overline{WD}$ Input Low Current (IIL1)	VIL1 = VCC -1.625V			80	µA
WD, $\overline{WD}$ Input High Current (IIH1)	VIH1 = VCC -0.72V			100	µA
WD, $\overline{WD}$ Input Low Voltage (VIL1)		VCC -1.870		VCC -1.625	VDC
WD, $\overline{WD}$ Input High Voltage (VIH1)		VCC -1.00		VCC -0.720	VDC
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Current (IIL2)	VIL2 = 0.8V	-0.4			mA
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Current (IIH2)	VIH2 = 2.0V			100	µA
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Voltage (VIL2)				0.8	VDC
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Voltage (VIH2)		2.0			VDC

DC CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
WUS Output Low Voltage (VOL)	ILUS = 8.0 mA			0.5	VDC
VDD Fault Voltage		8.5	-	10.0	VDC
VCC Fault Voltage		3.5	-	4.2	VDC
Head Current (HnX, HnY)	Write Mode, 0 ≤ VCC ≤ 3.5V 0 ≤ VDD1 ≤ 8.5V	-200	-	+200	µA
	Read/Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200	-	+200	µA

WRITE CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and f(WD) = 5 MHz.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
WC Pin Voltage (Vwc)		-	1.65 ±5%	-	V
Differential Head Voltage Swing		7	-	-	Vpp
Unselected Head Current		-	-	1	mA(pk)
Differential Output Capacitance		-	-	25	pF
Differential Output Resistance	32R528R	500	700	950	Ω
	32R528	4	-	-	kΩ
WD Transition Frequency	WUS = low	1.7	-	-	MHz
Write Current Range	0 - pk	10	-	40	mA

READ CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20 pF and RL (RDX,RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin = 1 mVpp @ 1 MHz	125	-	175	V/V
Bandwidth	-1dB	|Zs| < 5Ω, Vin=1 mVpp	25	-	-	MHz
	-3dB	|Zs| < 5Ω, Vin=1 mVpp	45	-	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	0.62	0.85	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	-	35	pF
Differential Input Resistance	32R528R	Vin = 1 mVpp, f = 5 MHz	300	-	-	Ω
	32R528	Vin = 1 mVpp, f = 5 MHz	640	-	-	Ω
Dynamic Range		Peak-to-peak ac input voltage where gain falls to 90% of its small signal value, f = 5 MHz	6	-	-	mVpp

READ CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Common Mode Rejection Ratio	Vin = 0 VDC+100 mVpp @ 5 MHz	54	-	-	dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1 100 mVpp @ 5 MHz on VCC	54	-	-	dB
Channel Separation	Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	-	dB
Output Offset Voltage		-360	-	+360	mV
RDX, RDY Common Mode Output Voltage	Read Mode	2.2	2.9	3.6	VDC
	Write Mode	-	2.9	-	VDC
Single Ended Output Resistance	f = 5 MHz	-	-	40	Ω
Output Current	AC Coupled Load, RDX to RDY	3.2	-	-	mA

SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 μH, Rh = 30Ω and f(WD) = 5 MHz.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	μs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100 mV 10 MHz Read signal envelope or to 90% decay of write current	-	0.6	μs
$\overline{CS}$				
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100 mV 10 MHz Read signal envelope	-	0.6	μs
$\overline{CS}$ to Unselect	Delay to 10% of write current	-	0.6	μs
HSn				
HS0, 1, 2, 3 to any Head	Delay to 90% of 100 mV 10 MHz Read signal envelope	-	0.4	μs
WUS				
Safe to Unsafe - TD1		0.6	3.6	μs
Unsafe to Safe - TD2		-	1	μs
Head Current				
Prop. Delay - TD3	From 50% points, Lh=0μh, Rh=0Ω	-	32	ns
Asymmetry	WD has 50% duty cycle and 1ns rise/fall time, Lh=0μh, Rh=0Ω	-	1	ns
Rise/Fall Time	10% - 90% points, Lh=0μh, Rh=0Ω	-	9	ns

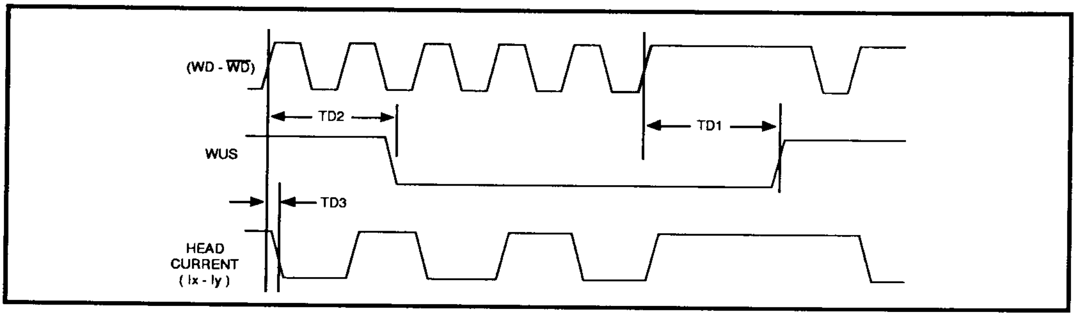


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: Key Parameters Under Worst Case Input Noise Conditions

PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.70	0.85	nV/√Hz
Differential Input Resistance (Min.)	32R528R	390	420	Ω
	32R528	1200	1500	Ω
Differential Input Capacitance (Max.)		32	34	pF

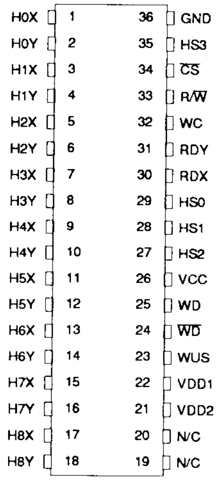
TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions

PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.58	0.71	nV/√Hz
Differential Input Resistance (Min.)	32R528R	310	350	Ω
	32R528	643	846	Ω
Differential Input Capacitance (Max.)		33	35	pF

SSI 32R528/528R
8 & 9-Channel Thin Film Read/Write Device

PACKAGE PIN DESIGNATIONS

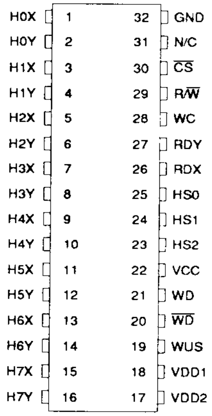
(Top View)



36-Lead SOM

THERMAL CHARACTERISTICS: Øja

32-Lead SOW	55°C/W
36-Lead SOM	50°C/W



32-Lead SOW, FLATPACK

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R528 Read/Write IC		
8-Channel SOW	SSI 32R528-8W	32R528-8W
9-Channel SOM	SSI 32R528-9M	32R528-9M
SSI 32R528R with Internal Damping Resistor		
8-Channel SOW	SSI 32R528R-8W	32R528R-8W
9-Channel SOM	SSI 32R528R-9M	32R528R-9M

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.