NEC

MOS INTEGRATED CIRCUIT
μPD45125421, 45125821, 45125161

128M-BIT VirtualChannel™ SDRAM

Description

The 128M-bit VirtualChannel (VC) SDRAM is implemented to be 100% pin and package compatible to the industry standard SDRAM. It uses the same command protocol and interface as SDRAM. The VirtualChannel SDRAM command set is a superset of the SDRAM. It also follows the same electrical and timing specifications of the SDRAM, such that it is possible for one product platform to be used with the VirtualChannel SDRAM and non-VirtualChannel SDRAM part.

Features

- Fully Standard Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Dual internal banks controlled by Bank Select Address
- Sixteen Channels controlled by Channel Select Address
- Quad segments controlled by Segment Select Address
- Byte control (x16) by LDQM and UDQM
- Programmable Wrap sequence (Sequential / Interleave)
- Programmable burst length (1, 2, 4, 8 and 16)
- Read latency (1, 2)
- ★ Prefetch Read latency (2, 4) : For x4 bits organization(μPD45125421), prefetch read operation can not be used.
- Auto precharge and without auto precharge
- Auto refresh and Self refresh
- x4, x8, x16 organization
- Single 3.3 V ± 0.3 V power supply
- Interface: LVTTL
- Refresh cycle: 4 K cycles / 64 ms

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The mark ★ shows major revised points.

★ **Ordering Information (Under development)**

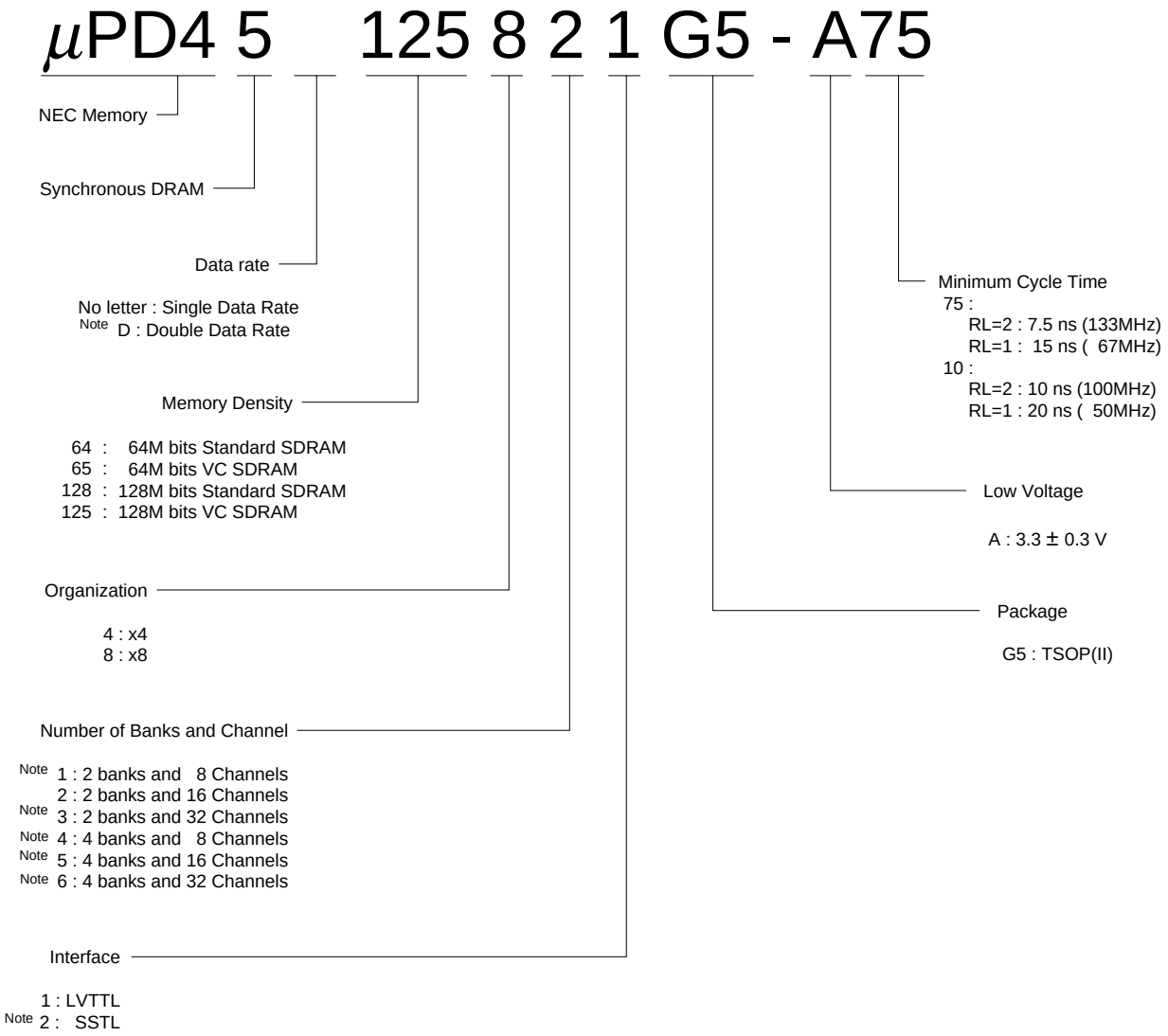
Part number	Organization (word x bit x bank)	Clock frequency MHz (MAX.)	Read latency	Prefetch Read Latency	Channel and Interface	Package
μPD45125421G5-A75-9JF	16M x 4 x 2	133	2	–[Note1]	16 channels and LVTTL	54-pin Plastic TSOP(II) (10.16mm (400))
		67	1[Note2]	–[Note1]		
μPD45125421G5-A10-9JF		100	2	–[Note1]		
		50	1[Note2]	–[Note1]		
μPD45125821G5-A75-9JF	8M x 8 x 2	133	2	4		
		67	1[Note2]	2		
μPD45125821G5-A10-9JF		100	2	4		
		50	1[Note2]	2		
μPD45125161G5-A75-9JF	4M x 16 x 2	133	2	4		
		67	1[Note2]	2		
μPD45125161G5-A10-9JF		100	2	4		
		50	1[Note2]	2		

Notes 1. For x4 bits organization, prefetch read operation can not be used.

2. Under development.

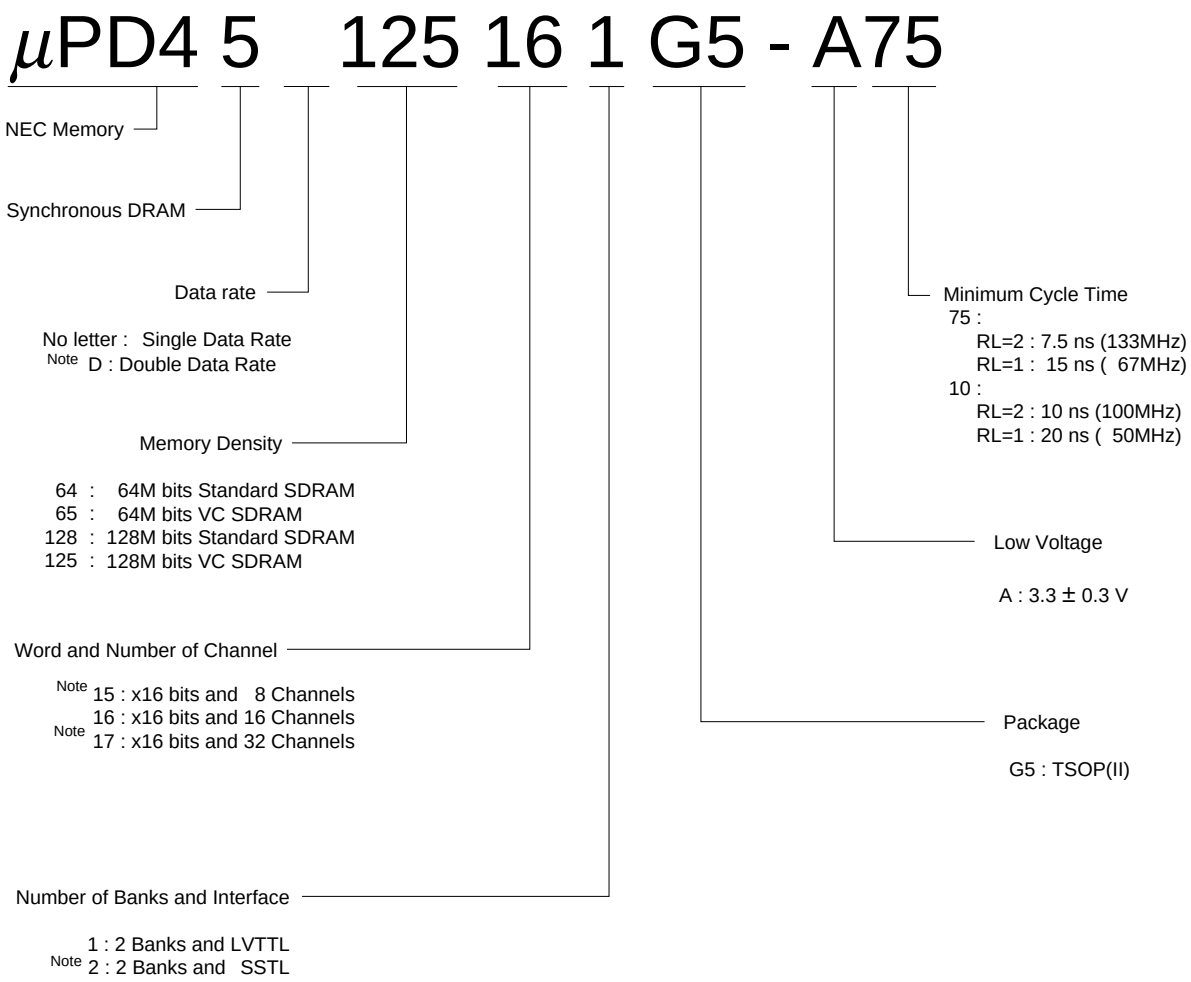
Part Number

★ [x4, x8]



Note Reserved

★ [x16]



Note Reserved

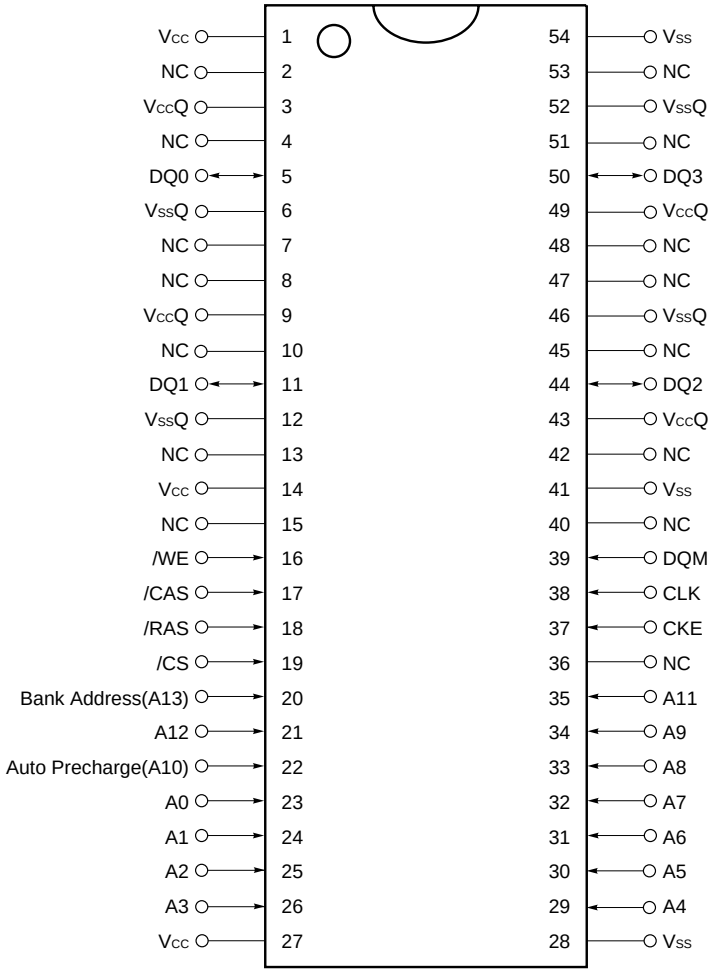
Pin Configurations

/xxx indicates active low signal.

[μPD45125421]

54-pin Plastic TSOP (II) (10.16mm (400))

16M words x 4 bits x 2 banks



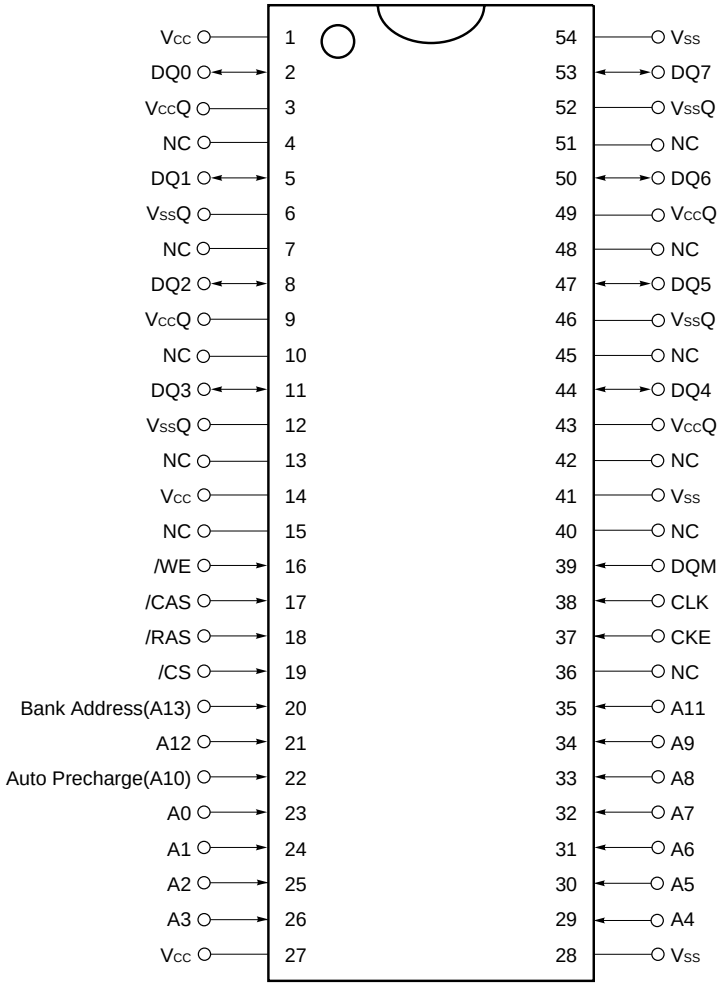
A0 - A13	:	Address inputs	DQM	:	DQ mask enable
A0 - A12	:	Row address inputs	CKE	:	Clock enable
A0 - A7, A10	:	Column address inputs	CLK	:	System clock input
DQ0 - DQ3	:	Data inputs/outputs	VCC	:	Supply voltage
/CS	:	Chip select	VSS	:	Ground
/RAS	:	Row address strobe	VCCQ	:	Supply voltage for DQ
/CAS	:	Column address strobe	VSSQ	:	Ground for DQ
/WE	:	Write enable	NC	:	No connection

Remark Refer to **1. Input/ Output Pin Function** for Bank address, Channel address and Segment address.

[μPD45125821]

54-pin Plastic TSOP (II) (10.16mm (400))

8M words x 8 bits x 2 banks



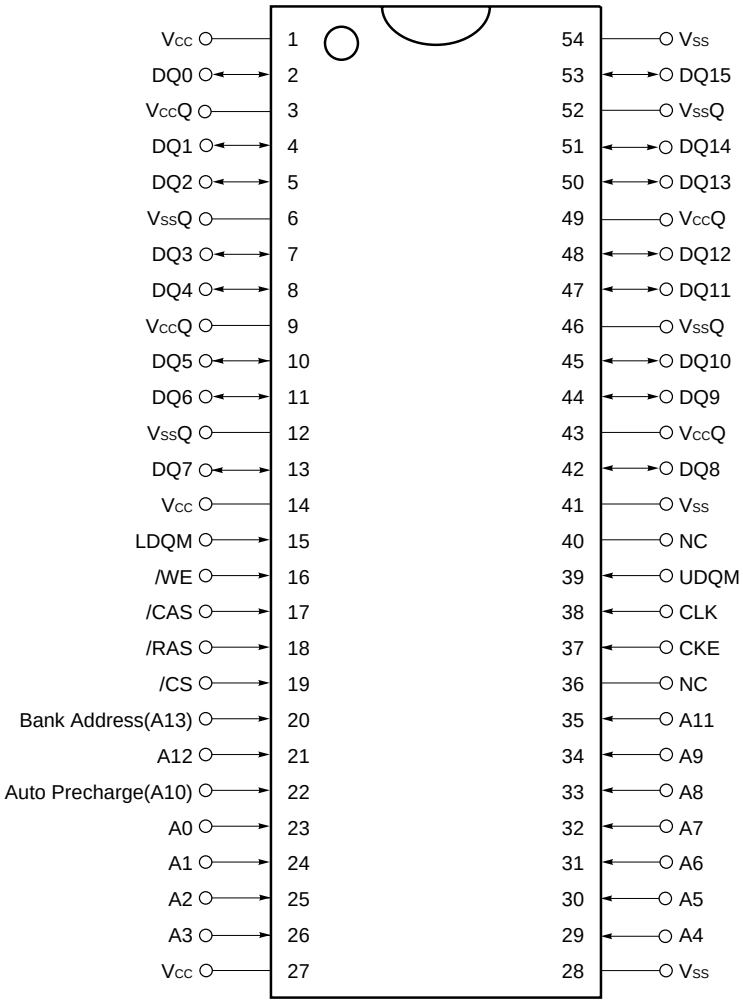
A0 - A13	:	Address inputs	DQM	:	DQ mask enable
A0 - A12	:	Row address inputs	CKE	:	Clock enable
A0 - A7	:	Column address inputs	CLK	:	System clock input
DQ0 - DQ7	:	Data inputs/outputs	VCC	:	Supply voltage
/CS	:	Chip select	VSS	:	Ground
/RAS	:	Row address strobe	VCCQ	:	Supply voltage for DQ
/CAS	:	Column address strobe	VSSQ	:	Ground for DQ
/WE	:	Write enable	NC	:	No connection

Remark Refer to **1. Input/ Output Pin Function** for Bank address, Channel address and Segment address.

[μPD45125161]

54-pin Plastic TSOP (II) (10.16mm (400))

4M words x 16 bits x 2 banks



A0 - A13	:	Address inputs	UDQM	:	Upper DQ mask enable
A0 - A12	:	Row address inputs	LDQM	:	Lower DQ mask enable
A0 - A6	:	Column address inputs	CKE	:	Clock enable
DQ0 - DQ15	:	Data inputs/outputs	CLK	:	System clock input
/CS	:	Chip select	VCC	:	Supply voltage
/RAS	:	Row address strobe	VSS	:	Ground
/CAS	:	Column address strobe	VCCQ	:	Supply voltage for DQ
/WE	:	Write enable	VSSQ	:	Ground for DQ
			NC	:	No connection

Remark Refer to **1. Input/ Output Pin Function** for Bank address, Channel address and Segment address.

VCMemory™ Architecture

The VCMemory is a memory core technology designed to improve memory data throughput efficiency and initial latency of memories. Intended for use in next generation memory systems, the VCMemory technology is ideal memory for a wide range of application such as Multimedia PC, Game machine, Internet Server etc…. The slow core operation memory such as DRAM, Flash Memory and Mask ROM can get very significant performance improvements with VCMemory technology.

Today's memory subsystems are accessed by multiple tasks/sources (memory masters), working in multitasking mode. Each memory master accesses memory with an address locality with a time locality, a block size and a number of contiguous accesses. VCMemory architecture is designed for this multitasking, multiple masters, interleaving access scenarios. The VCMemory provides memory masters with VirtualChannels. Each channel is a set of resources that constitute a fast dedicated path for each memory masters to access the memory. The VirtualChannels will minimize the overhead resulting from other memory master's accesses, reduce the access latency and facilitate automatic data sharing.

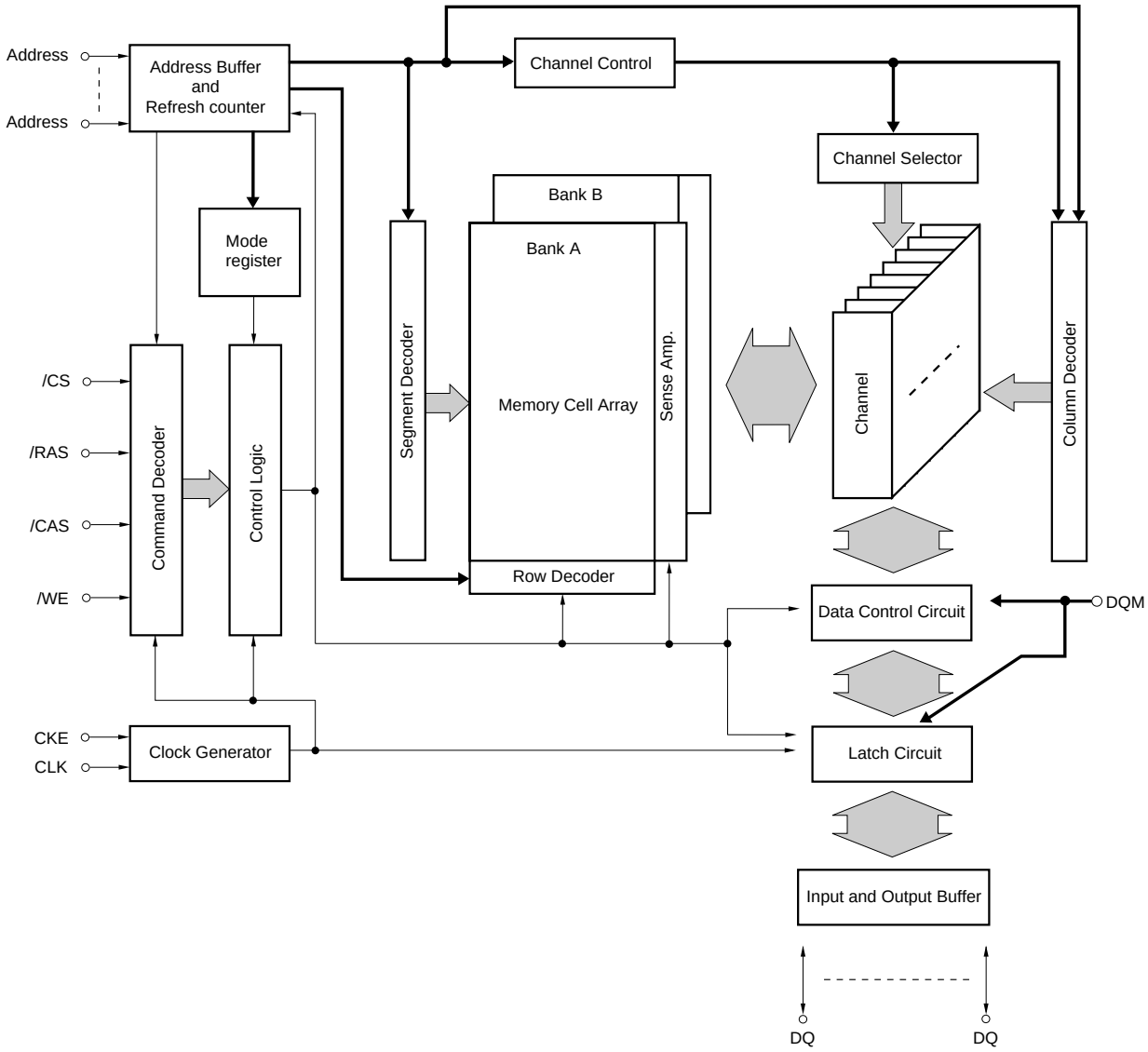
Each channel is equipped with a data row buffer and its own independent operating modes. To the memory masters, this looks like its own very fast memory. The system memory controller associates these channels to the memory masters for their accesses. Thus, the channels are made to track the accesses of these memory masters. The system memory controller has complete controls over the operations of the channels. It can schedule and issue commands that causes segments of memory rows to be loaded into the channels or for data from the channels to be written back to the memory rows. Any channels can store the data from any rows, can be written to any rows and hence are fully associative. Then the Read and Write operations will be occurring as much as possible with these high speed channels, minimizing all overheads associated with the DRAM bank operations.

The Read/Write operations of the channels (foreground operations) can operate independently with the DRAM bank operations (background operations) of Activate, Precharge, Prefetch (Loading row data to channel) and Restore (Writing channel data to row). Then VCMemory also further enhances performance by allowing the system memory controller to schedule the foreground and background operations to operate concurrently.

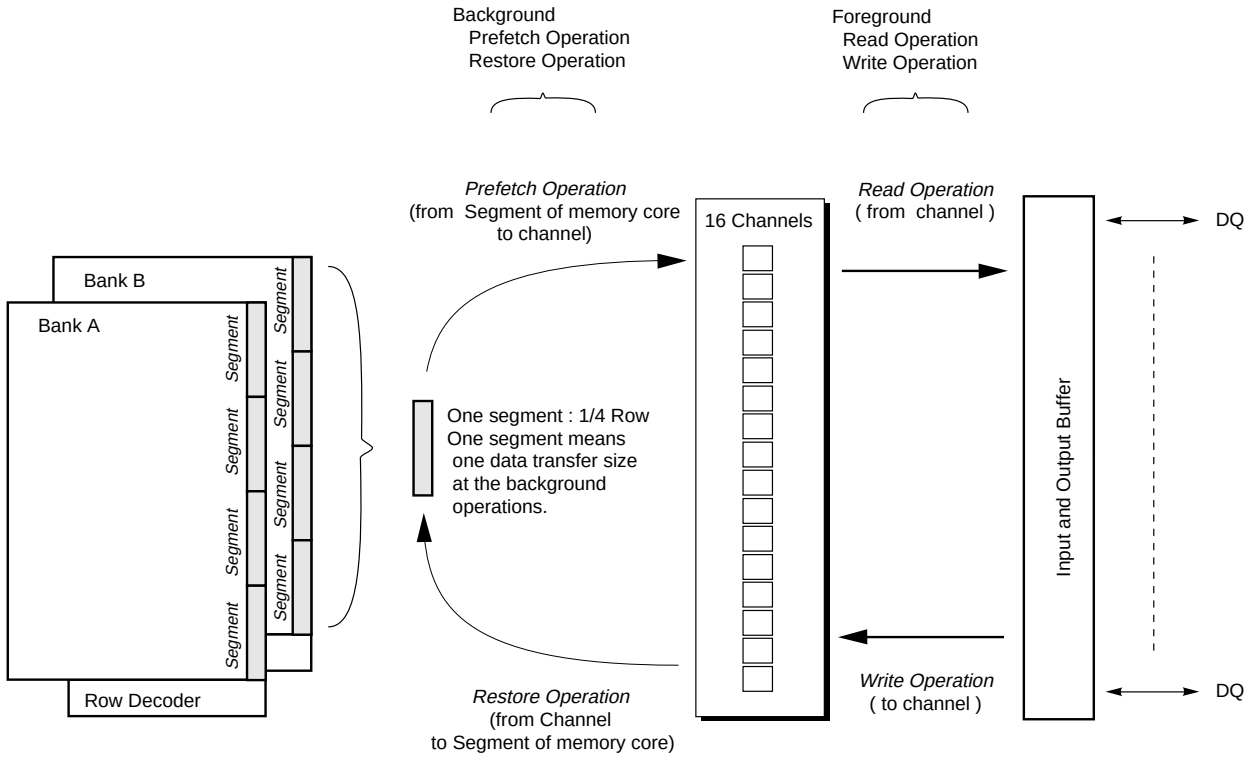
VirtualChannel SDRAM architecture offers the following features and benefits:

1. Multiplies the effective data throughput performance of conventional DRAM core.
2. Achieving close to full data bus bandwidth with low latency, interleaved random row, random column Read/Write through the channels.
3. Transparent DRAM bank operations through the concurrent foreground and Background Operations
4. Very wide (256 bytes wide) internal data transfer bus between Channel and memory core
5. Equivalence of tens of multiple memory banks by using only a fraction of the frequency of Row Activate and Precharge of conventional DRAM core.

Block Diagram



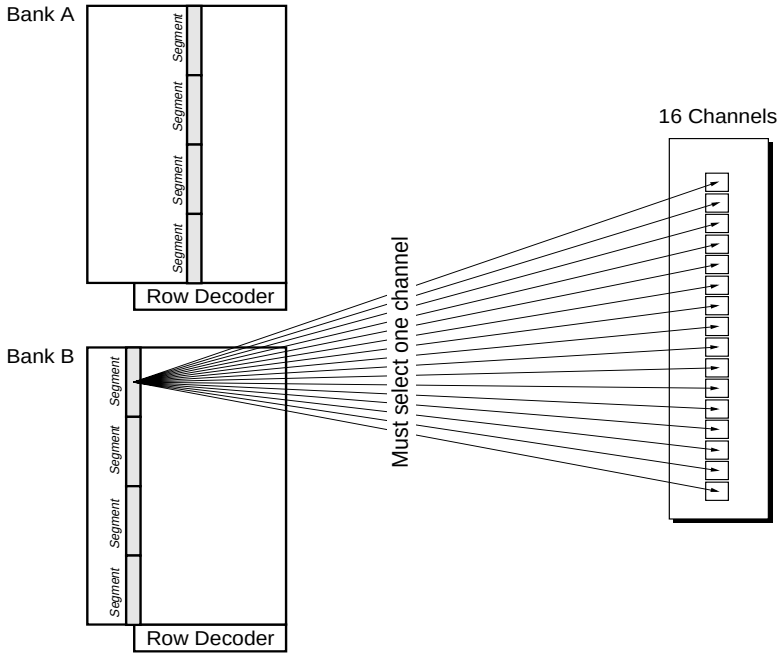
Conceptual Schematic 1



Conceptual Schematic 2

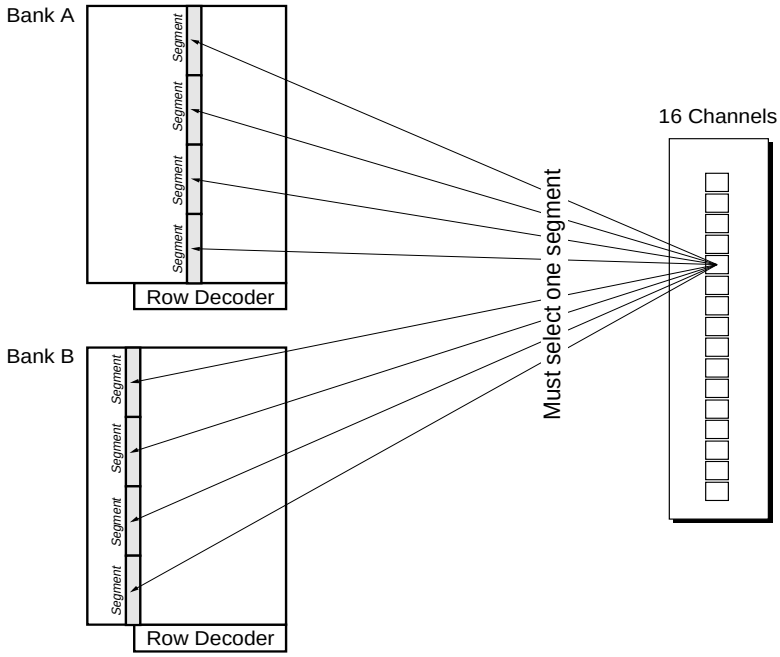
Prefetch Operation

The data is fetched from a segment to any channel buffer.

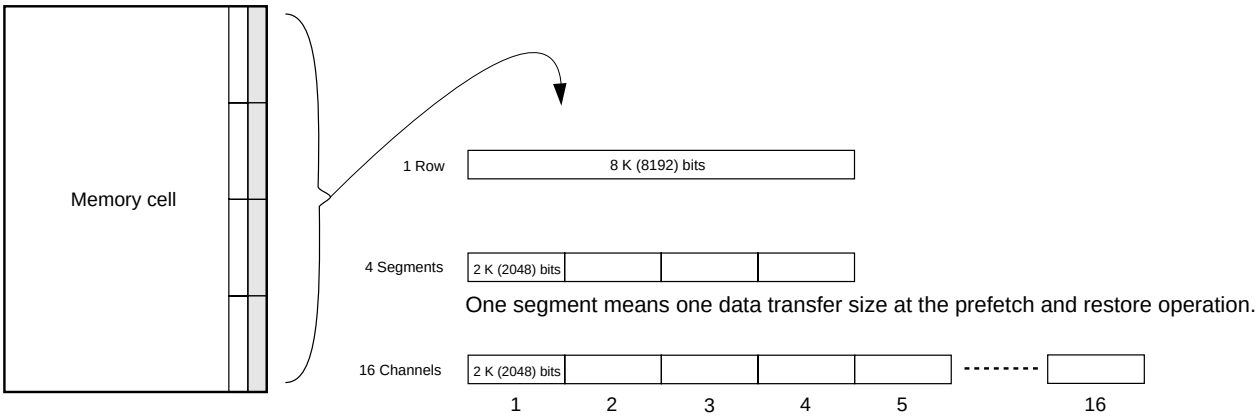


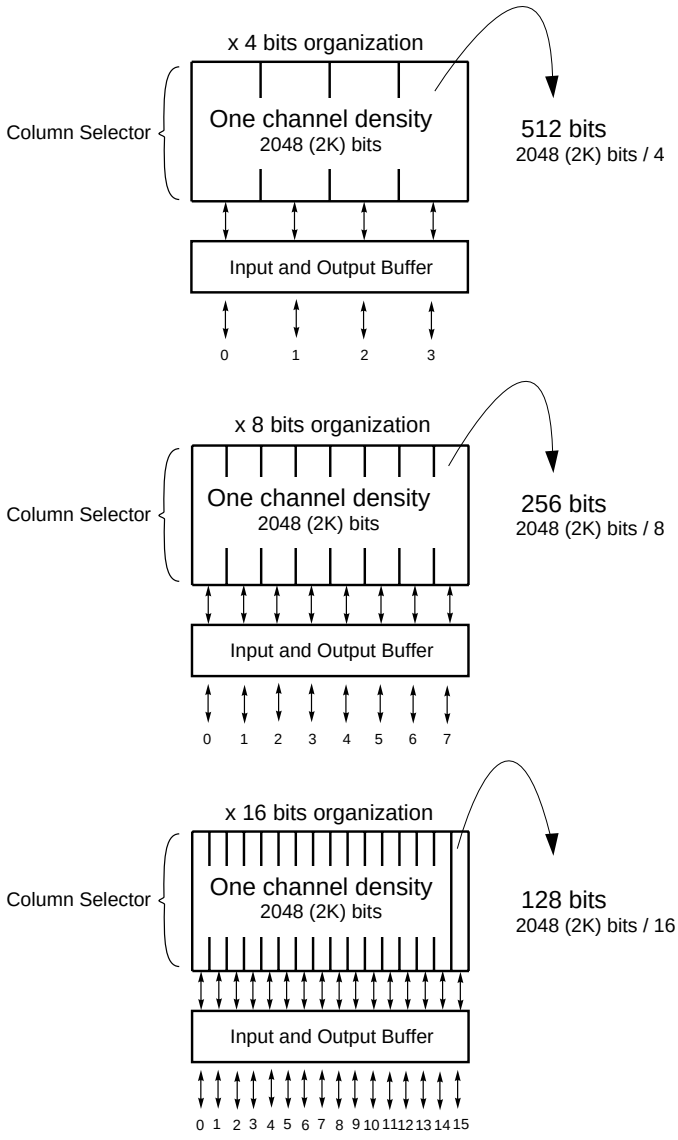
Restore Operation

The data is transferred from a channel buffer to any segment.



Data size of segment and channel





1. Input/Output Pin Function

(1/3)

Pin name	Input/Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals for all commands are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the VirtualChannel SDRAM suspends operation. When the VirtualChannel SDRAM is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.
/CS	Input	Chip select. /CS low starts the command input cycle, which occurs on rising edge of CLK. During /CS high, commands are ignored but operations continue.
/RAS, /CAS, /WE	Input	Command Inputs. The combination of these signals defines the command being entered. For details, refer to the Command Table in Command Functions. The symbol names (/RAS, /CAS, /WE) do not refer to the functional meanings used for conventional DRAM.
DQM For x8,x4 devices UDQM LDQM For x16 device	Input	For x4, x8 devices DQM controls I/O buffers. For x16 device UDQM and LDQM control upper byte and lower byte I/O buffers, respectively. **In read mode** DQM controls the output buffers like a conventional /OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. **In write mode** DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ3 DQ0 - DQ7 DQ0 - DQ15	Input/Output	DQ pins have the same function as I/O pins on a Standard Synchronous DRAM. DQ0 - DQ3 (for x 4 device) DQ0 - DQ7 (for x 8 device) DQ0 - DQ15 (for x 16 device)
NC	−	No connect. Leave these pins unconnected.
V_{CC} V_{SS}	(Power supply)	V_{CC} and V_{SS} are power supply pins for internal circuits.
$V_{CC}Q$ $V_{SS}Q$	(Power supply)	$V_{CC}Q$ and $V_{SS}Q$ are power supply pins for the output buffers.

(2/3)

Pin name	Input/Output	Function
A0 - A13	Input	Address specification. These pins provide memory source and target addresses (bank, row, column, etc.), and channel addresses. **Row Address** Row Address is determined by A0 - A12 at the CLK (clock) rising edge in the active command cycle. It does not depend on the bit organization. **Column Address** Column Address is determined by A0 - A7 and A10 at the CLK rising edge in the read or write command cycle. It depends on the bit organization. : A0 - A7, A10 for x4 device : A0 - A7 for x8 device : A0 - A6 for x16 device. **Bank Address(A13)** A13 is the bank select signal. In command cycle, A13 low select bank A, and A13 high select bank B.

(3/3)

<table>
<tr><th>Pin name</th><th>Input/Output</th><th>Function</th></tr>
<tr><td>A0 - A13</td><td>Input</td><td>
Channel Address(A8, A9, A10, A11, A12)
A8, A9, A11, A12 are the channel select signals.
In prefetch, restore, read and write operations, channel is determined by A8, A9, A11 and A12.
<table>
<tr><th>Channel number</th><th>A12</th><th>A11</th><th>A9</th><th>A8</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>5</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>7</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>9</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>10</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>11</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>12</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>13</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>14</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>15</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
In set register operation, channel is determined by A9, A10, A11 and A12.
<table>
<tr><th>Channel number</th><th>A12</th><th>A11</th><th>A10</th><th>A9</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>5</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>7</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>9</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>10</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>11</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>12</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>13</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>14</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>15</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Segment Address(A0, A1, A10, A13)
A0, A1, A10, A13 are the segment select signals.
In prefetch and restore operations, column address in channel is determined by A0, A1.
In prefetch read operation, segment is determined by A10, A13.

Auto precharge Address(A10)
A10 defines the precharge mode.

In the precharge command cycle
High level: All banks are precharged.
Low level: Only the bank selected by A13 is precharged.

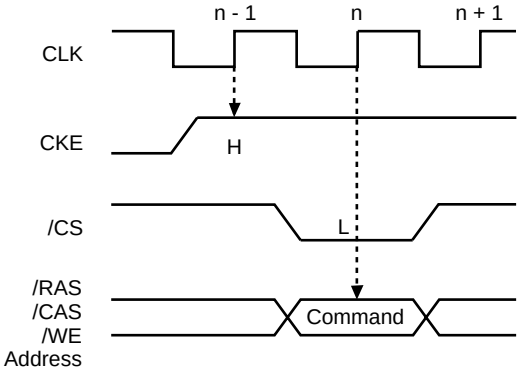
In the prefetch or restore command cycle
High level: Auto precharge
Low level: Without auto precharge
</td></tr>
</table>

2. Truth Table

2.1 Command Execution

All commands are executed with the signal combination at the rising edge of the clock (CLK), /CS (Chip Select) must be low at the command input cycle. CKE (Clock Enable) must be high at one clock before the command input cycle as shown in below. The state of the /RAS, /CAS, and /WE signals specifies the command function to be executed. Some commands have the same signal combination for /RAS, /CAS, and /WE and are distinguished by some of address Input signals. When /CS becomes high, operations continue as specified in the command, but further commands (signal states that would specify a command) are not registered until /CS becomes low.

This state is Device deselect.



2.2 Command Truth Table

Function	*Symbol*	*/CS*	*/RAS*	*/CAS*	*/WE*	*A13*	*A12*	*A11*	*A10*	*A9*	*A8*	*A7*	*A6*	*A5*	*A4*	*A3*	*A2*	*A1*	*A0*
Device deselect	DESL	H	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
No operation	NOP	L	H	H	H	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Prefetch without auto precharge	PFC	L	H	H	L	BA	Cha.	Cha.	L	Cha.	Cha.	L	L	L	x	x	x	Seg.	Seg.
Prefetch with auto precharge	PFCA	L	H	H	L	BA	Cha.	Cha.	H	Cha.	Cha.	L	L	L	x	x	x	Seg.	Seg.
Restore without auto precharge	RST	L	H	H	L	BA	Cha.	Cha.	L	Cha.	Cha.	H	x	x	x	x	x	Seg.	Seg.
Restore with auto precharge	RSTA	L	H	H	L	BA	Cha.	Cha.	H	Cha.	Cha.	H	x	x	x	x	x	Seg.	Seg.
Channel read	READ	L	H	L	H	x	Cha.	Cha.	Col.	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.
Channel write	WRIT	L	H	L	L	L	Cha.	Cha.	Col.	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.
Bank activate	ACT	L	L	H	H	BA	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row
Prefetch read with auto precharge	PFR [Note]	L	L	H	L	Seg.	Cha.	Cha.	Seg.	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.
Precharge selected bank	PRE	L	L	L	L	BA	x	x	L	x	x	x	x	L	x	x	x	x	x
Precharge all banks	PALL	L	L	L	L	x	x	x	H	x	x	x	x	L	x	x	x	x	x
Set register operation	SCLR	L	L	L	L	L	L	L	L	L	L	L	L	H	PRL	RL	RL	RL	WT
	SCCR	L	L	L	L	L	Cha.	Cha.	Cha.	Cha.	L	L	H	H	x	x	BL	BL	BL

Note For x4 bits organization, this command is illegal.

Remark Abbreviations in the table mean as follows.

H : High level	L : Low level	X : High or Low level (Don' t care)
Row : Row address	Col. : Column address	BA : Bank Address
Cha. : Channel address	Seg. : Segment address	
BL : Burst length	RL : Read Latency	PRL : Prefetch Read Latency
WT : Wrap Type		

2.3 CKE Truth Table

Current state	Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	Address
			n–1	n					
Activating	Clock suspend mode entry	–	H	L	x	x	x	x	x
Any	Clock suspend	–	L	L	x	x	x	x	x
Clock suspend	Clock suspend mode exit	–	L	H	x	x	x	x	x
Idle	Auto refresh command	REF	H	H	L	L	L	H	x
Idle	Self refresh entry	SELF	H	L	L	L	L	H	x
Self refresh	Self refresh exit	–	L	H	L	H	H	H	x
			L	H	H	x	x	x	x
Idle	Power down entry	–	H	L	x	x	x	x	x
Power down	Power down exit	–	L	H	H	x	x	x	x
					L	H	H	H	x

Remark H: High level, L: Low level, x: High or Low level (Don' t care)

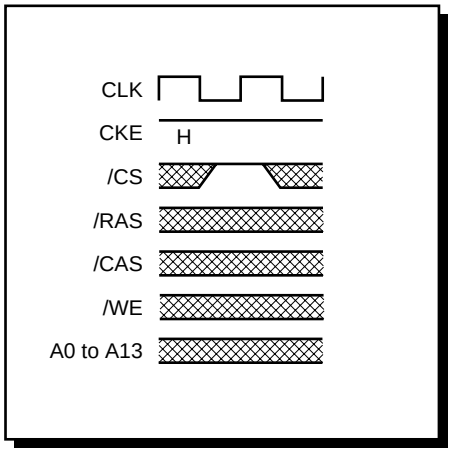
3. Commands

Device deselect (DESL)

	/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	High	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Remark x: High or Low level (Don' t care)

The device is deselected state by this command.

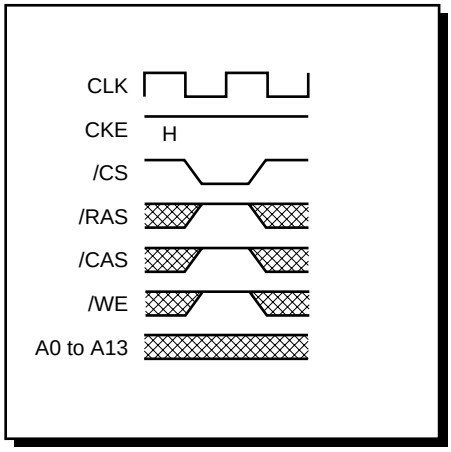


No operation (NOP)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	High	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Remark x: High or Low level (Don' t care)

This command is not a execution command. No operations begin or terminate by this command.



Prefetch without auto precharge (PFC)

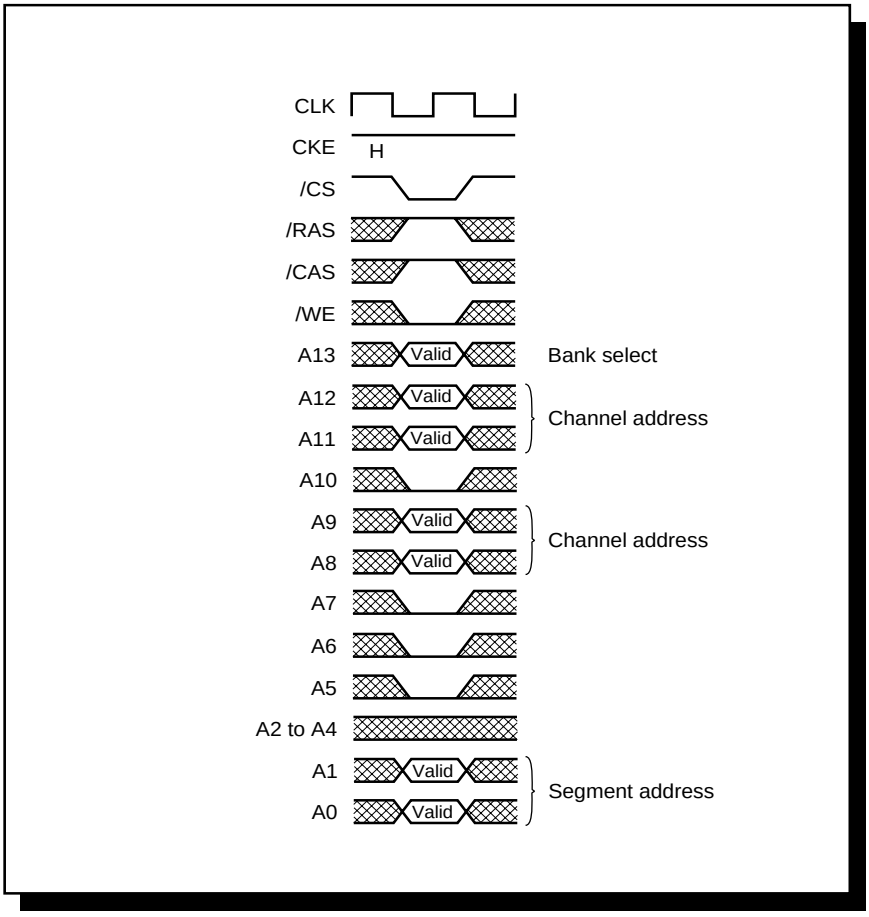
/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	Cha.	Cha.	Low	Cha.	Cha.	Low	Low	Low	x	x	x	Seg.	Seg.

Remark BA: Bank address, Cha.: Channel address, x: High or Low level (Don' t care), Seg.: Segment address

This command needs to follow Bank activate (ACT) command. This command fetches data from a segment of the activated row in a bank to a channel buffer which is chosen by channel address. The Segment and Bank fields specify the source segment and bank. In addition, the Channel Address field specifies the destination channel.

A10 specify the optional precharge operation. In case of A10: low, without auto precharge operation occurs. In case of A10: high, with auto precharge operation occurs after data fetch operation. (Please refer to **PFCA** command.) (Bank precharge is necessary after data fetch.)

This fetched command can be issued continuously without any precharge operation. For instance, when the first operation has been done from one of segment on activated row area to one of channel, if the second prefetch operation is required from same activated row, but different channel, the second prefetch command can be issued without any precharge operation. t_{PPD} (PFC to PFC/PFCA command period) is required between first and second prefetch command. When the new row address area need to be activated on same bank, bank precharge is necessary after this PFC command. t_{PPL} (PFC to PRE command period) is required between PFC and PRE. Fetched data into the channel buffer remains available for Channel Read and Channel Write operations.



Prefetch with auto precharge (PFCA)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	Cha.	Cha.	High	Cha.	Cha.	Low	Low	Low	x	x	x	Seg.	Seg.

Remark BA: Bank address, Cha.: Channel address, x: High or Low level (Don' t care), Seg.: Segment address

This command needs to follow Bank activate (ACT) command. This command fetches data from a segment of the activated row in a bank to a channel buffer, and precharge operation is performed automatically, which closes the activated row after data fetch operation.

The Segment and Bank fields specify the source segment and bank.

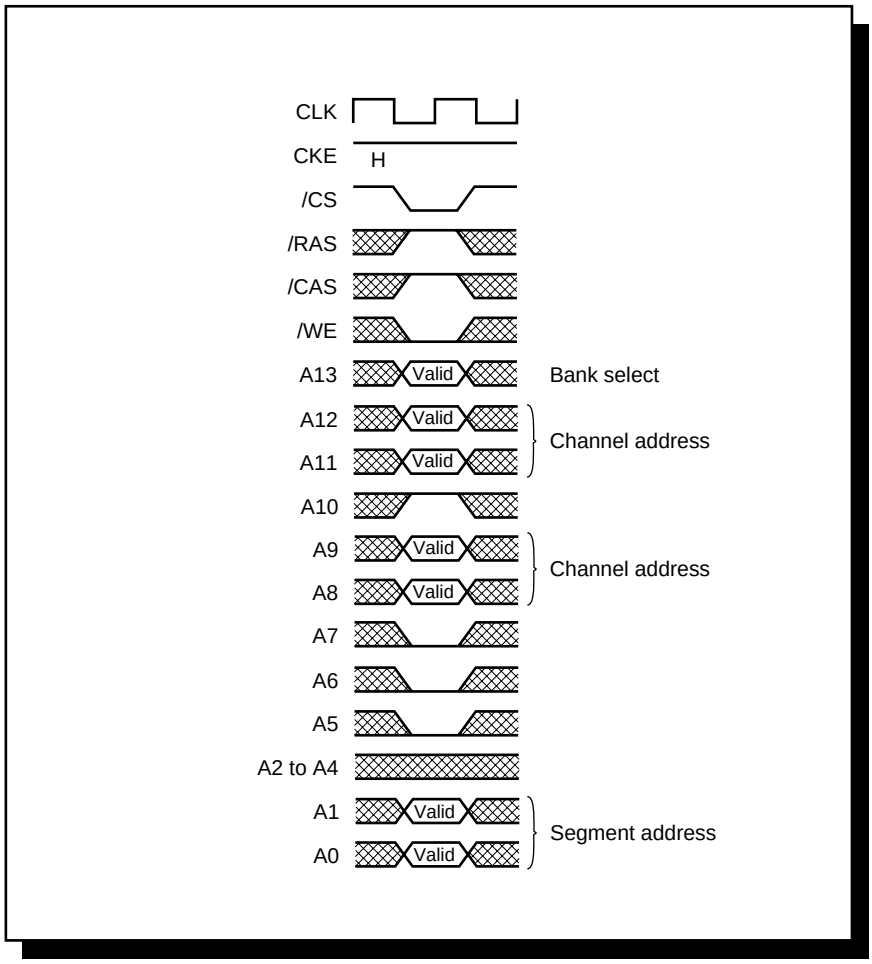
In addition, the Channel Address field specifies the destination channel.

A10 specify the optional precharge operation.

In case of A10: low, without auto precharge operation occurs. (Please refer to **PFC** command.)

In case of A10: high, with auto precharge operation occurs after data fetch operation.

Fetched data into the channel buffer remains available for Channel Read and Channel Write operations.



Restore without auto precharge (RST)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	Cha.	Cha.	Low	Cha.	Cha.	High	x	x	x	x	x	Seg.	Seg.

Remark BA: Bank address, Cha.: Channel address, x: High or Low level (Don' t care), Seg.: Segment address

This command transfers data from a channel buffer to a segment of a row which is going to be activated by following ACT command.

The command Bank Address field specifies the destination bank.

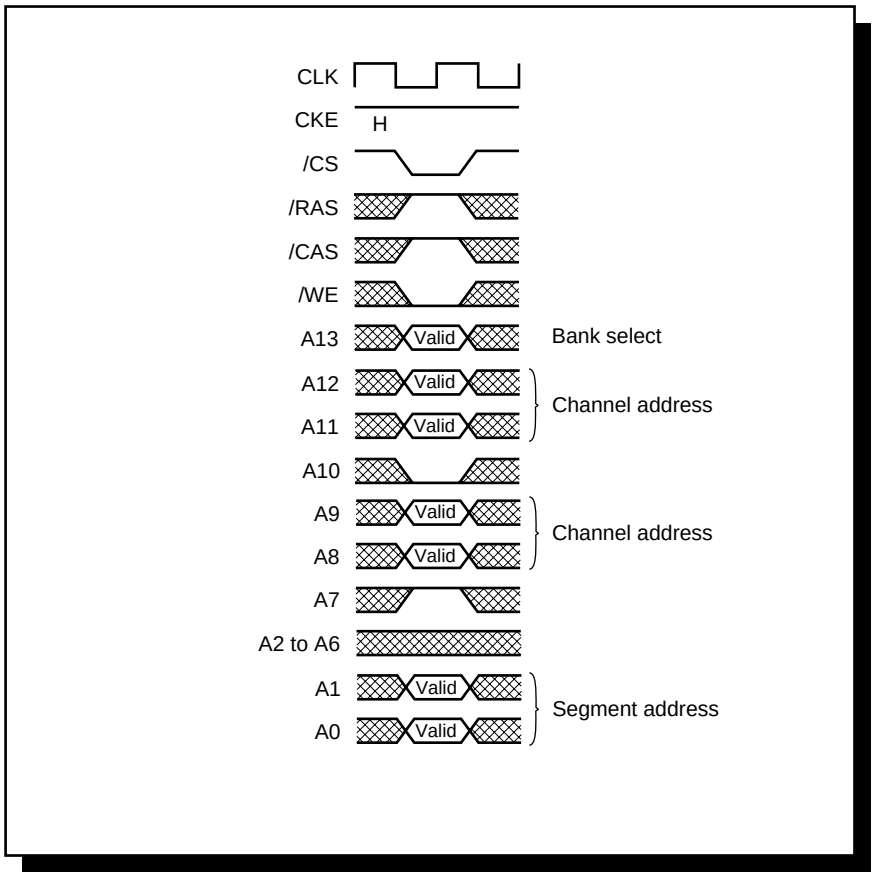
The Channel Address fields specify the source channel.

The Segment number field specifies the destination segment.

A10 specify the optional precharge operation.

In case of A10: low, without auto precharge operation occurs. (Please refer to **RSTA** command.)

In case of A10: high, with auto precharge operation occurs after data fetch operation.



Restore with auto precharge (RSTA)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	Cha.	Cha.	High	Cha.	Cha.	High	x	x	x	x	x	Seg.	Seg.

Remark BA: Bank address, Cha.: Channel address, x: High or Low level (Don' t care), Seg.: Segment address

This command transfers data from a channel buffer to a segment of a row which is going to be activated by following ACT command.

In addition, precharge operation is performed automatically which closes the active row after data restore operation.

The command Bank Address field specifies the destination bank.

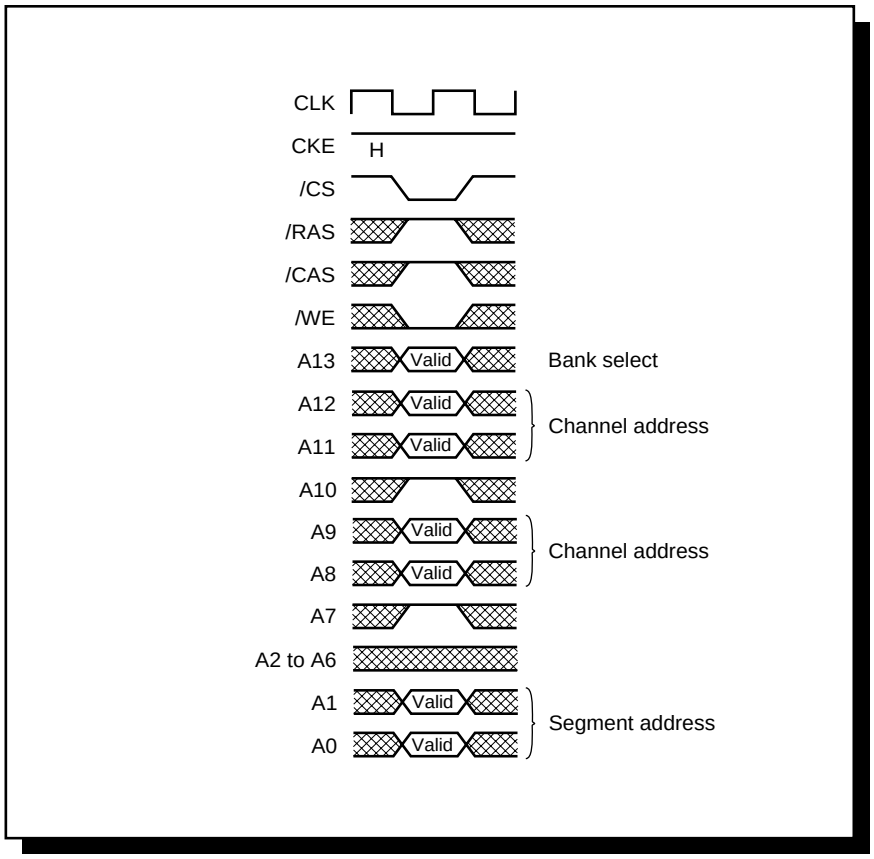
The Channel Address fields specify the source channel.

The Segment number field specifies the destination segment.

A10 specify the optional precharge operation.

In case of A10: low, without auto precharge operation occurs. (Please refer to **RSTA** command.)

In case of A10: high, with auto precharge operation occurs after data fetch operation.

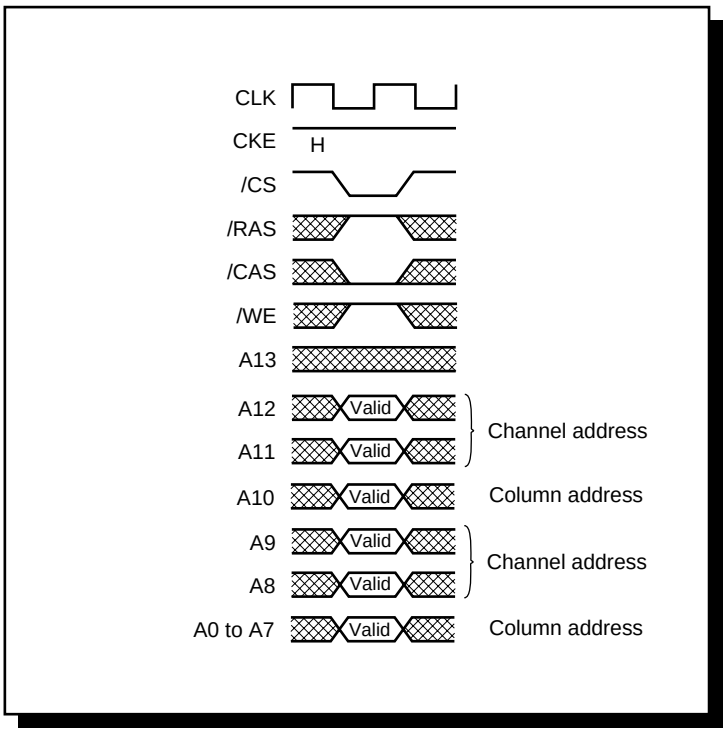


Channel read (READ)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	Low	High	x	Cha.	Cha.	Col.	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.

Remark x: High or Low level (Don' t care), Cha.: Channel address, Col.: Column address

Channel Read (READ) reads data words from a channel buffer onto the data bus (DQ). The Channel Address field specifies the source channel. The Column Address field specifies the starting location of the data word in the buffer (Data words may be 4, 8, or 16 bits.). The burst-length field in the channel control register for the channel specifies the number of data words to complete the read operation.



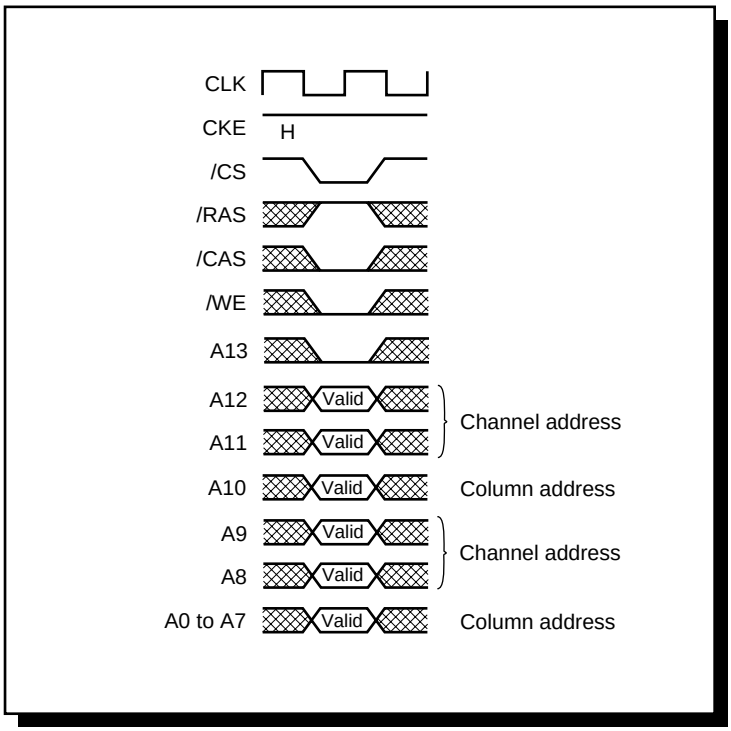
Channel write (WRIT)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	Low	Low	Low	Cha.	Cha.	Col.	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.

Remark x: High or Low level (Don' t care), Cha.: Channel address, Col.: Column address

Channel Write(WRIT) writes data from the data bus (DQ) into a channel buffer. The Channel Address field specifies the destination channel. The Column Address field specifies the starting location of the data word in the buffer (Data words may be 4, 8 or 16 bits.).

The burst-length field in the channel control register for the channel specifies the number of data words to complete the write operation.

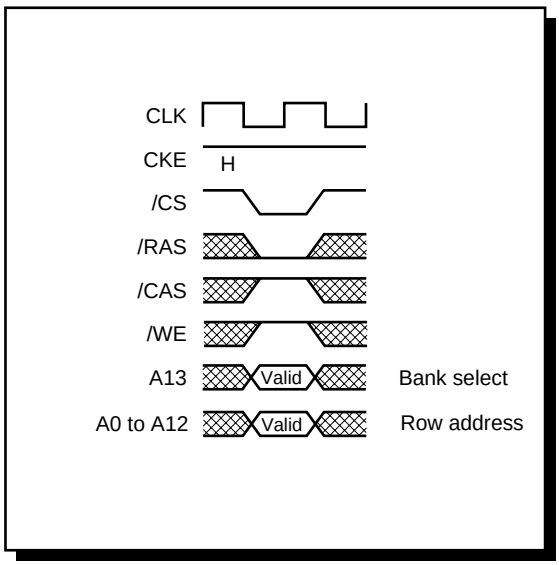


Bank activate (ACT)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	High	High	BA	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row

Remark BA: Bank address, Row: Row address

Activation causes row contents to be placed into the bank's sense amplifier. The command Bank Address and Row Address fields specify bank and row. This device has two banks, each with 8,192 rows. This command activates the bank selected by bank address(A13) and a row address selected by A0 through A12. The row remains active for access until a Precharge command is issued to the bank. A Precharge command must be issued before another row can be activated in that bank. Each bank can have one row active. This command corresponds to a conventional DRAM's /RAS falling.



Prefetch read with auto precharge (PFR)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	High	Low	Seg.	Cha.	Cha.	Seg.	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.

Remark Seg.: Segment address, Cha.: Channel address, Col.: Column address

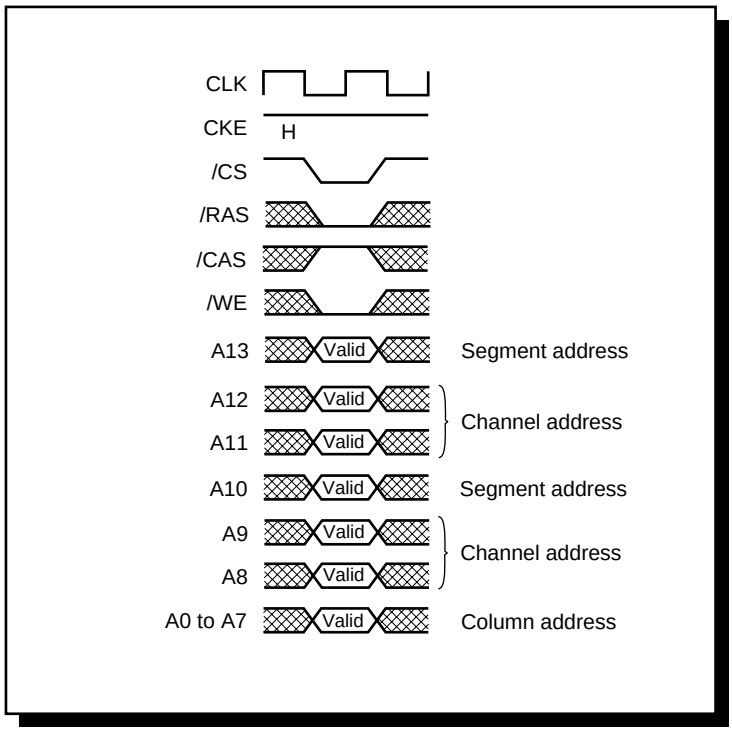
This command needs to follow Bank activate (ACT) command. This command fetches data from a segment of the activated row in a bank to a channel buffer, and reads data words from a channel buffer onto the data bus (DQ).

In addition, precharge operation is performed automatically, which closes the activated row after data fetch operation.

The Segment fields specify the source segment. In addition, the Channel Address field specifies the destination channel.

The Column Address field specifies the starting location of the data word in the buffer (Data words may be 4, 8, or 16 bits.). The burst-length field in the channel control register for the channel specifies the number of data words to complete the read operation.

For x4 bits organization, this command is illegal.



Precharge selected bank (PRE)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	Low	Low	BA	x	x	Low	x	x	x	x	Low	x	x	x	x	x

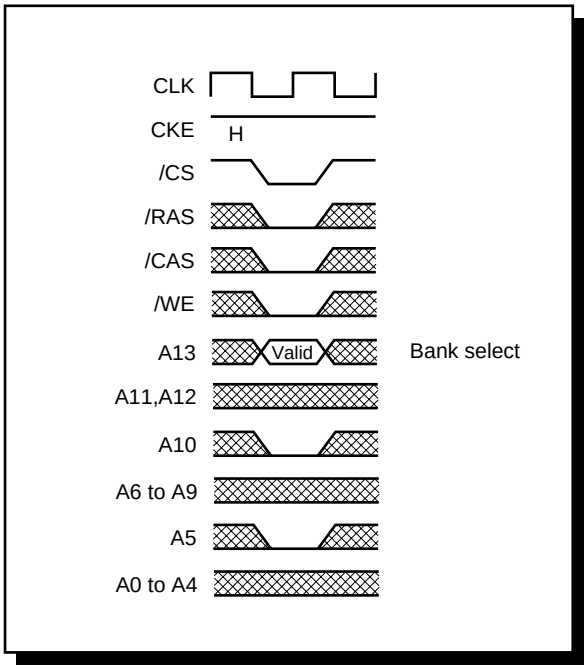
Remark BA: Bank address, x: High or Low level (Don' t care)

This command closes (deactivates) an activated row in a bank, in order to prepare the bank for an Activate or Restore command to activate a new row. After precharging, a bank is in the Idle state.

The Bank field specifies the bank to precharge and A10 Low specifies the command.

After this command, t_{RP} (precharge to activate command period) must be satisfied for next activate command to precharging bank.

This command corresponds to a conventional DRAM's /RAS rising.

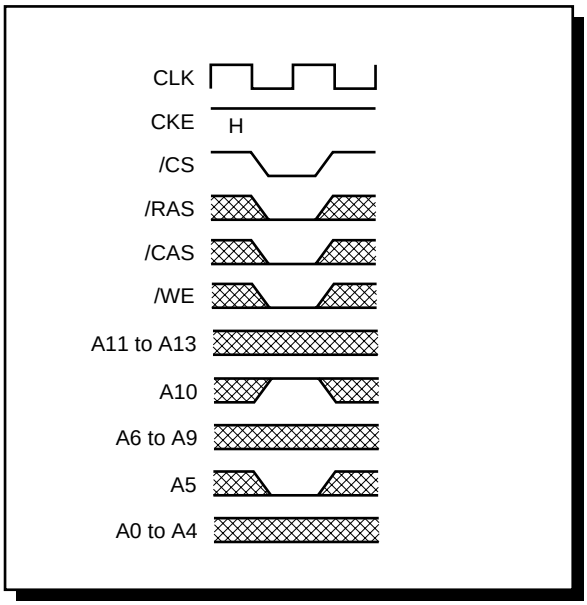


Precharge all banks (PALL)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	Low	Low	x	x	x	High	x	x	x	x	Low	x	x	x	x	x

Remark x: High or Low level (Don' t care)

The signal combination is Reserved (with command modifier A10 High). The PALL command is typically used during auto refresh operation and initialization. Replace with Precharge commands for each bank.



Set Channel Latency Register (SCLR)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	High	PRL	RL	RL	RL	WT

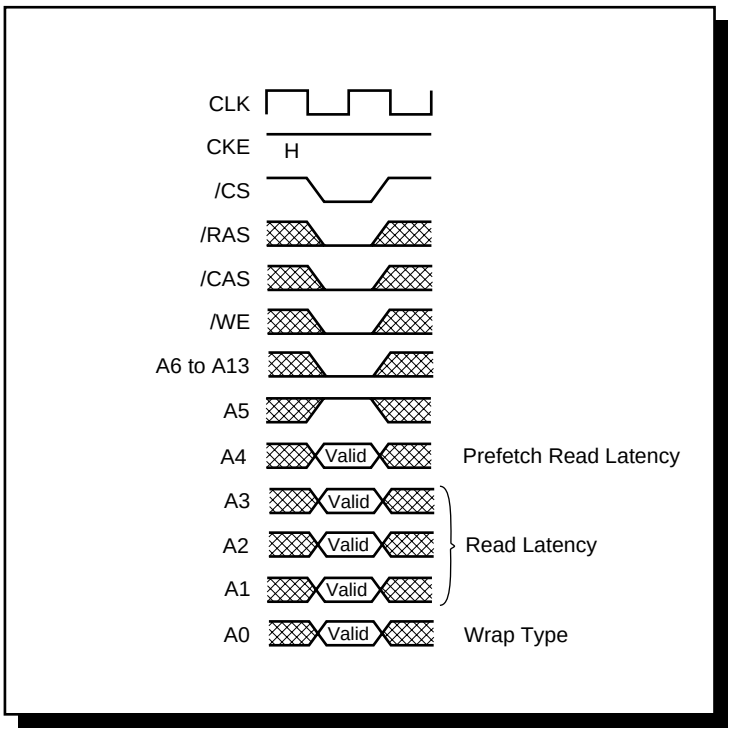
Remark PRL: Prefetch Read Latency, RL: Read Latency, WT: Wrap Type

This command sets the Read Latency value which specifies read delay time in channel read operation.

In addition, this command sets the Wrap type which specifies the order(Sequential or Interleave) in which the burst data will be addressed.

Moreover, this command sets the Read Latency value which specifies read delay time in prefetch read operation.

The commands can only be executed with all memory banks idle and no burst operations in progress.



Set Channel Control Register (SCCR)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	Low	Low	Low	Cha.	Cha.	Cha.	Cha.	Low	Low	High	High	x	x	BL	BL	BL

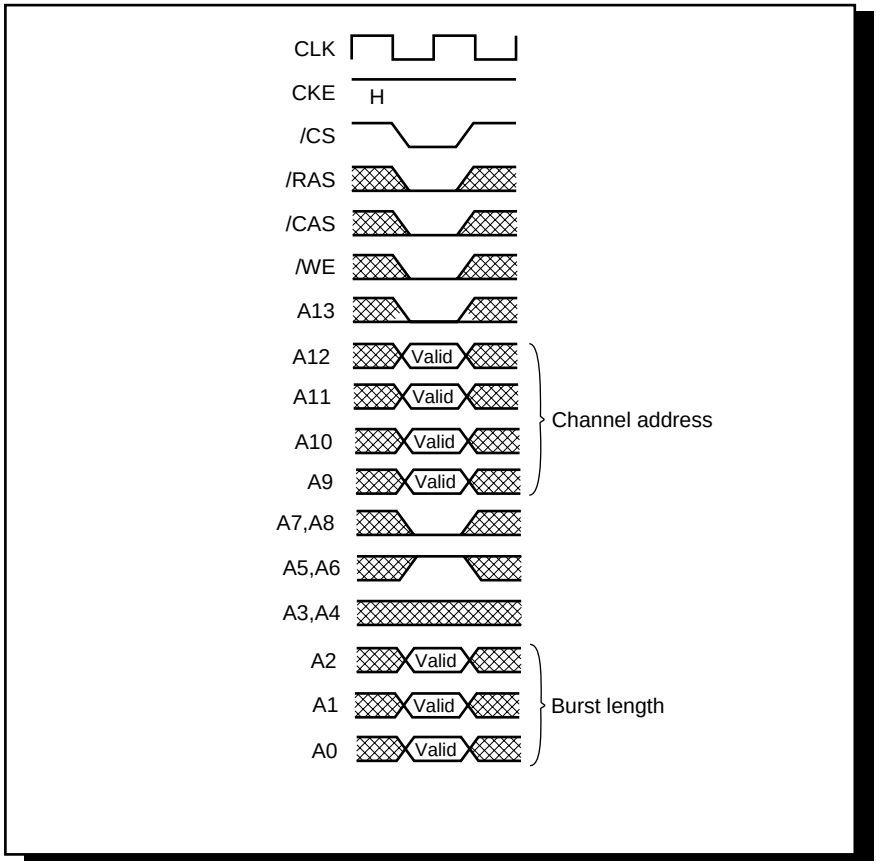
Remark Cha.: Channel address, BL: Burst Length, x: High or Low level (Don' t care)

This command sets Burst Length in channel address.

Burst Length for the 0-15 channels is the same.

This command is executed during Initialization.

The commands can only be executed with all memory banks idle and no burst operations in progress.

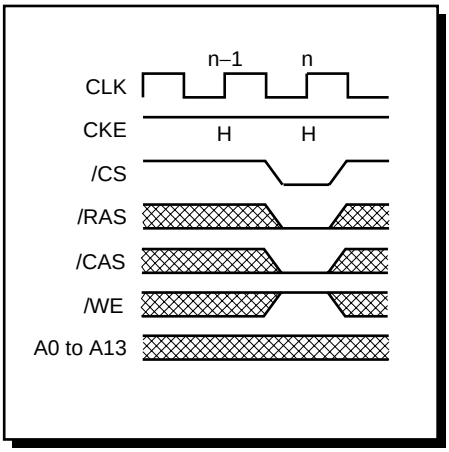


Auto Refresh (REF)

	CKE		*/CS*	*/RAS*	*/CAS*	*/WE*	*Address*
	n–1	*n*					
	High	High	Low	Low	Low	High	High or Low level (Don' t care)

This command is a request to begin the auto refresh operation. The refresh address is generated internally.

Before executing auto refresh, all banks must be in the idle state. After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command. During t_{RC} period (from refresh command to refresh or activate command), the VirtualChannel SDRAM cannot accept any other command.

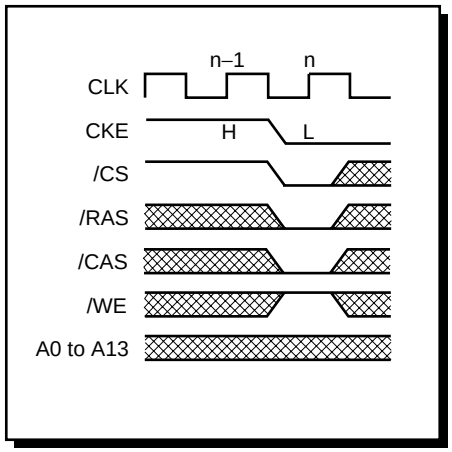


Self Refresh (SELF)

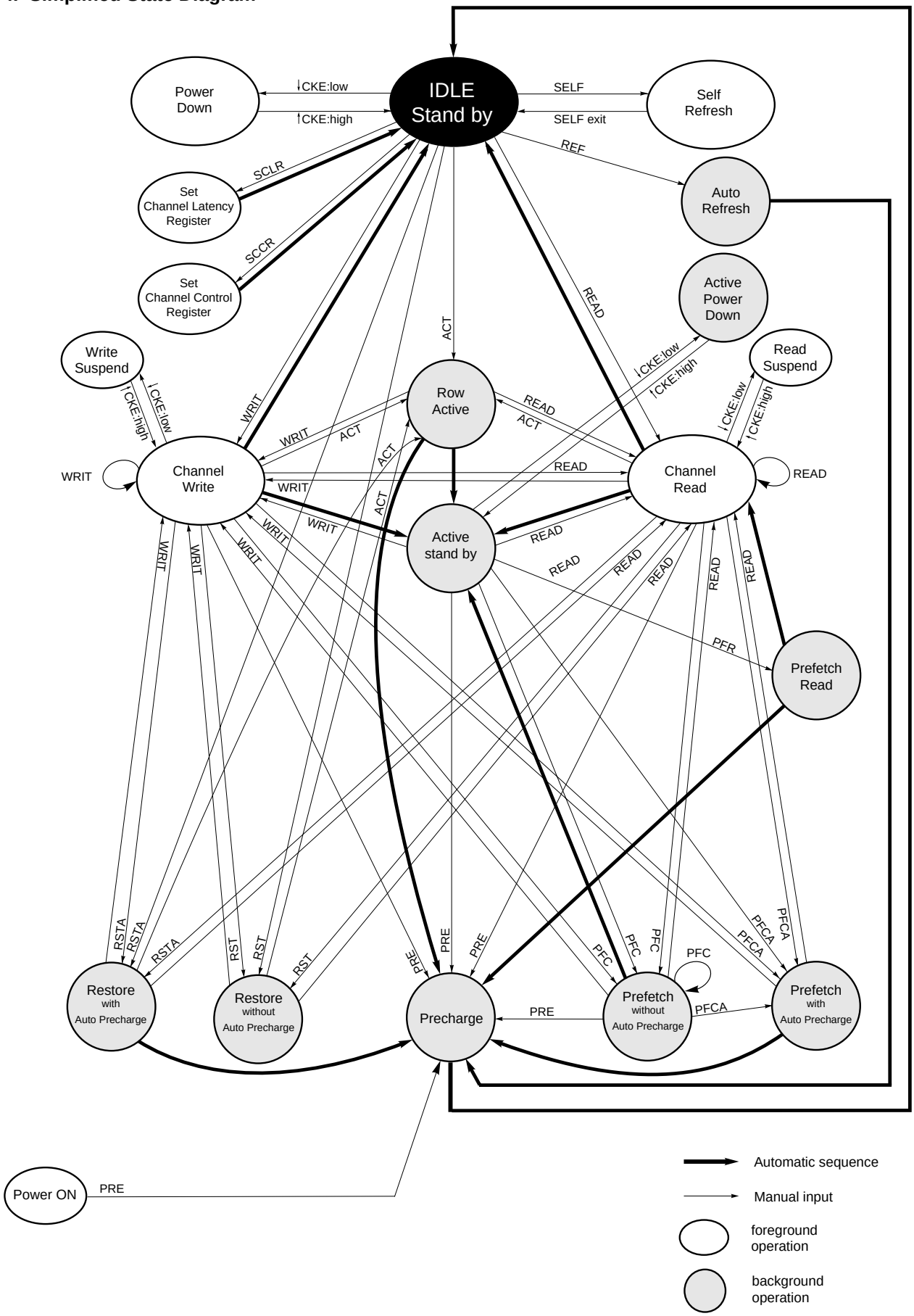
	CKE		*/CS*	*/RAS*	*/CAS*	*/WE*	*Address*
	n–1	*n*					
	High	Low	Low	Low	Low	High	High or Low level (Don' t care)

After the command execution, self refresh operation continues while CKE remains low. During self refresh mode, the internal refresh controller takes care of refresh interval and refresh operation. There is no need for external control. Before executing self refresh, both banks must be in the idle state.

During self refresh mode, both background and foreground operation can not be executed.



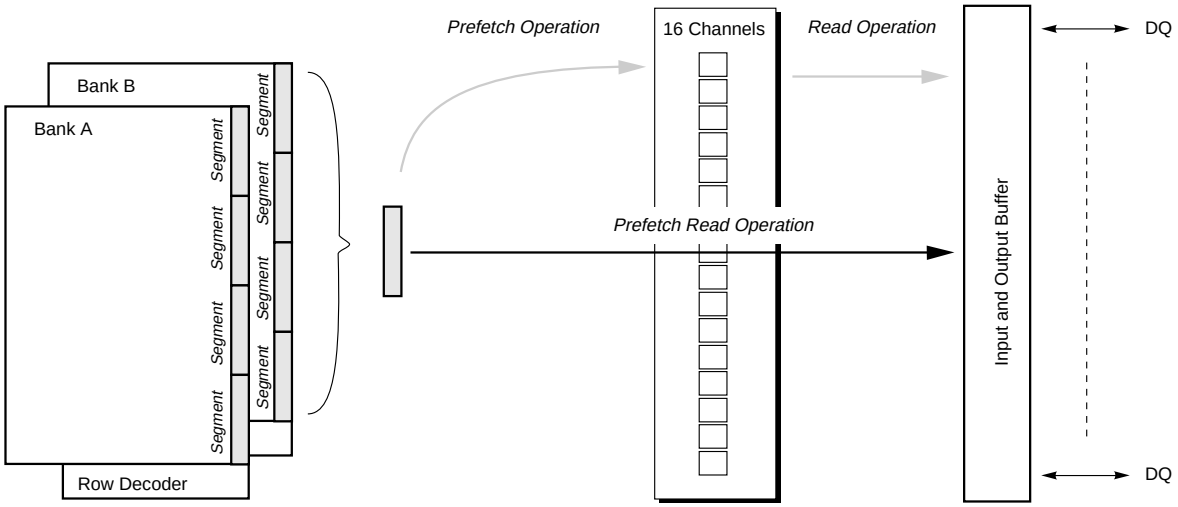
4. Simplified State Diagram

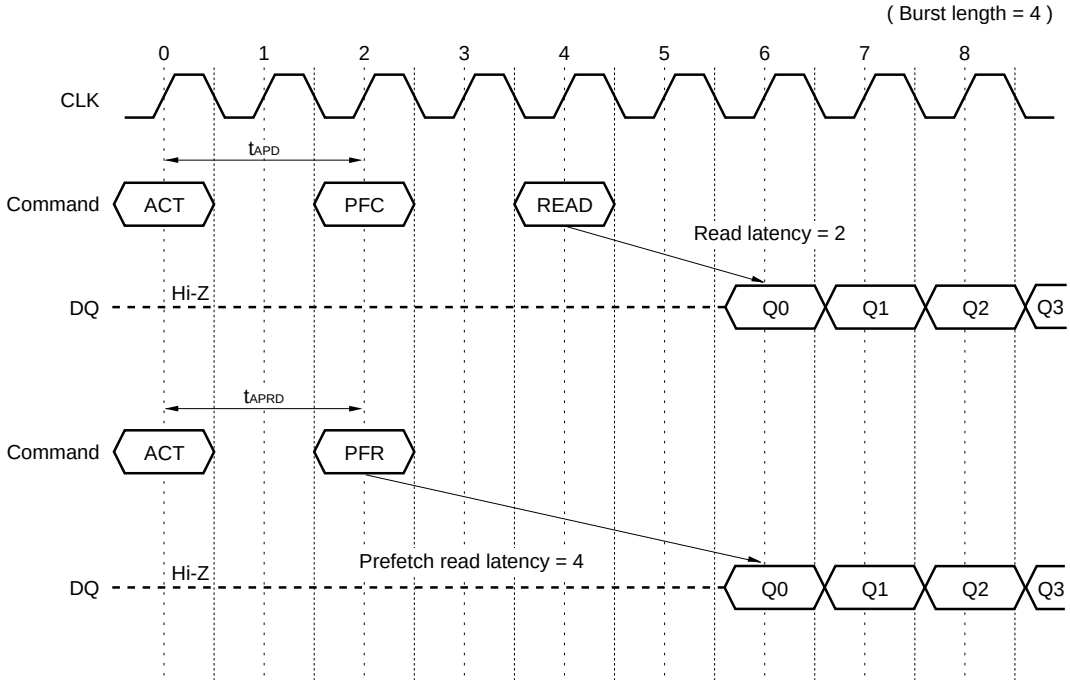


5. Prefetch Read Operation (Optional)

This operation fetches data from a segment of the activated row in a bank to a channel buffer, and reads data words from a channel buffer onto the data bus (DQ). In addition, precharge operation is performed automatically, which closes the activated row after data fetch operation.

For x4 bits organization, prefetch read operation can not be used (PFR command is illegal).





The relationship between clock frequency and read latency, prefetch read latency

Clock frequency MHz(MAX.)	Read latency	Prefetch read latency
133 100	2	4
67 50	1	2

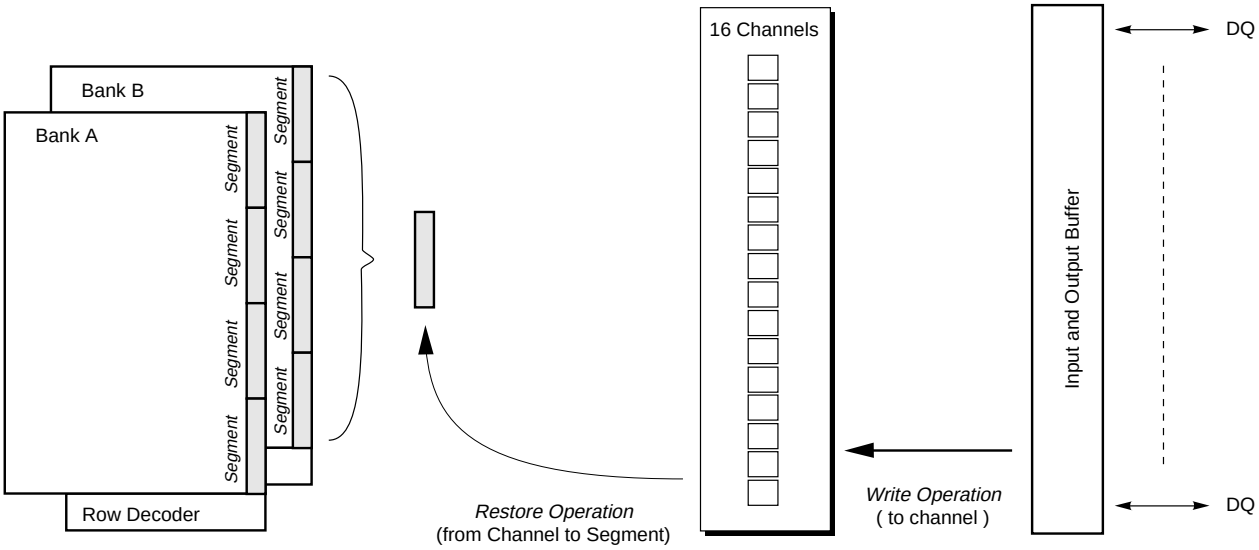
6. Write Operation and Restore Operation

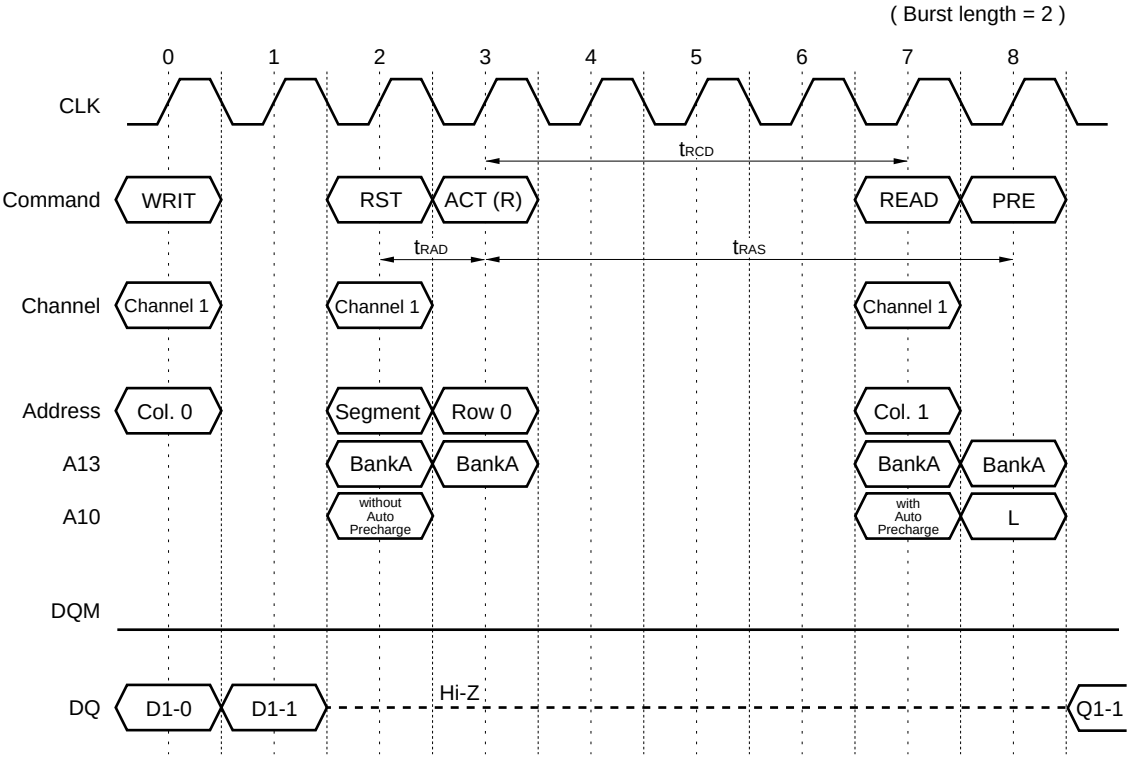
Write command proceeds write operation to the channel. When the system needs to refill the channel with new data, restore operation may be necessary. The restore operation needs both restore command and active command. Restore command must be first command. Restore operation is also fully associative operation.

The data in the channel can be transferred to anywhere on memory core array. Another write and read operation to another channel can proceed during this restore operation.

The another background operation is illegal while t_{RAD} (RST/RSTA to ACT(R) command delay time).

In addition, the foreground operation to the same channel set by RST command is illegal too.

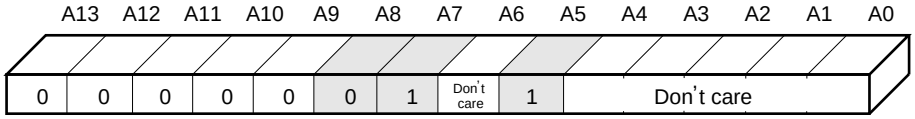




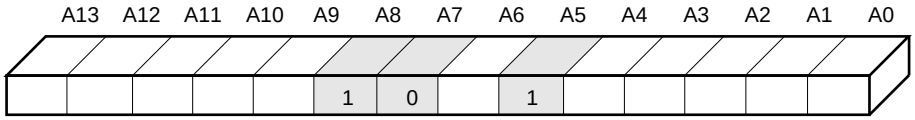
Remark ACT(R) command is ACT command after RST command.

7. Set Register Operation

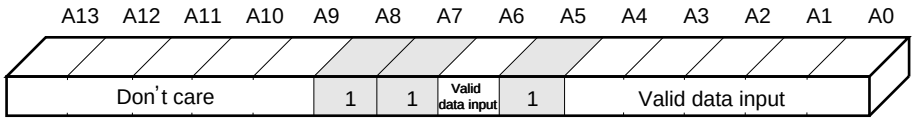
JEDEC standard test set (Refresh counter test)



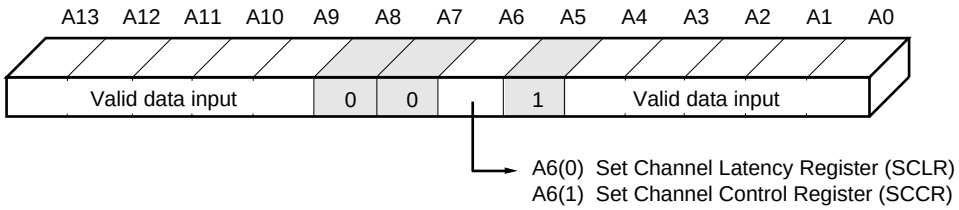
Use in future



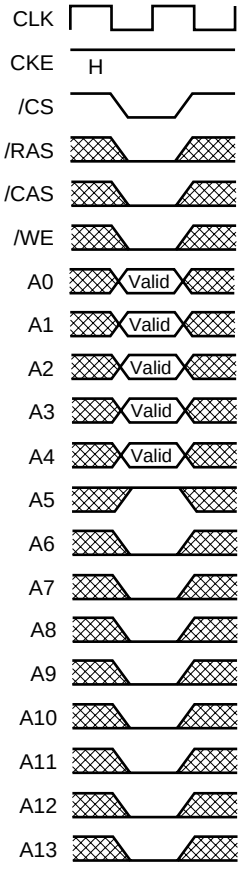
Vender specification

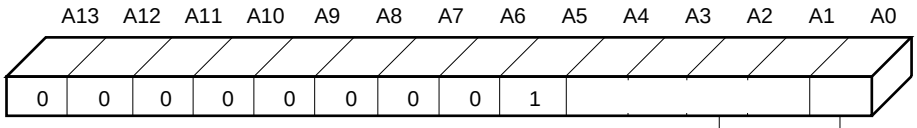


Mode register set



8. Set Channel Latency Register (SCLR)





Wrap type

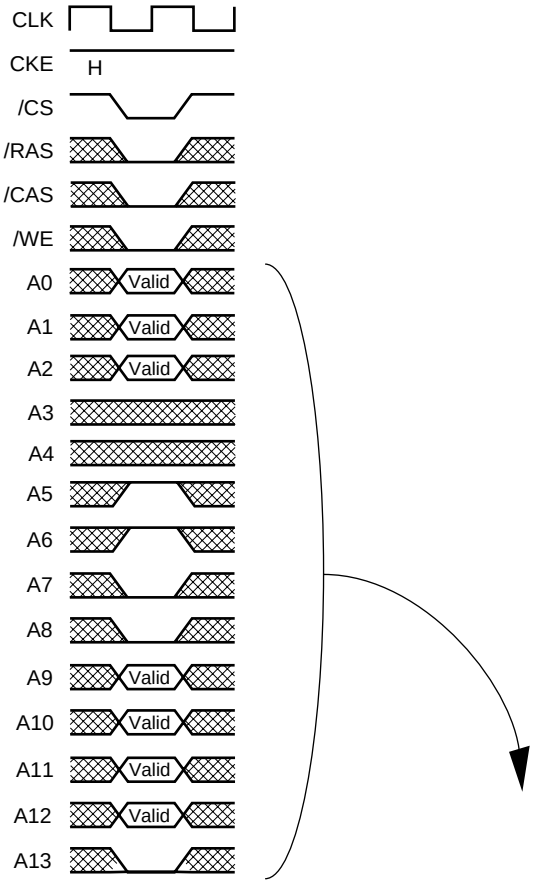
A0	Wrap type
0	Sequential
1	Interleave

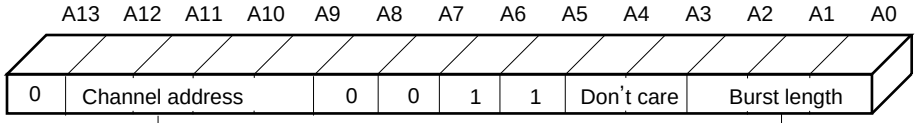
Read latency and Prefetch read latency

A4	A2	A1	Read latency	Prefetch read latency	Remark
0	0	1	1	2	legal
1	0	1	1	3	illegal
0	1	0	2	3	illegal
1	1	0	2	4	legal

Remark For x4 bits organization, Prefetch read latency (A4) is don't care.

9. Set Channel Control Register (SCCR)





Channel number

Channel number	A12	A11	A10	A9
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Burst length

Sequential	Interleave	A2	A1	A0
1	1	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
16	16	1	0	0
Reserved	Reserved	1	0	1
Reserved	Reserved	1	1	0
Reserved	Reserved	1	1	1

10. Burst Length and Sequence

[Burst of Two]

Starting Address (column address A0) (binary)	Addressing Sequence Sequential (decimal)	Addressing Sequence Interleave (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

Starting Address (column address A1,A0) (binary)	Addressing Sequence Sequential (decimal)	Addressing Sequence Interleave (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

Starting Address (column address A2-A0) (binary)	Addressing Sequence Sequential (decimal)	Addressing Sequence Interleave (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

[Burst of Sixteen]

Starting Address (column address A3-A0) (binary)	Addressing Sequence Sequential (decimal)	Addressing Sequence Interleave (decimal)
0000	0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15	0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15
0001	1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,0	1,0,3,2,5,4,7,6,9,8,11,10,13,12,15,14
0010	2,3,4,5,6,7,8,9,10,11,12,13,14,15,0,1	2,3,0,1,6,7,4,5,10,11,8,9,14,15,12,13
0011	3,4,5,6,7,8,9,10,11,12,13,14,15,0,1,2	3,2,1,0,7,6,5,4,11,10,9,8,15,14,13,12
0100	4,5,6,7,8,9,10,11,12,13,14,15,0,1,2,3	4,5,6,7,0,1,2,3,12,13,14,15,8,9,10,11
0101	5,6,7,8,9,10,11,12,13,14,15,0,1,2,3,4	5,4,7,6,1,0,3,2,13,12,15,14,9,8,11,10
0110	6,7,8,9,10,11,12,13,14,15,0,1,2,3,4,5	6,7,4,5,2,3,0,1,14,15,12,13,10,11,8,9
0111	7,8,9,10,11,12,13,14,15,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0,15,14,13,12,11,10,9,8
1000	8,9,10,11,12,13,14,15,0,1,2,3,4,5,6,7	8,9,10,11,12,13,14,15,0,1,2,3,4,5,6,7
1001	9,10,11,12,13,14,15,0,1,2,3,4,5,6,7,8	9,8,11,10,13,12,15,14,1,0,3,2,5,4,7,6
1010	10,11,12,13,14,15,0,1,2,3,4,5,6,7,8,9	10,11,8,9,14,15,12,13,2,3,0,1,6,7,4,5
1011	11,12,13,14,15,0,1,2,3,4,5,6,7,8,9,10	11,10,9,8,15,14,13,12,3,2,1,0,7,6,5,4
1100	12,13,14,15,0,1,2,3,4,5,6,7,8,9,10,11	12,13,14,15,8,9,10,11,4,5,6,7,0,1,2,3
1101	13,14,15,0,1,2,3,4,5,6,7,8,9,10,11,12	13,12,15,14,9,8,11,10,5,4,7,6,1,0,3,2
1110	14,15,0,1,2,3,4,5,6,7,8,9,10,11,12,13	14,15,12,13,10,11,8,9,6,7,4,5,2,3,0,1
1111	15,0,1,2,3,4,5,6,7,8,9,10,11,12,13,14	15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0

11. Initialization

The VirtualChannel SDRAM is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, when power is applied, a 100 μs or longer pause must precede any signal toggling.

(2) After the pause, both banks must be precharged using the Precharge command (The Precharge all banks command is convenient).

(3) Once the precharge is completed and the minimum t_{RP} is satisfied, the mode register can be programmed. After the mode register set cycle, t_{RSC} (2 CLK minimum) pause must be satisfied as well.

(4) Two or more auto refresh must be performed.

Remarks 1. The sequence of Mode register programming and Refresh above may be transposed.

2. CKE and DQM must be held high until the Precharge command is issued to ensure data-bus Hi-Z.

12. Electrical Specifications (Target)

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute **Power on sequence and Auto Refresh** before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}, $V_{CC}Q$		–0.5 to +4.6	V
Voltage on input pin relative to GND	V_T		–0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}, $V_{CC}Q$		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3 Note1	V
Low level input voltage	V_{IL}		–0.3 Note2		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Notes 1. $V_{IH\ (MAX.)} = V_{CC} + 1.5$ V (Pulse width ≤ 5 ns)

2. $V_{IL\ (MIN.)} = -1.5$ V (Pulse width ≤ 5 ns)

★ **Capacitance (T_A = 25 °C, f = 1 MHz)**

Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	CLK	-A75	2.5		3.5	pF
			-A10	2.5		4.0	
	C_{I2}	A0 - A13,CKE, /CS,/RAS, /CAS,	-A75	2.5		3.8	
		/WE,DQM, UDQM, LDQM	-A10	2.5		4.0	
Data input/output capacitance	$C_{I/O}$	DQ		4.0		6.5	pF

★ **DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)**

Parameter	Symbol	Test condition	Grade	Read Latency	Maximum. x4	Maximum. x8	Maximum. x16	Unit	Notes
Operating current (Prefetch mode at one bank active)	$I_{CC1}P$	$t_{RC} \geq t_{RC(MIN.)}$ Prefetch is executed one time during t_{RC}.	-A75	RL=1	TBD			mA	1
				RL=2	150				
			-A10	RL=1	TBD				
				RL=2	130				
Operating current (Restore mode at one bank active)	$I_{CC1}R$	$t_{RC} \geq t_{RC(MIN.)}$	-A75	RL=1	TBD			mA	1
				RL=2	150				
			-A10	RL=1	TBD				
				RL=2	130				
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns			1.2			mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞			1.2				
Precharge standby current in non power down mode	$I_{CC2}N$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns /CS≥$V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.			20			mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ Input signals are stable.			10				
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns			6			mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞			6				
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns /CS ≥ $V_{IH(MIN.)}$ Input signals are changed one time during 30 ns.			30			mA	
	$I_{CC3}NS$	CKE≥$V_{IH(MIN.)}$,t_{CK}=∞ Input signals are stable.			20				
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA, Background: precharge standby	-A75	RL=1	TBD			mA	2
				RL=2	60	65	75		
			-A10	RL=1	TBD				
				RL=2	45	50	75		
Auto refresh current	I_{CC5}	$t_{RCF} \geq t_{RCF(MIN.)}$	-A75	RL=1	TBD			mA	3
				RL=2	230				
			-A10	RL=1	TBD				
				RL=2	220				
Self refresh current	I_{CC6}	CKE ≤ 0.2 V			2			mA	

Notes 1. I_{CC1} depends on cycle rates. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

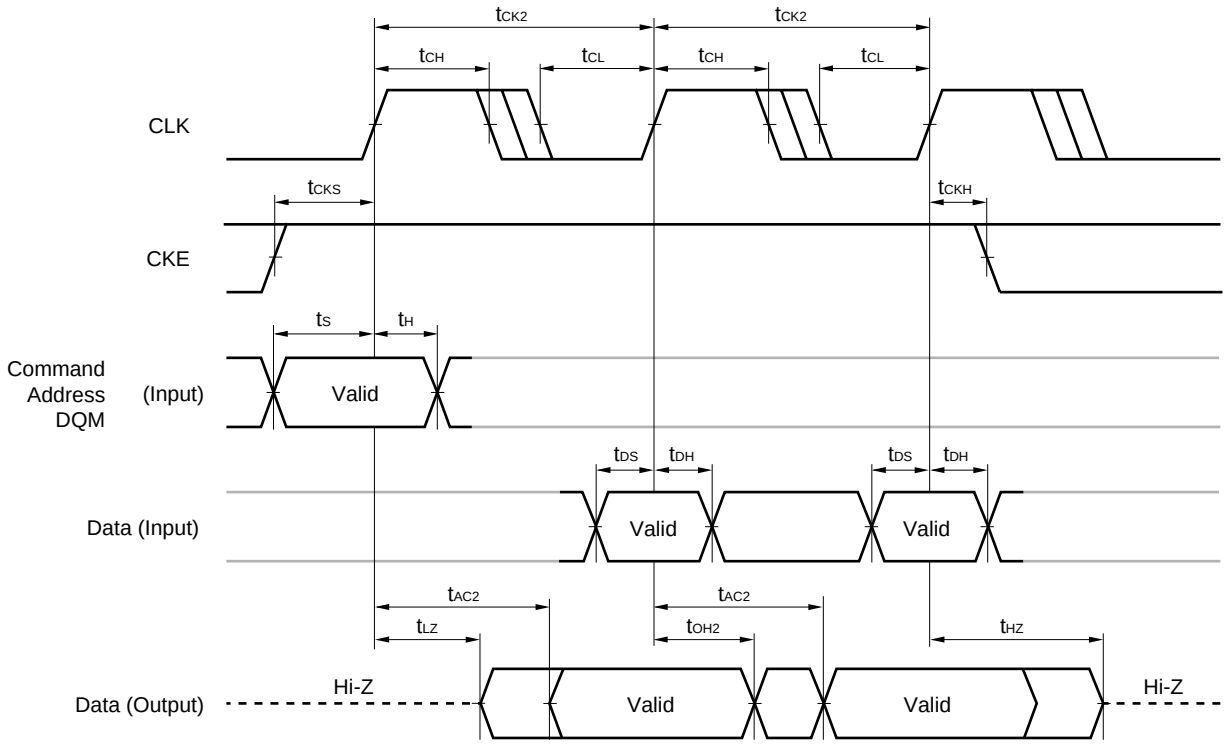
DC Characteristics 2 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit	Note
Input leakage current	$I_{I(L)}$	0 ≤ V_I ≤ $V_{CC}Q$, $V_{CC}Q$ = V_{CC} All other pins not under test = 0 V	– 1.0	–	+ 1.0	μA	
Output leakage current	$I_{O(L)}$	0 ≤ V_O ≤ $V_{CC}Q$, D_{OUT} is disabled.	– 1.5	–	+ 1.5	μA	
High level output voltage	V_{OH}	I_O = – 4 mA	2.4	–	–	V	
Low level output voltage	V_{OL}	I_O = + 4 mA	–	–	0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

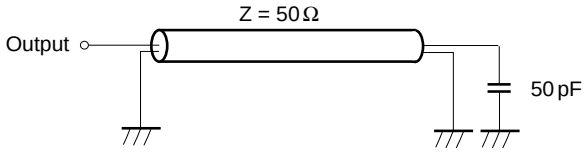
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$.
- An access time is measured at 1.4 V.



AC characteristics(Target)

	Parameter		Symbol	-A75		-A10		Unit	Note
				MIN.	MAX.	MIN.	MAX.		
★	Clock cycle time	RL=1	t_{CK1}	15	–	20	–	ns	
		RL=2	t_{CK2}	7.5	–	10	–	ns	
★	Access time from CLK	RL=1	t_{AC1}	–	12	–	15	ns	1
		RL=2	t_{AC2}	–	5.4	–	6	ns	
	CLK high level width		t_{CH}	2.5	–	3	–	ns	
	CLK low level width		t_{CL}	2.5	–	3	–	ns	
	Data-out hold time		t_{OH}	2.7	–	3	–	ns	1
	Data-out low-impedance time		t_{LZ}	0	–	0	–	ns	
★	Data-out high-impedance time	RL=1	t_{HZ1}	2.5	12	3	15	ns	
		RL=2	t_{HZ2}	2.5	5.4	3	6	ns	
	Data-in setup time		t_{DS}	1.5	–	2	–	ns	
	Data-in hold time		t_{DH}	0.8	–	1	–	ns	
	Address, Command, DQM setup time		t_{S}	1.5	–	2	–	ns	
	Address, Command, DQM hold time		t_{H}	0.8	–	1	–	ns	
	CKE setup time		t_{CKS}	1.5	–	2	–	ns	
	CKE hold time		t_{CKH}	0.8	–	1	–	ns	
	CKE setup time (Power down exit)		t_{CKSP}	1.5	–	2	–	ns	
	Transition time		t_{T}	0.8	30	1	30	ns	
	Refresh time (4,096 refresh cycle)		t_{REF}	–	64	–	64	ms	
	Mode register set cycle time		t_{RSC}	2	–	2	–	CLK	

Note1 Output load.



AC characteristics (Background to Background operation)

Parameter	Symbol	-A75		-A10		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
SAME BANK OPERATION							
ACT to ACT/REF Command period	t_{RC}	67.5	–	80	–	ns	
REF to REF/ ACT Command period	t_{RCF}	67.5	–	90	–	ns	
ACT to PRE Command period	t_{RAS}	52.5	120,000	60	120,000	ns	
PRE to ACT / REF Command period	t_{RP}	20	–	20	–	ns	
ACT to PFC/PFCA Command delay time	t_{APD}	15	–	20	–	ns	
ACT to PFR Command delay time (Prefetch Read Operation)	t_{APRD}	15	–	20	–	ns	3
PFC to PRE Command delay time	t_{PPL}	22.5	–	30	–	ns	
PFCA / PFR to ACT/REF Command delay time	t_{PAL}	45	–	50	–	ns	
RST / RSTA to ACT(R) [Note1] Command delay time	t_{RAD}	7.5	30	10	40	ns	2
SAME,OTHER BANK OPERATION							
ACT(R) [Note1] to PFC/PFCA/PFR Command delay time	t_{RPD}	37.5	–	40	–	ns	
PFC to PFC / PFCA Command delay time	t_{PPD}	22.5	–	30	–	ns	
OTHER BANK OPERATION							
ACT to ACT/ACT(R) or ACT(R) to ACT Command delay time	t_{RRD}	15	–	20	–	ns	
ACT(R) to ACT(R) Command delay time	t_{RRDR}	30	–	40	–	ns	
PFC /PFCA to RST /RSTA Command delay time	t_{PRD}	22.5	–	30	–	ns	

Notes 1 ACT(R) command is ACT command after RST command.

2 The another background operation and same channel foreground operation are illegal while t_{RAD} period.

3 For x4 bits organization, prefetch read operation can not used.

AC characteristics (Foreground to Foreground operation)

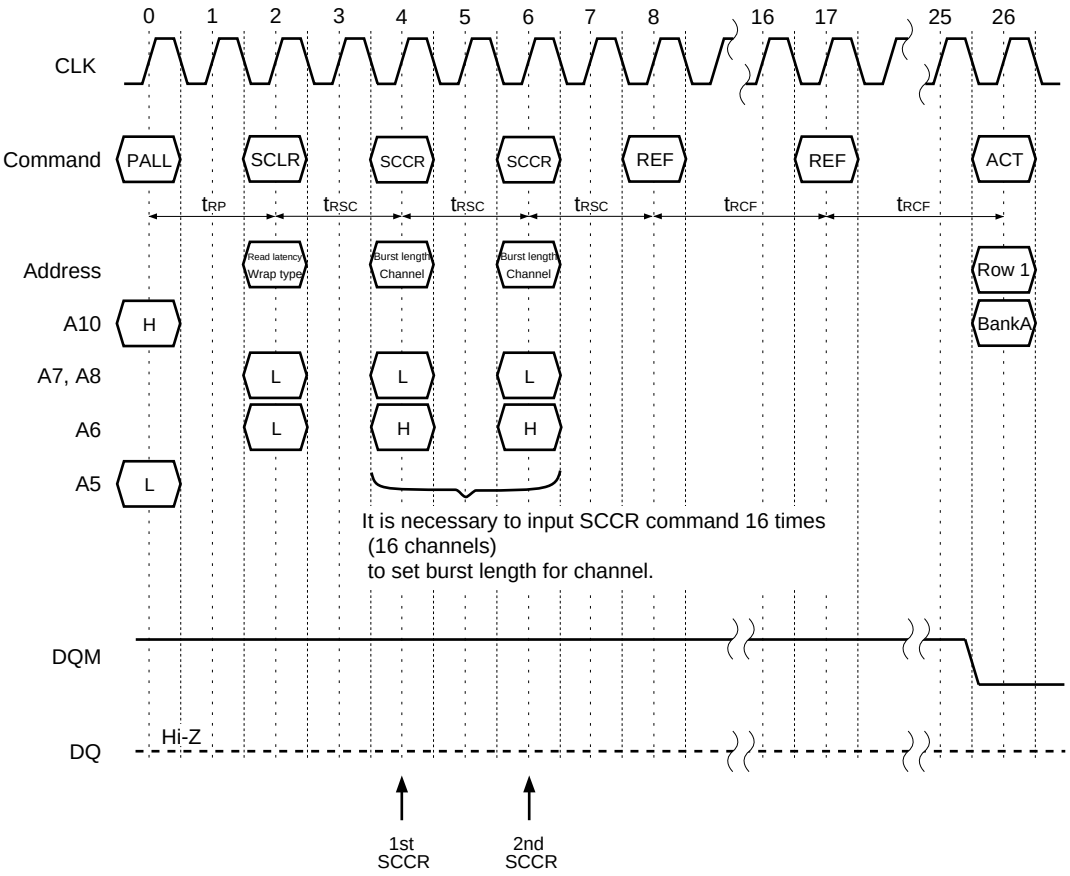
Parameter	Symbol	-A75		-A10		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
READ/WRITE to READ/WRITE Command delay time	t_{CCD}	7.5	–	10	–	ns	

AC characteristics (Background to Foreground operation)
(after same channel Prefetch/Restore)

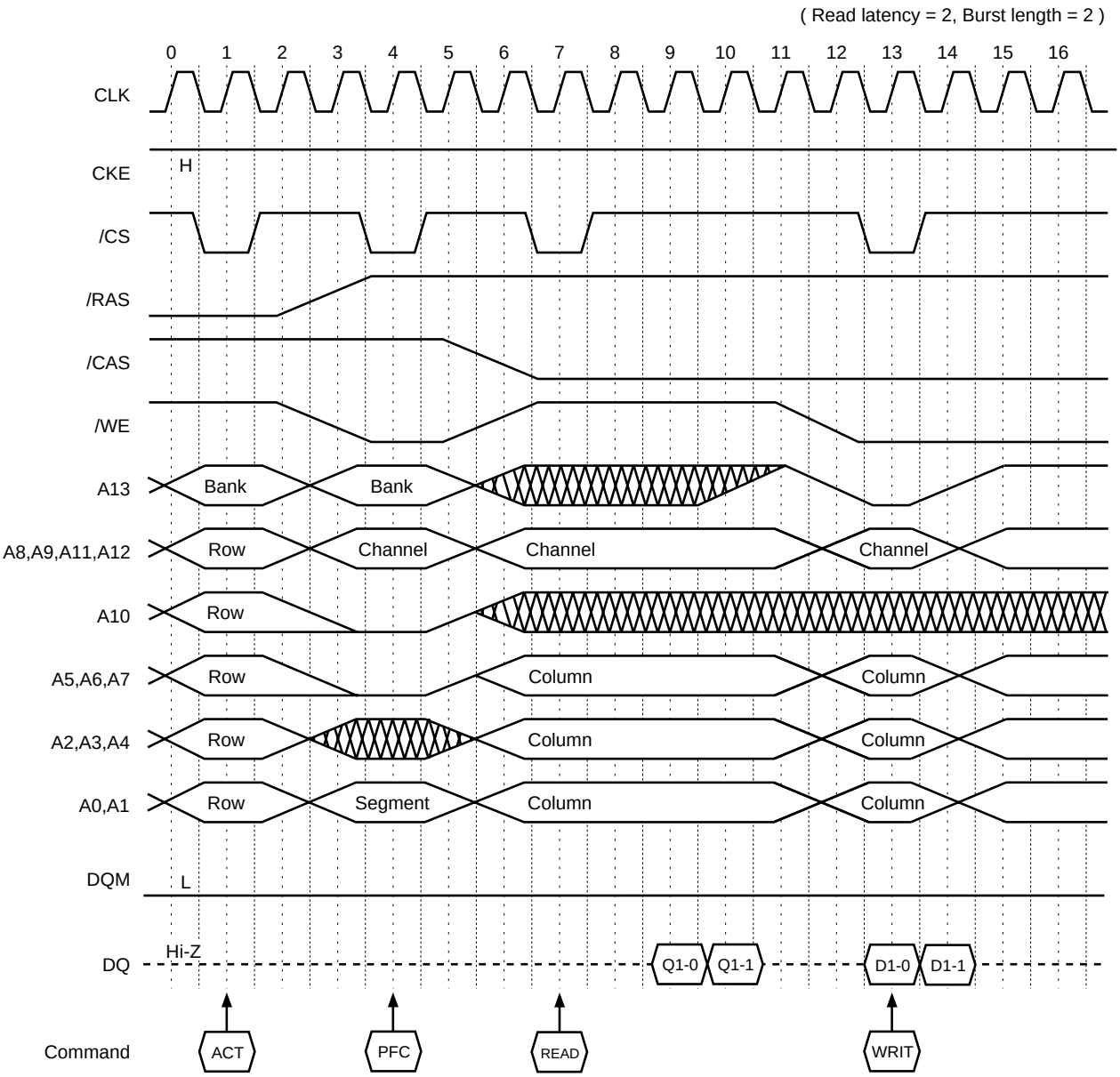
Parameter	Symbol	-A75		-A10		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
PFC/PFCA to READ/WRITE Command delay time	t_{PCD}	15	–	20	–	ns	
ACT(R) to READ/WRITE Command delay time	t_{RCD}	30	–	40	–	ns	1

Note1 ACT(R) command is ACT command after RST command.

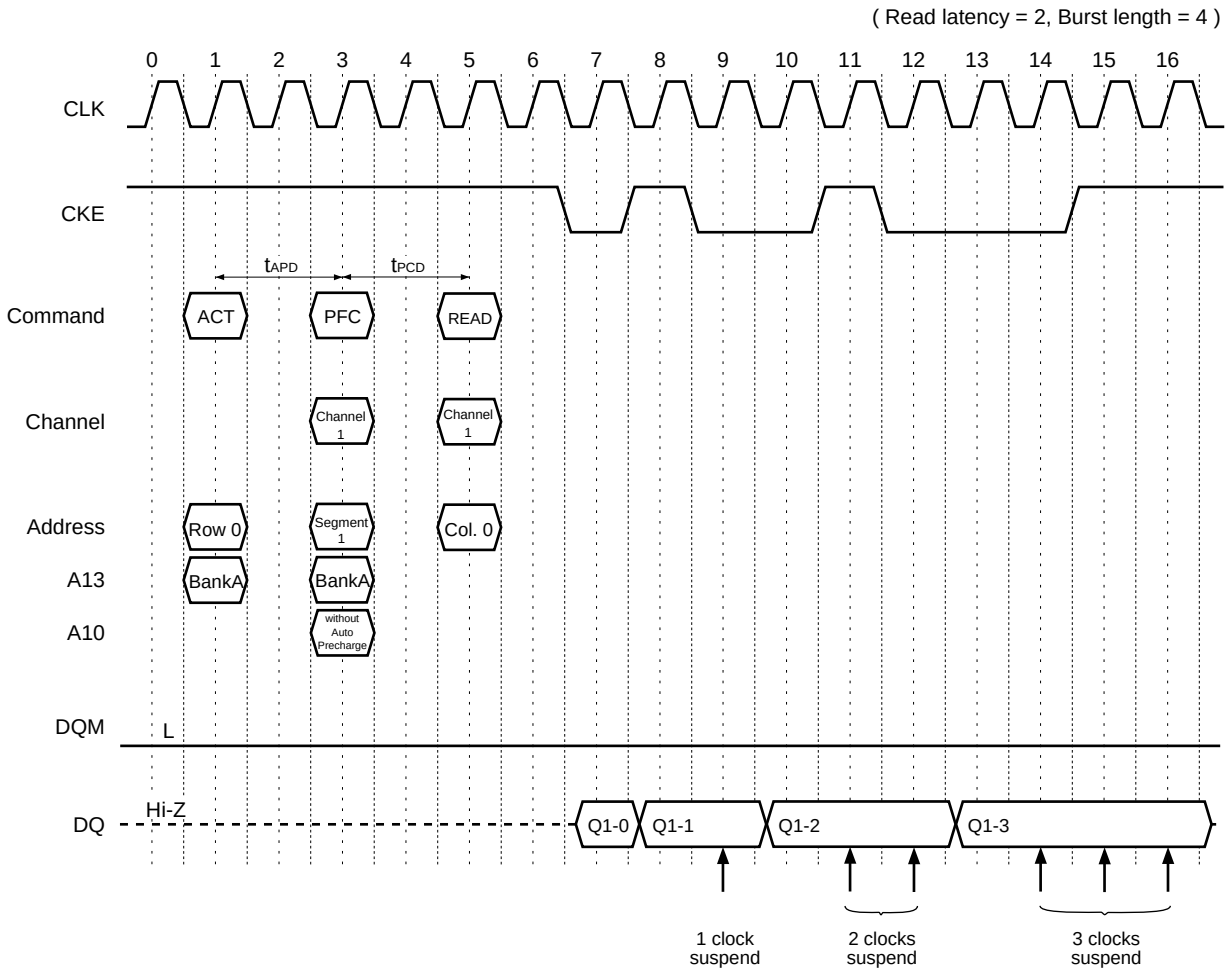
Power on Sequence and Auto Refresh



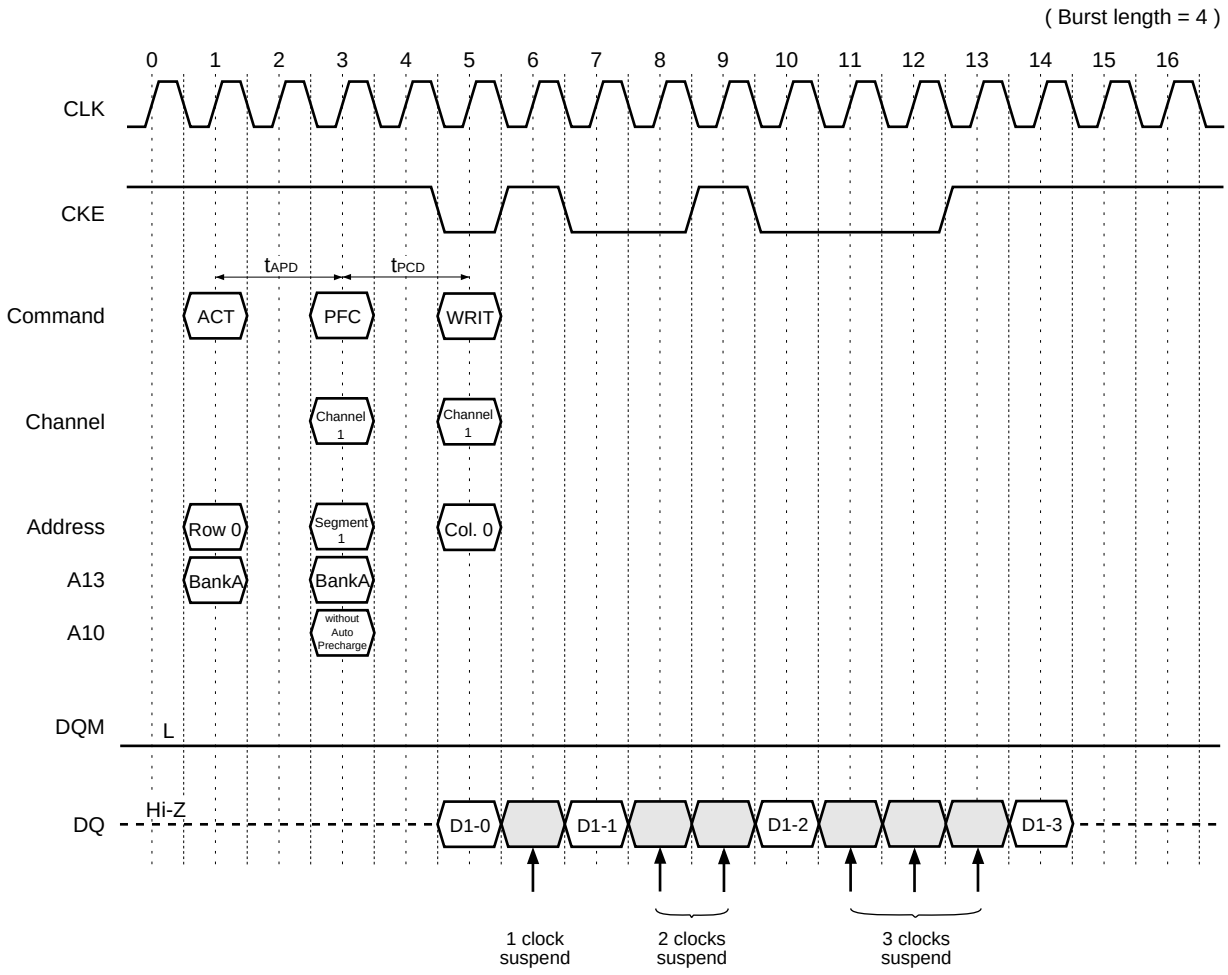
/CS Function (Only /CS signal needs to be issued at minimum rate)



Clock Suspension during Burst Read (using CKE Function)

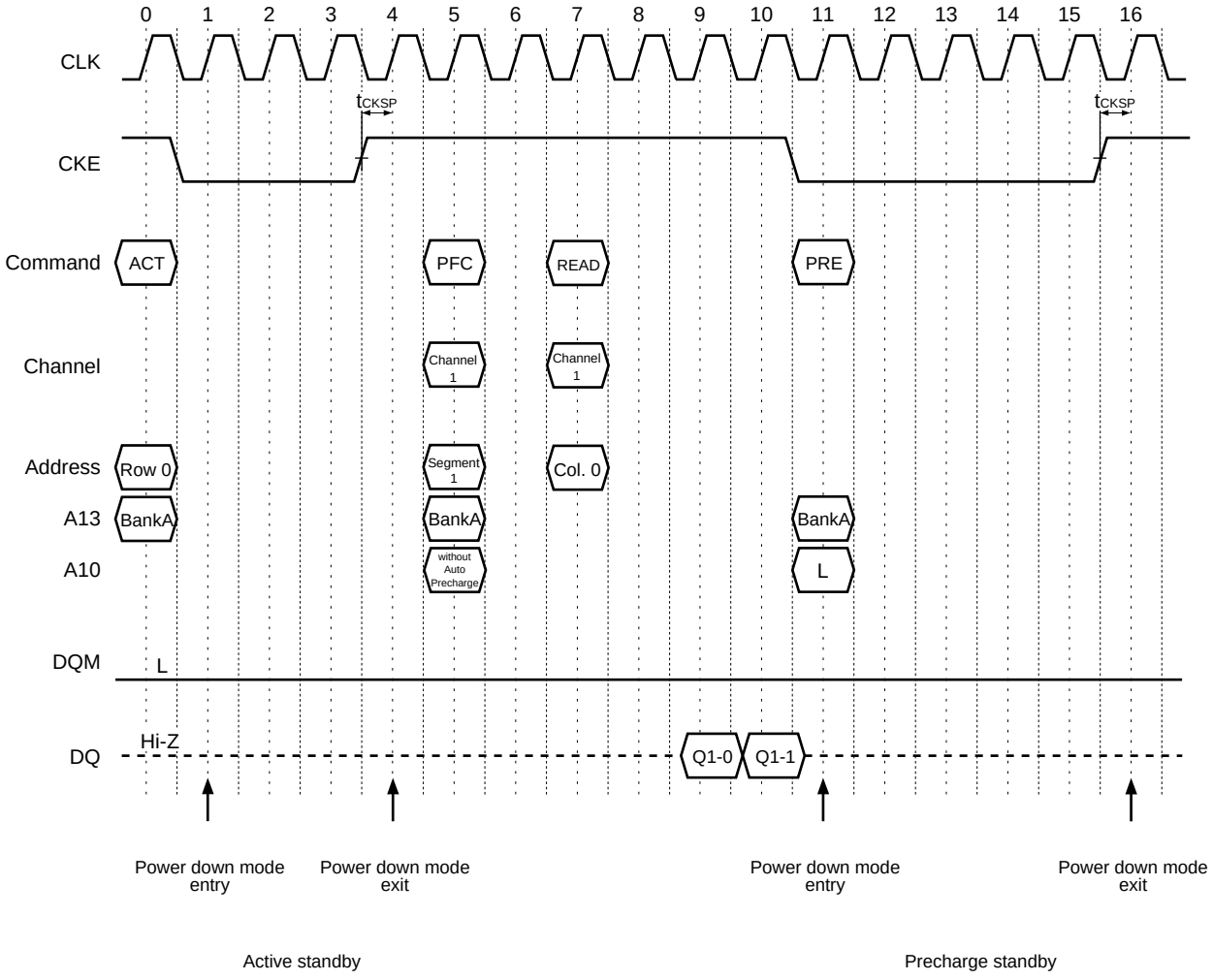


Clock Suspension during Burst Write (using CKE Function)

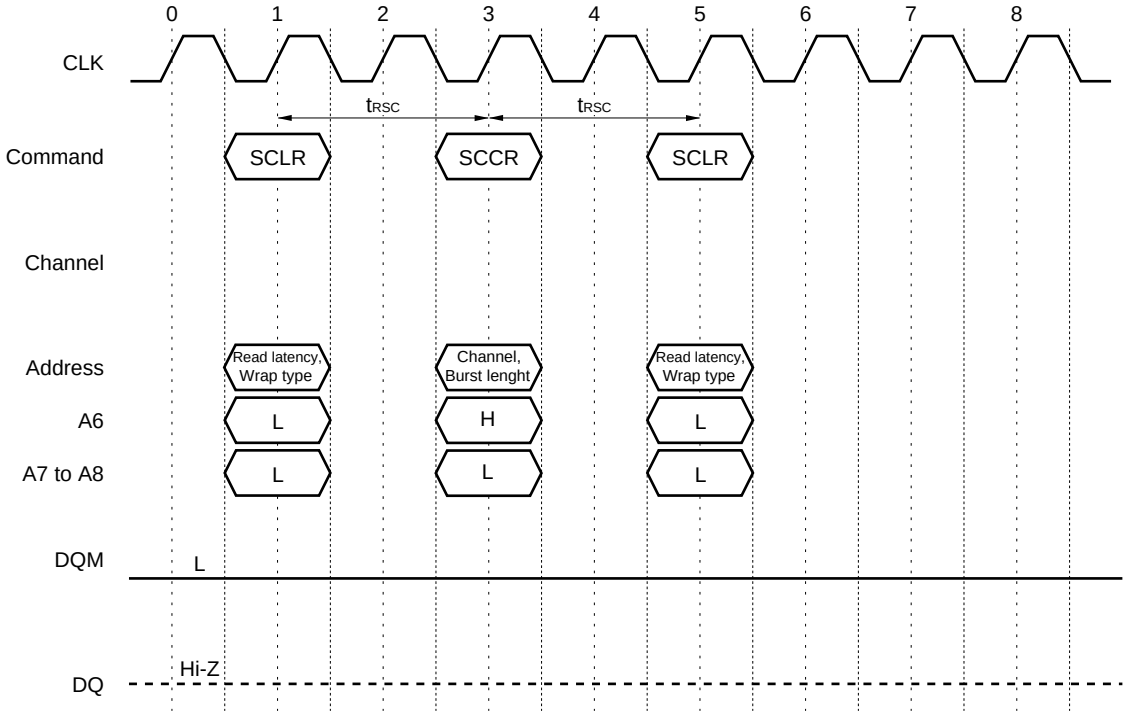


Power Down Mode

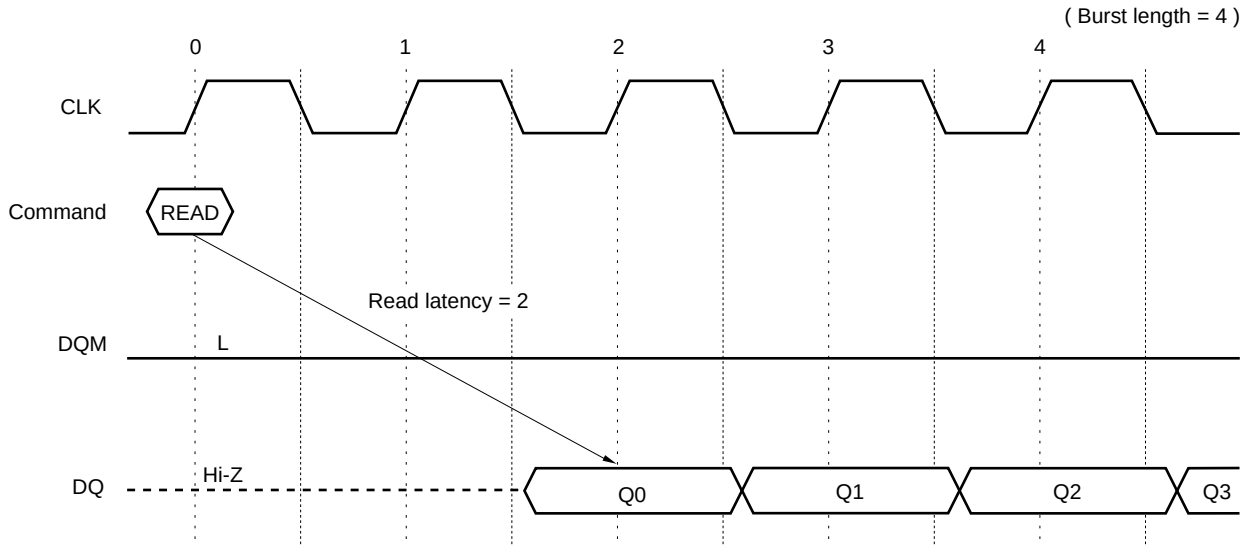
(Read latency = 2, Burst length = 2)



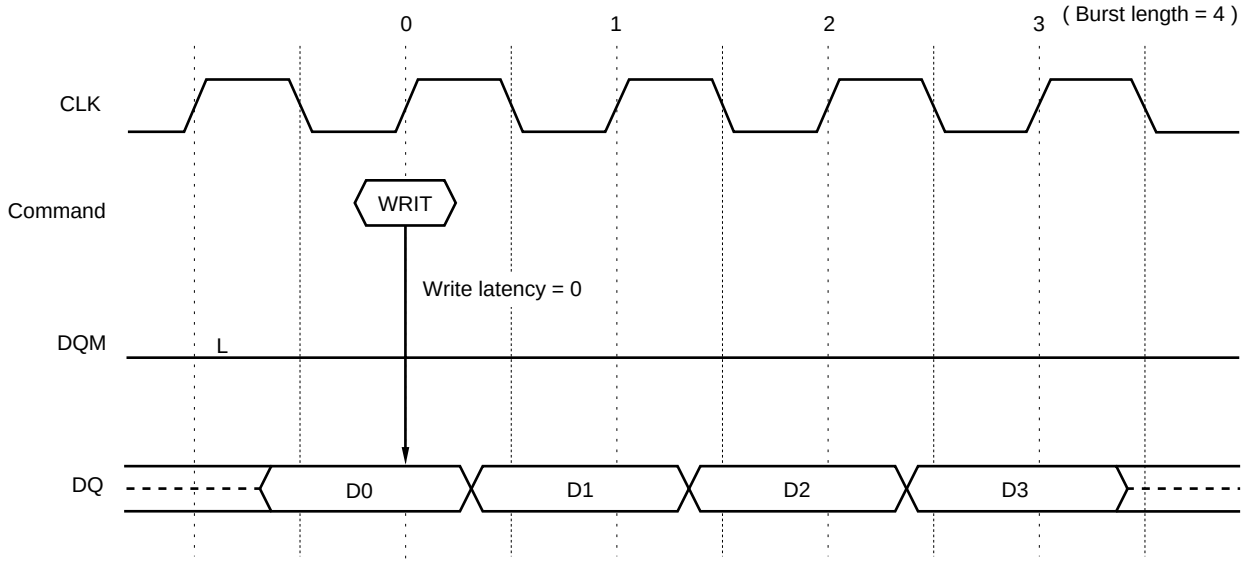
Set Register Operation



Read Operation

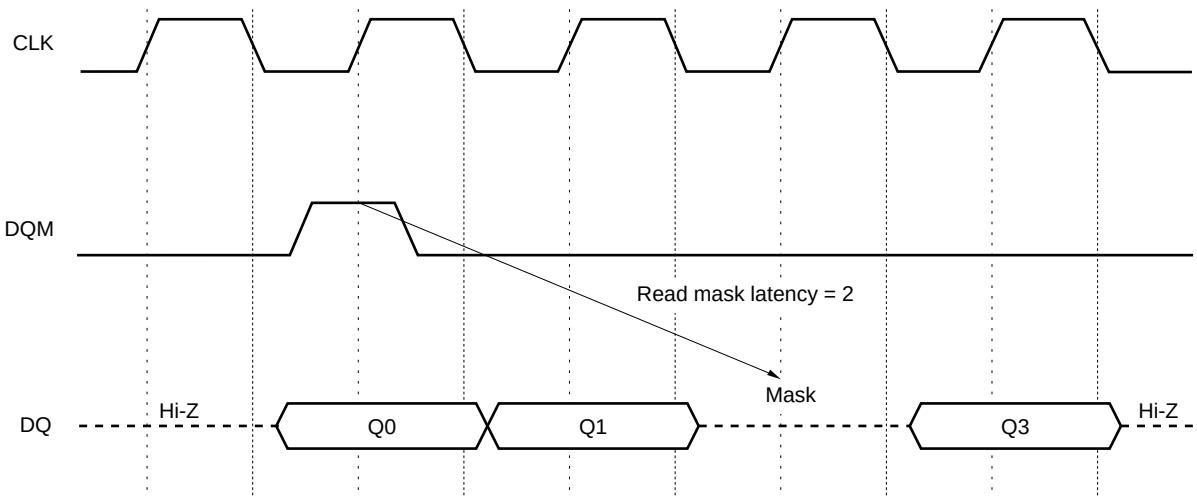


Write Operation



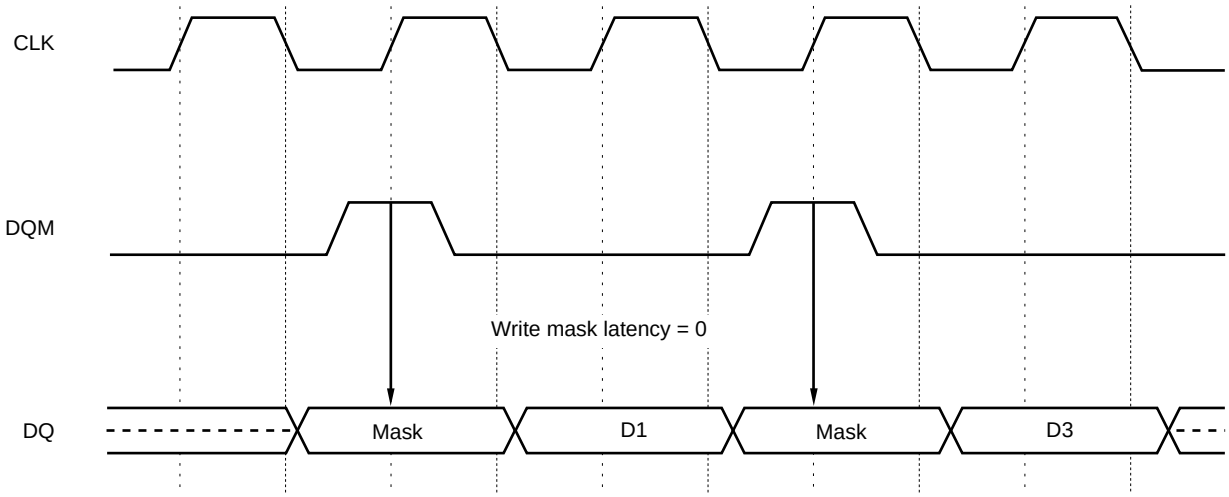
DQM Operation in READ

(Burst length = 4)



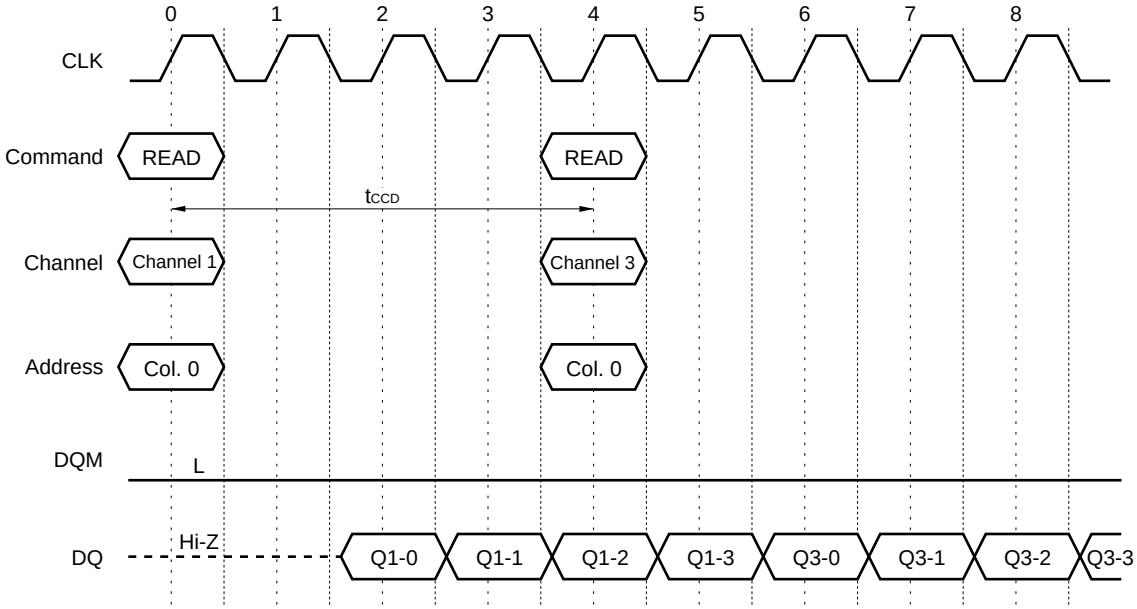
DQM Operation in WRITE

(Burst length = 4)



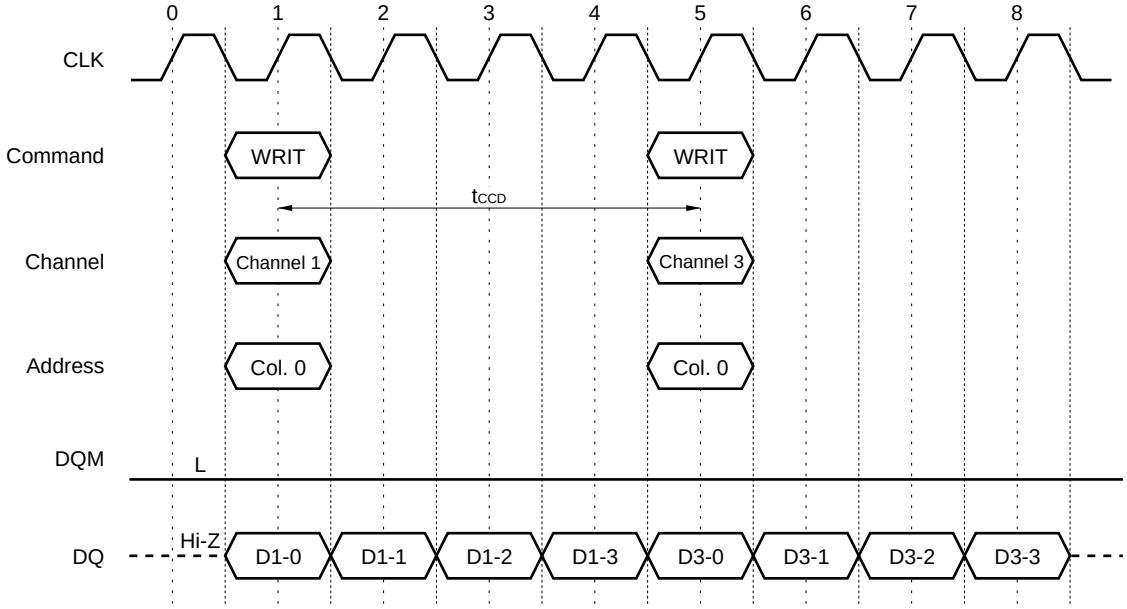
Read to Read Operation

(Read latency = 2, Burst length = 4)



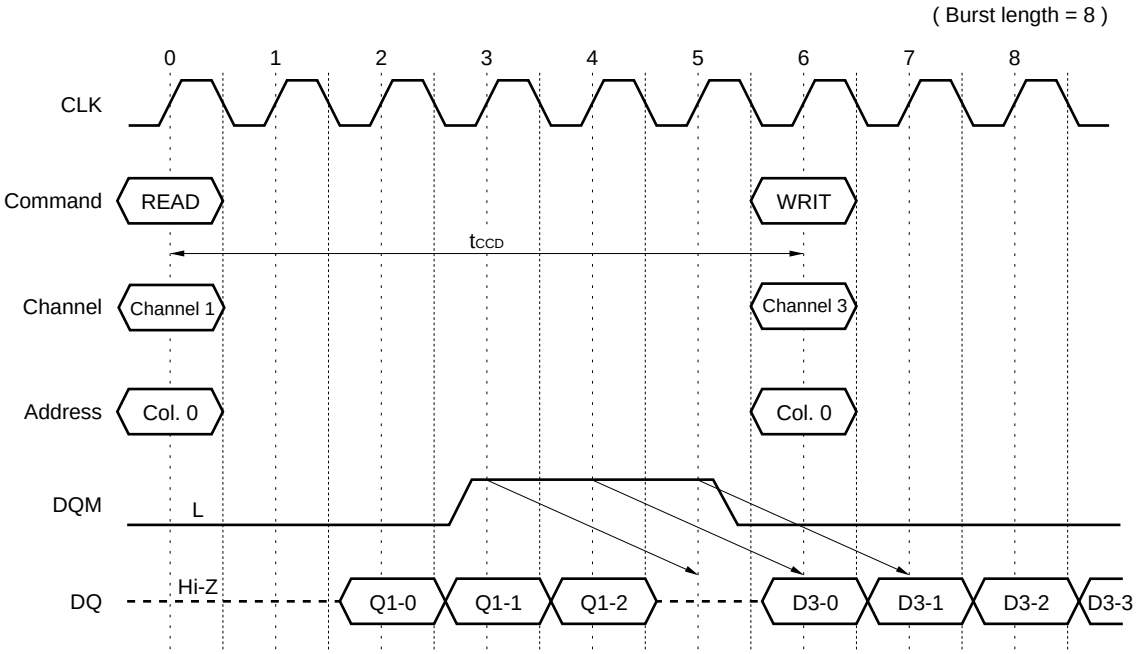
Write to Write Operation

(Burst length = 4)

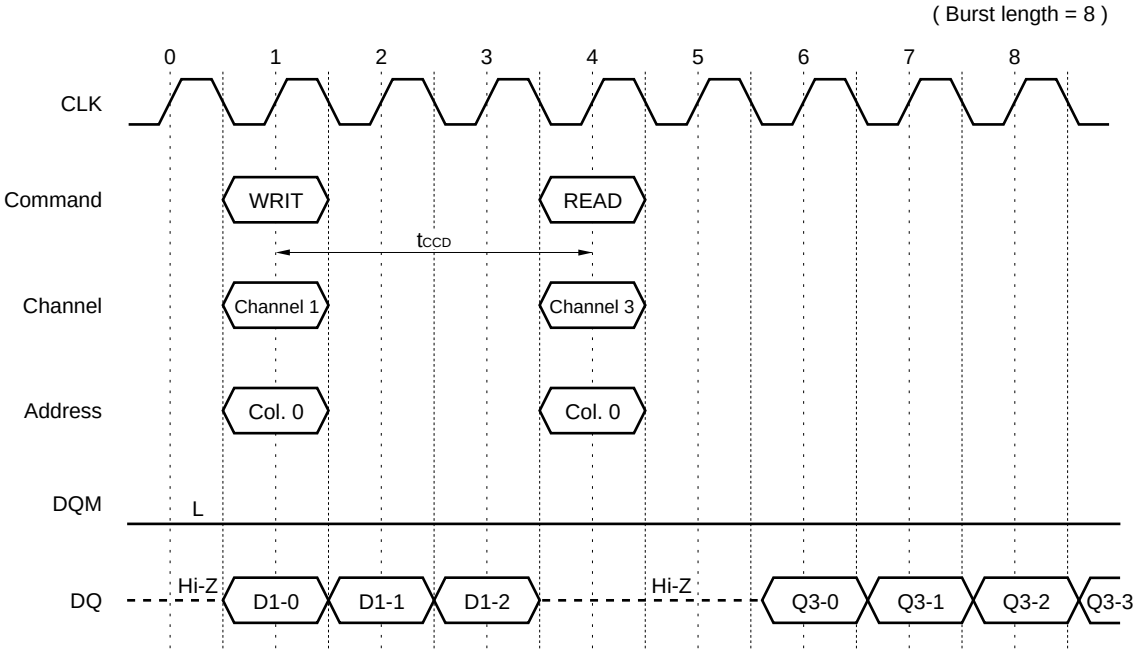


★

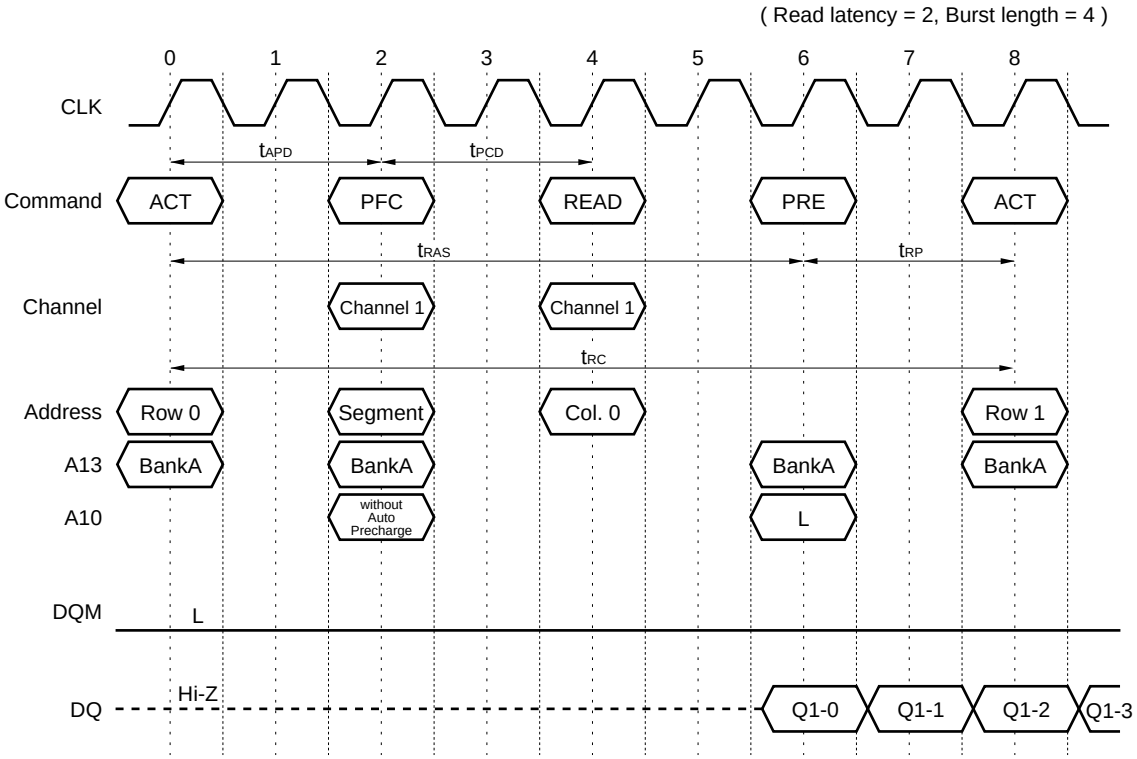
Read to Write Operation



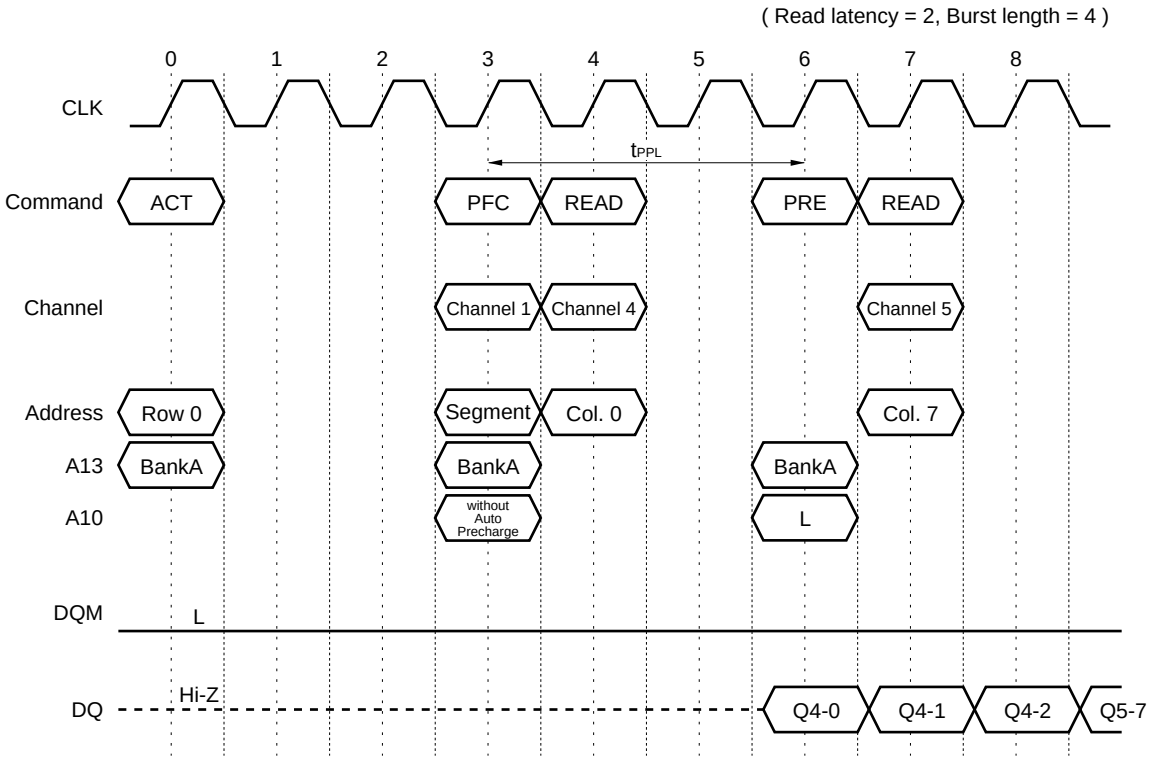
Write to Read Operation



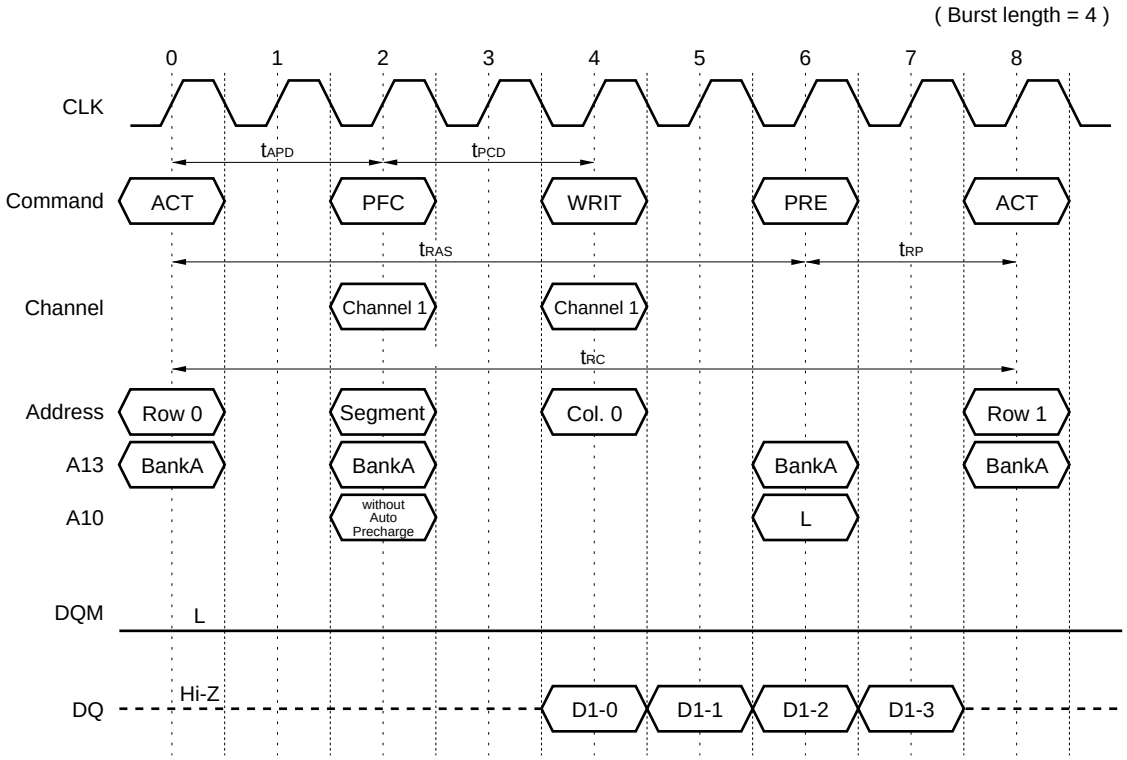
Prefetch to Read Operation without Auto Precharge (Same Channel Read)



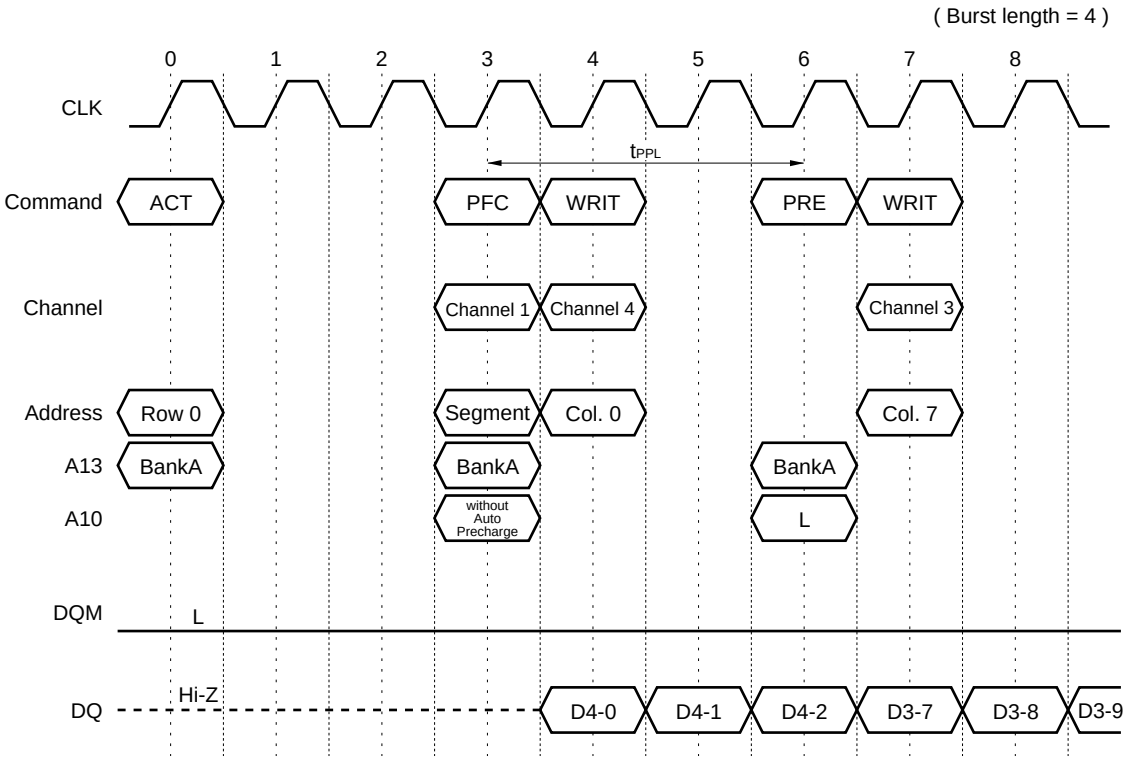
Prefetch to Read Operation without Auto Precharge (Other Channel Read)



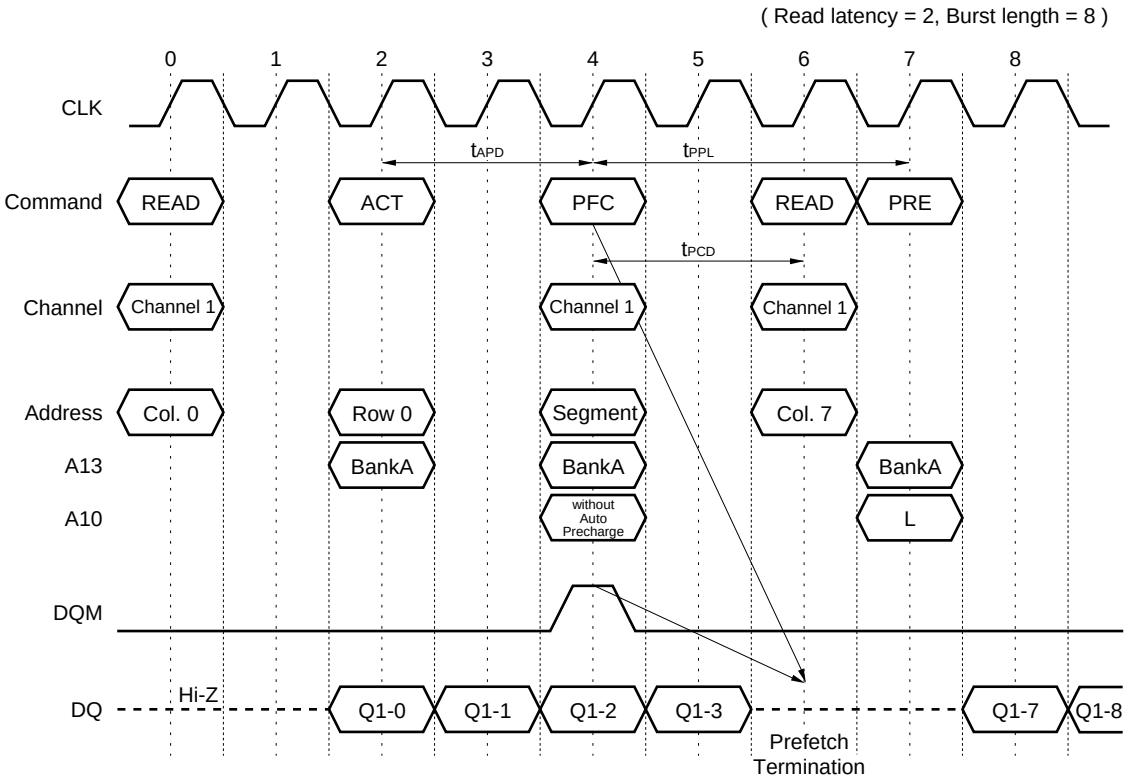
Prefetch to Write Operation without Auto Precharge (Same Channel Write)



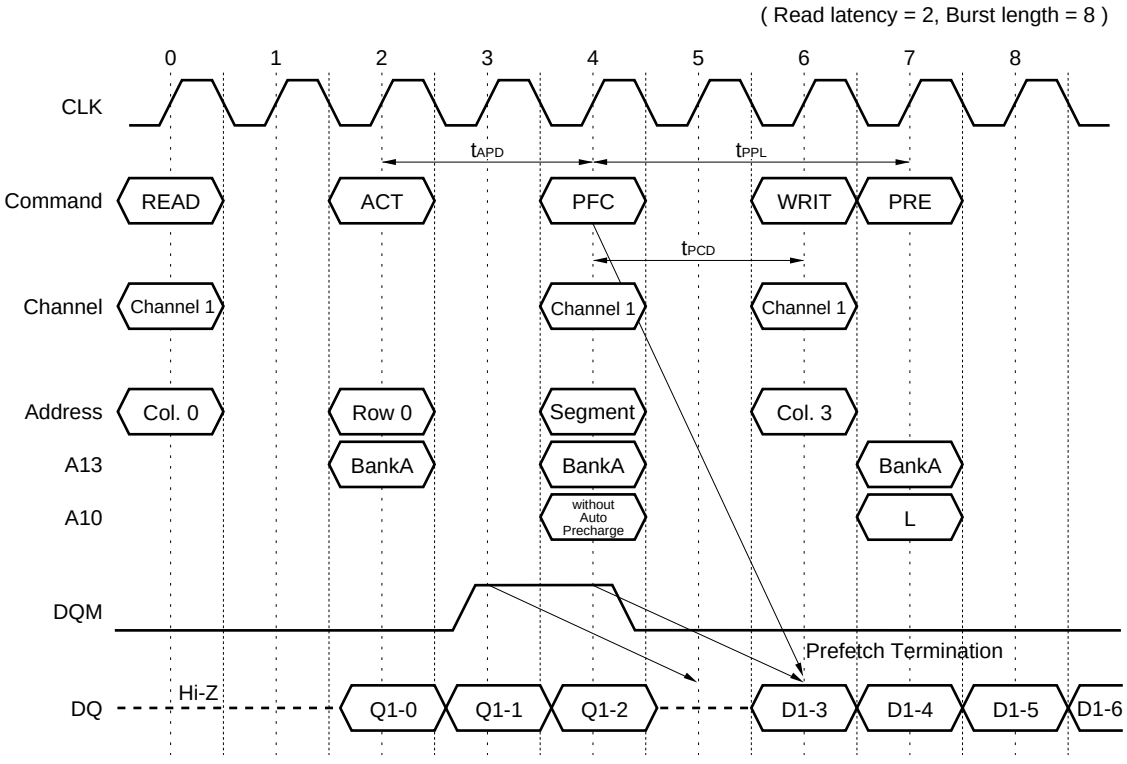
Prefetch to Write Operation without Auto Precharge (Other Channel Write)



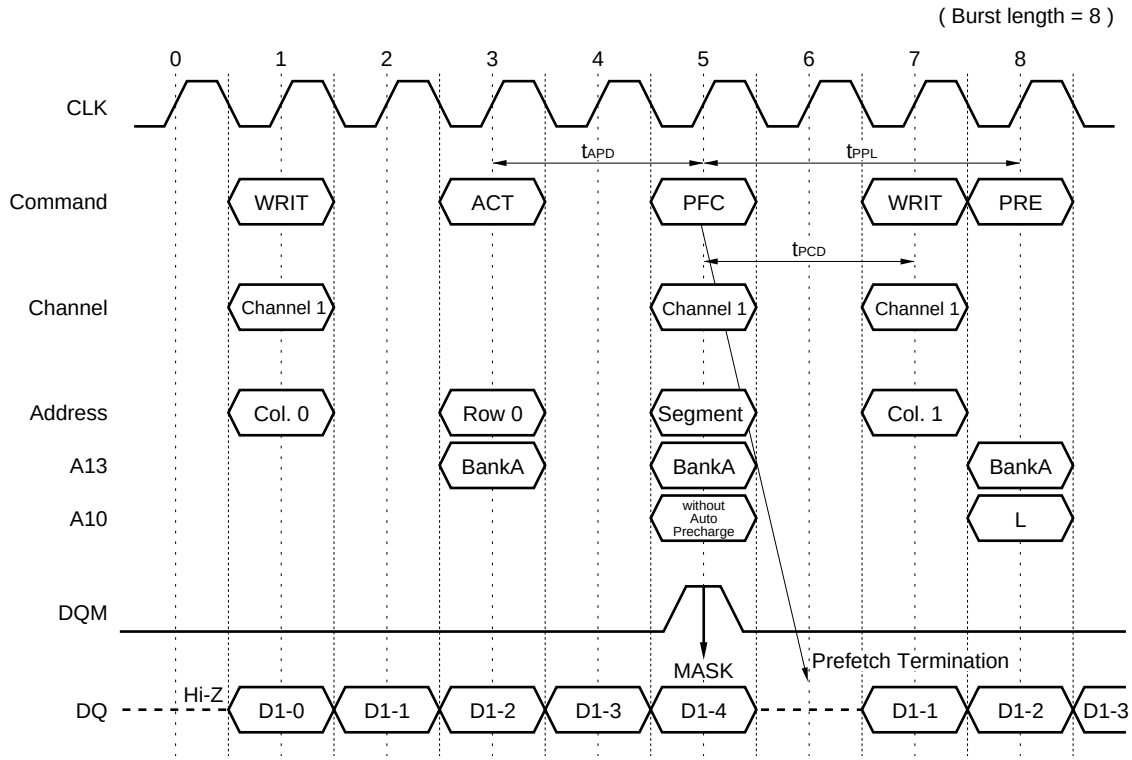
Read to Prefetch to Read Operation without Auto Precharge (Same Channel Prefetch)



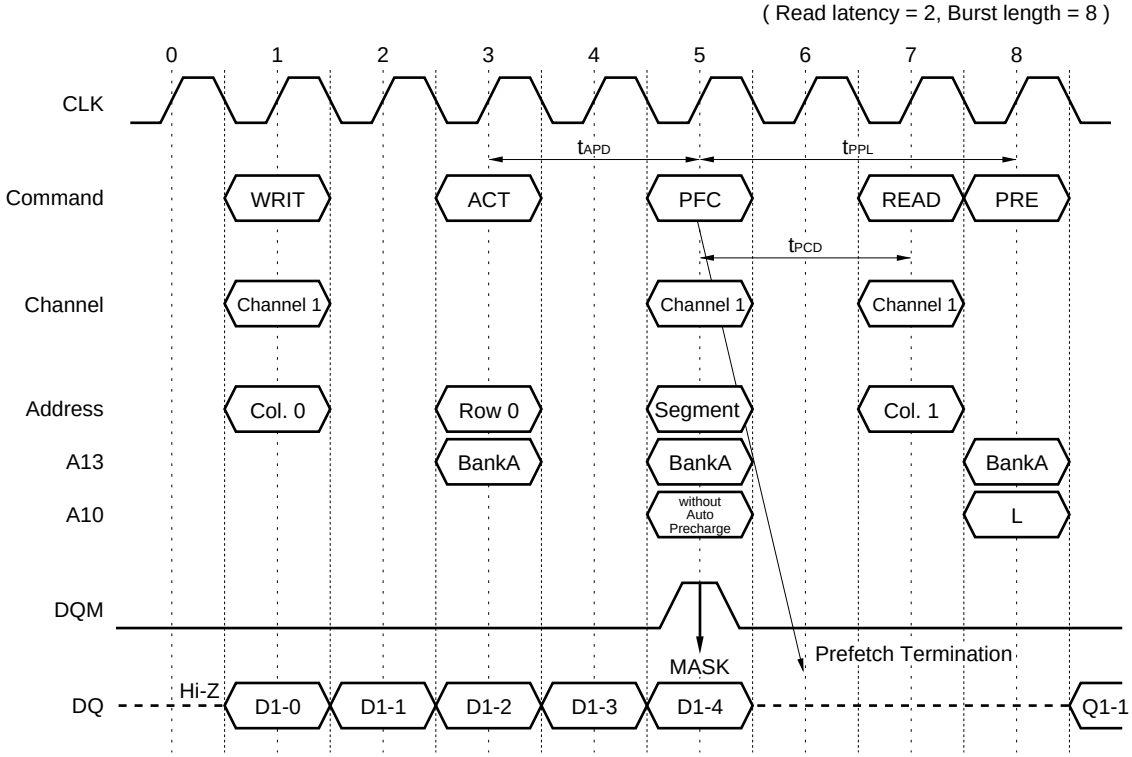
Read to Prefetch to Write Operation without Auto Precharge (Same Channel Prefetch)



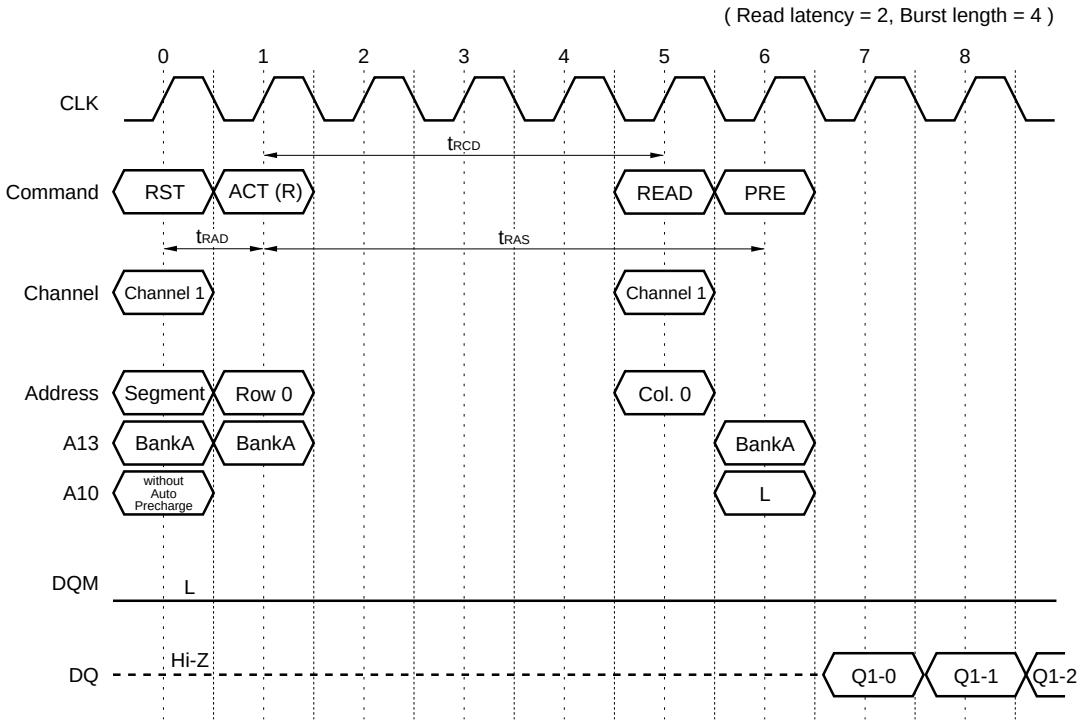
Write to Prefetch to Write Operation without Auto Precharge (Same Channel Prefetch)



Write to Prefetch to Read Operation without Auto Precharge (Same Channel Prefetch)

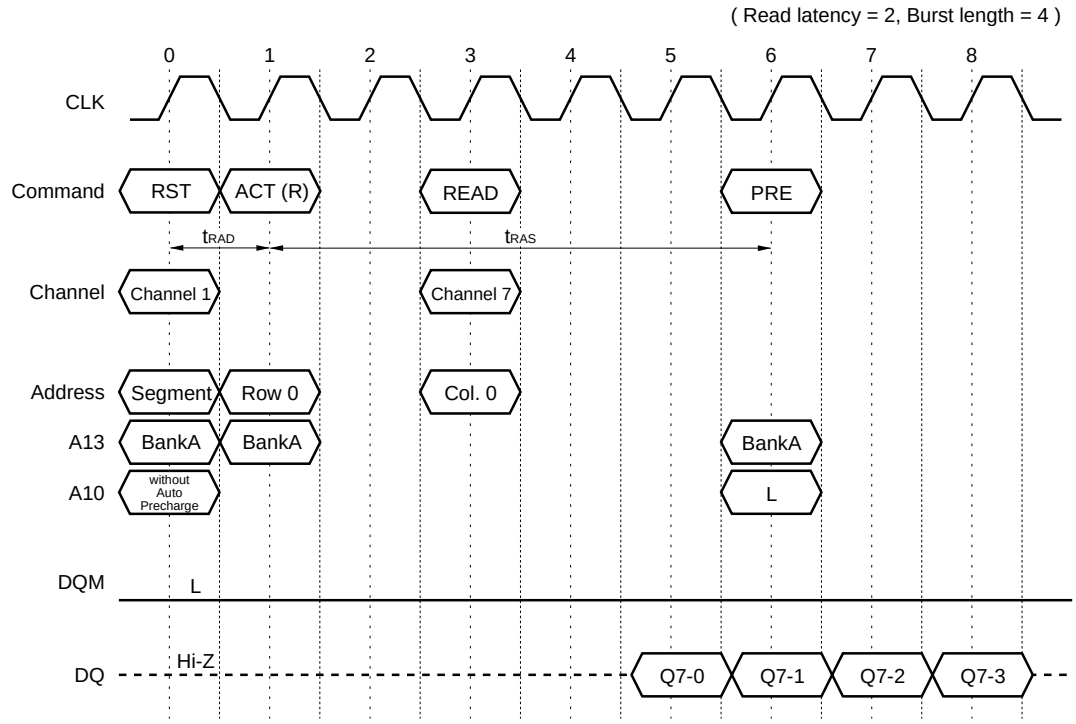


Restore to Read Operation without Auto Precharge (Same Channel Read)



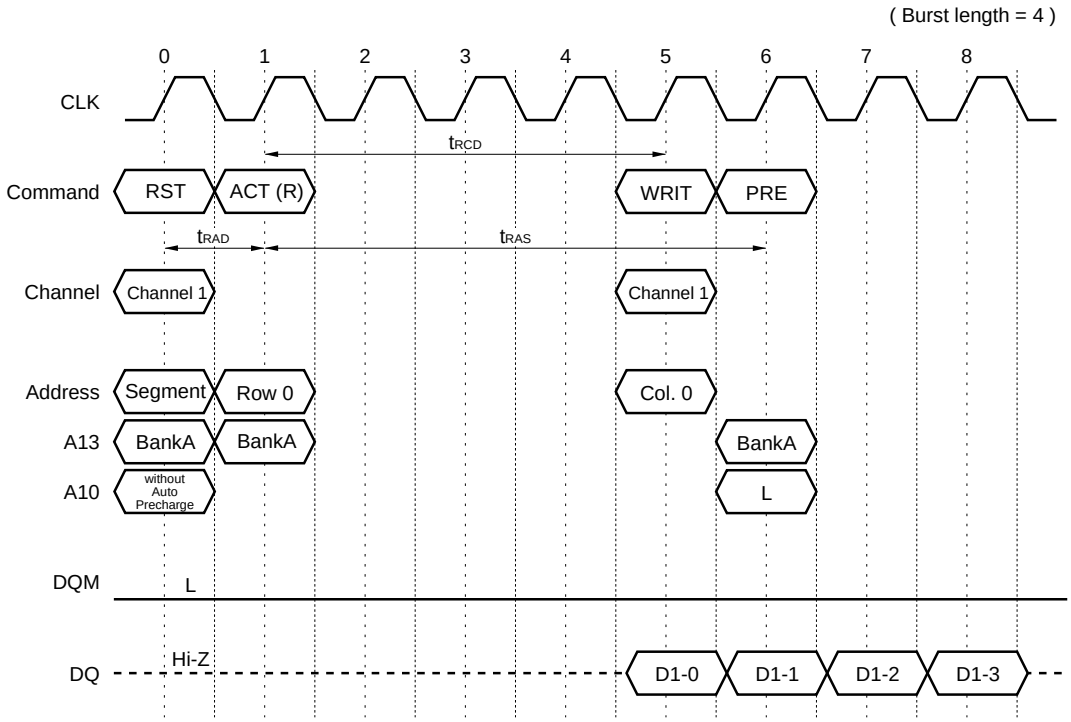
Remark ACT(R) command is ACT command after RST command.

Restore to Read Operation without Auto Precharge (Other Channel Read)



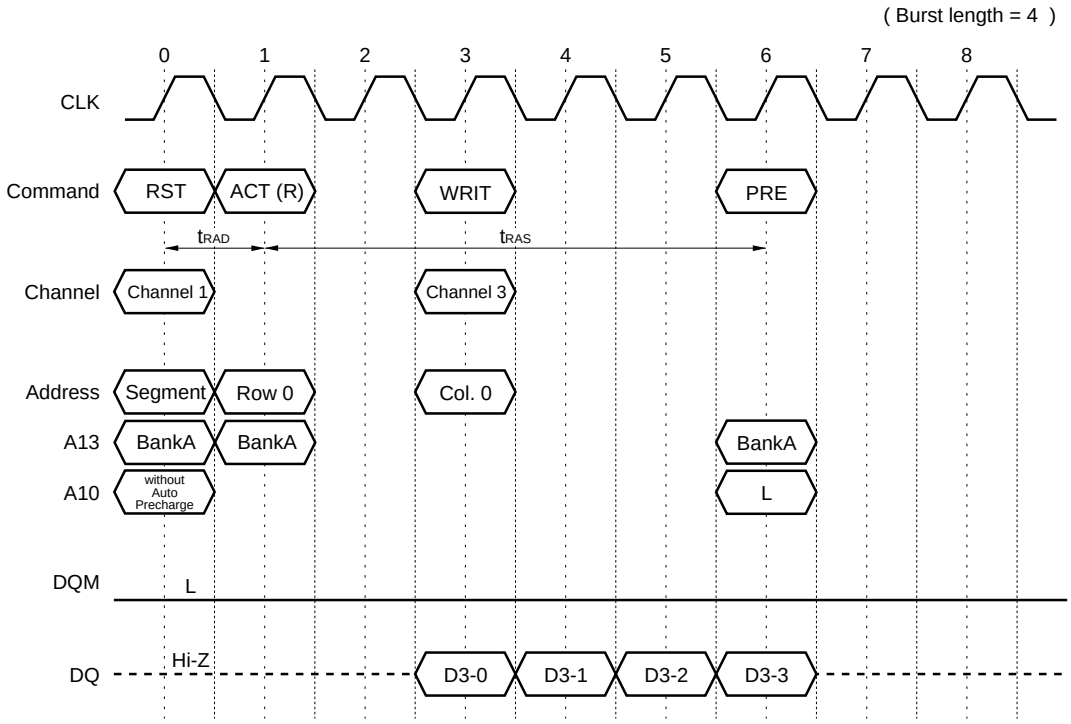
Remark ACT(R) command is ACT command after RST command.

Restore to Write Operation without Auto Precharge (Same Channel Write)



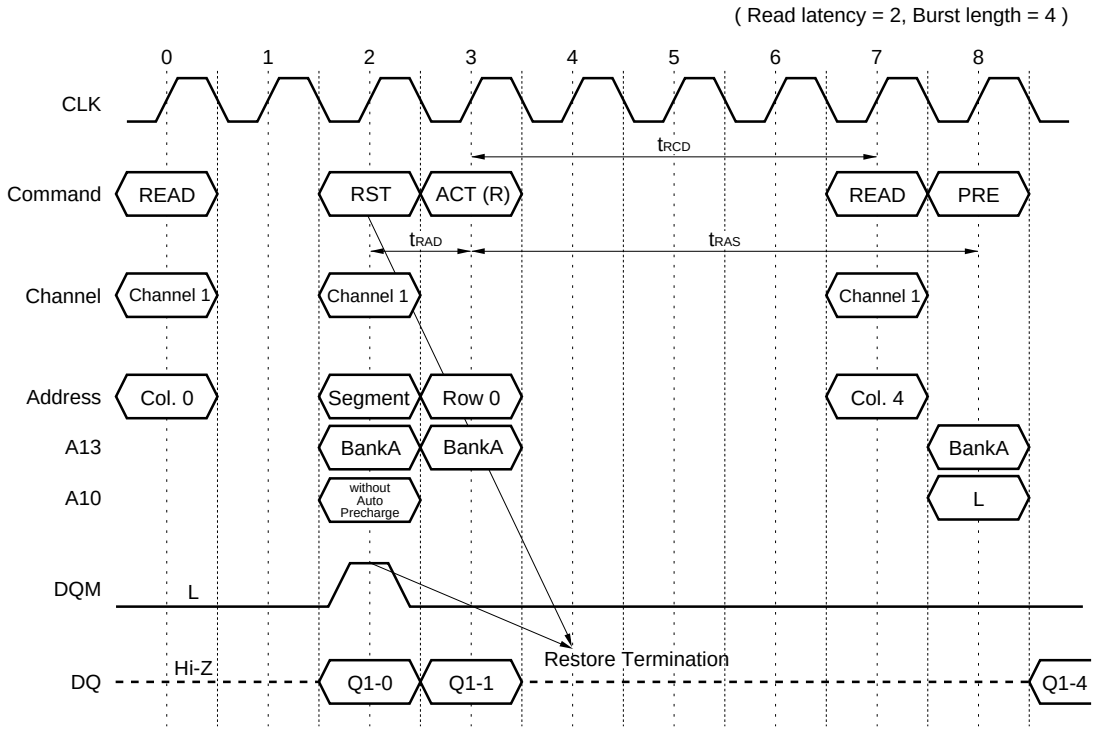
Remark ACT(R) command is ACT command after RST command.

Restore to Write Operation without Auto Precharge (Other Channel Write)



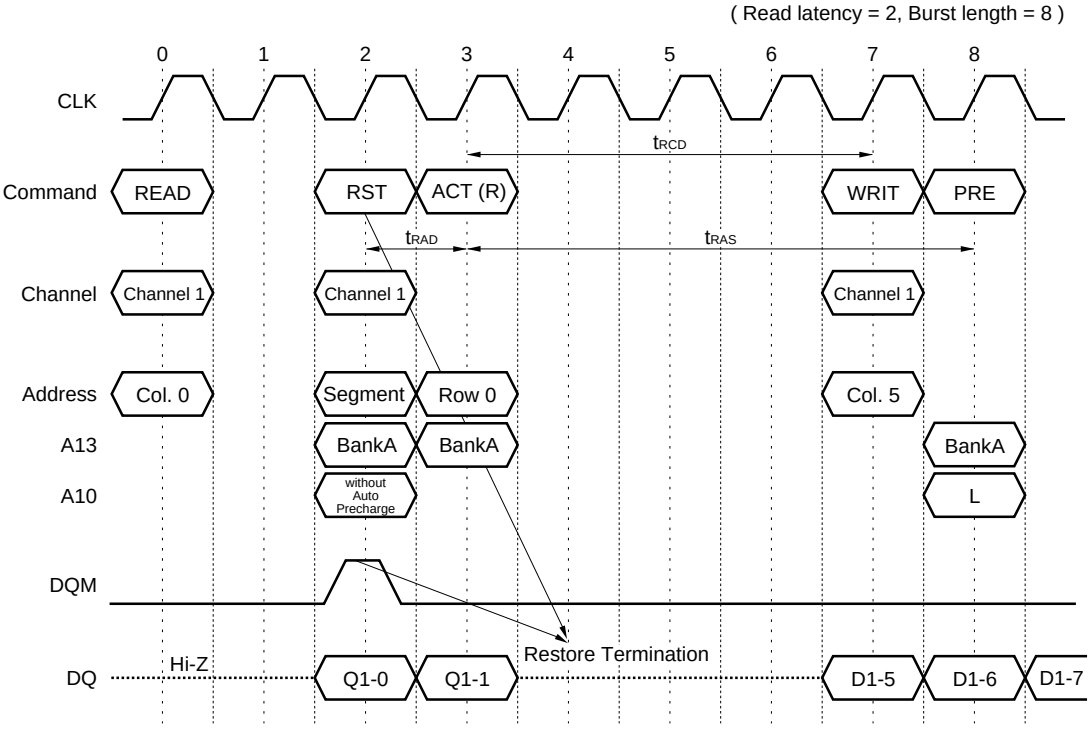
Remark ACT(R) command is ACT command after RST command.

Read to Restore to Read Operation without Auto Precharge (Same Channel Restore)



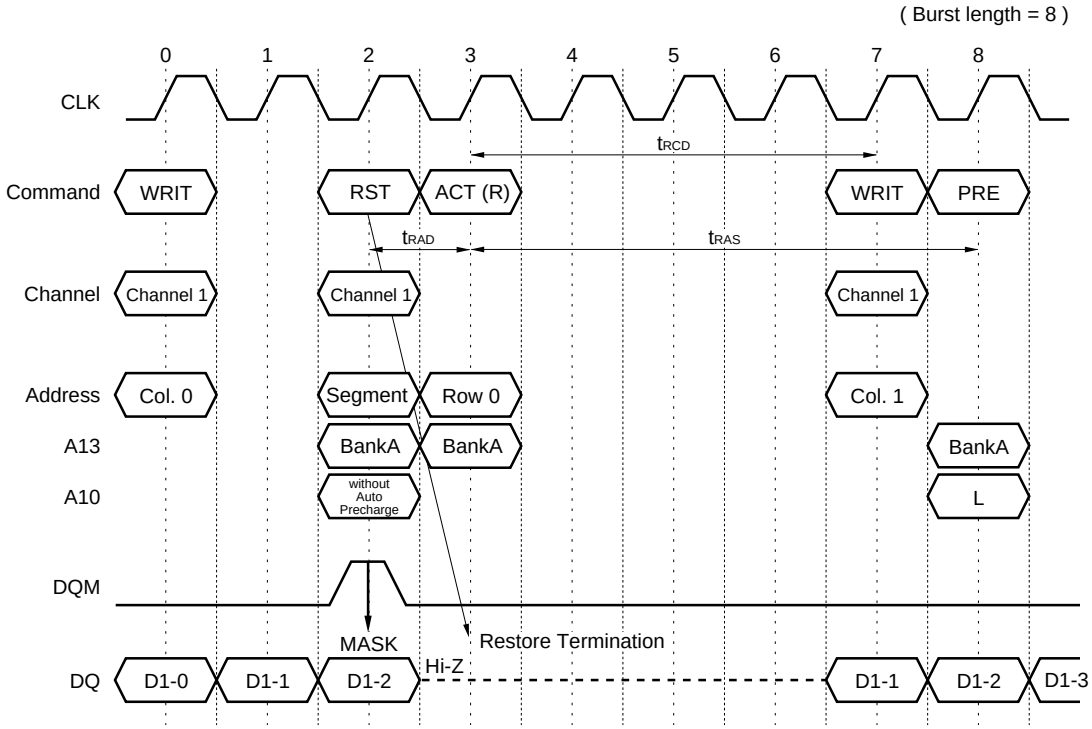
Remark ACT(R) command is ACT command after RST command.

Read to Restore to Write Operation without Auto Precharge (Same Channel Restore)



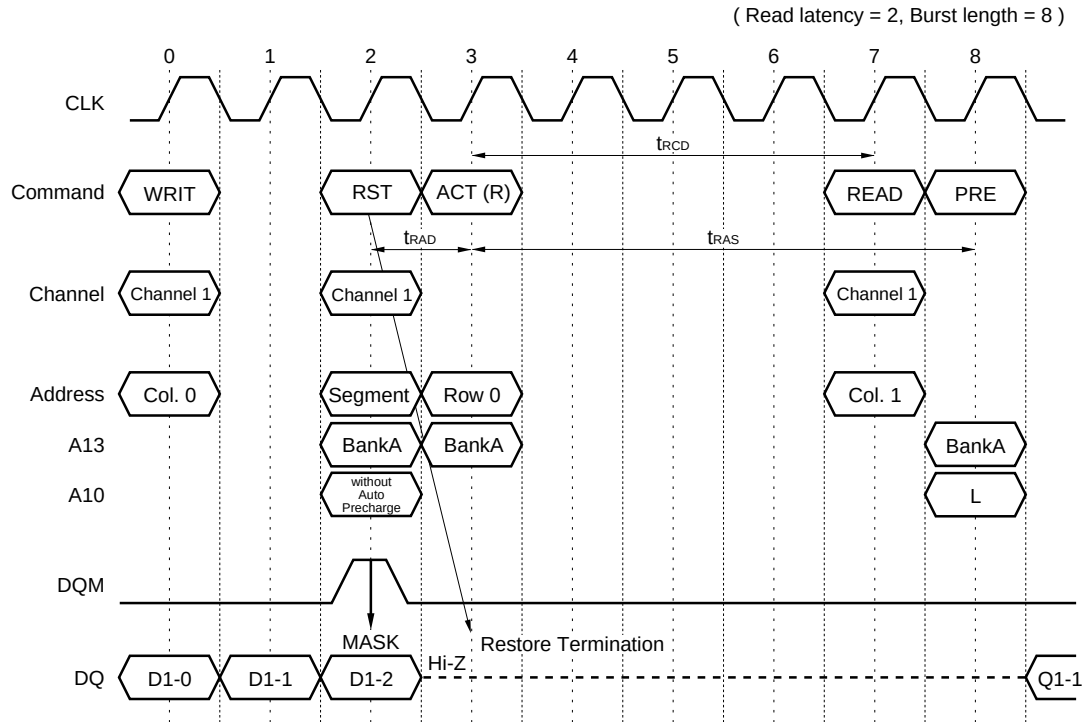
Remark ACT(R) command is ACT command after RST command.

Write to Restore to Write Operation without Auto Precharge (Same Channel Restore)



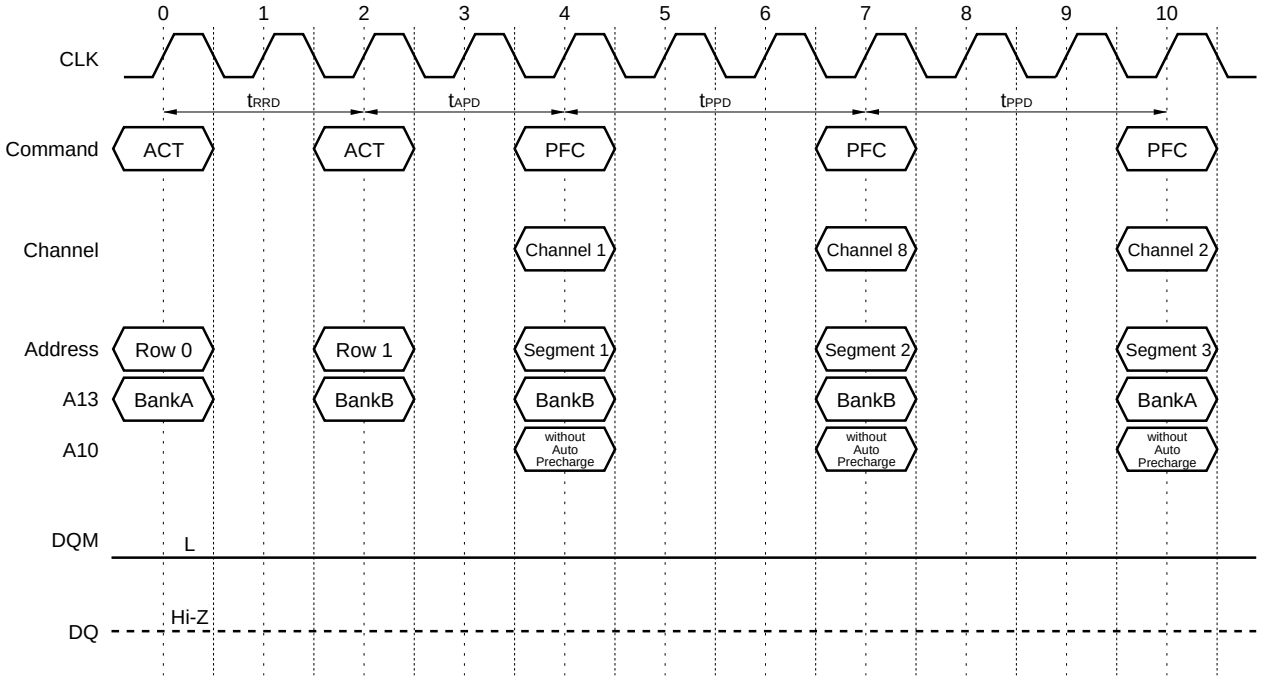
Remark ACT(R) command is ACT command after RST command.

Write to Restore to Read Operation without Auto Precharge (Same Channel Restore)

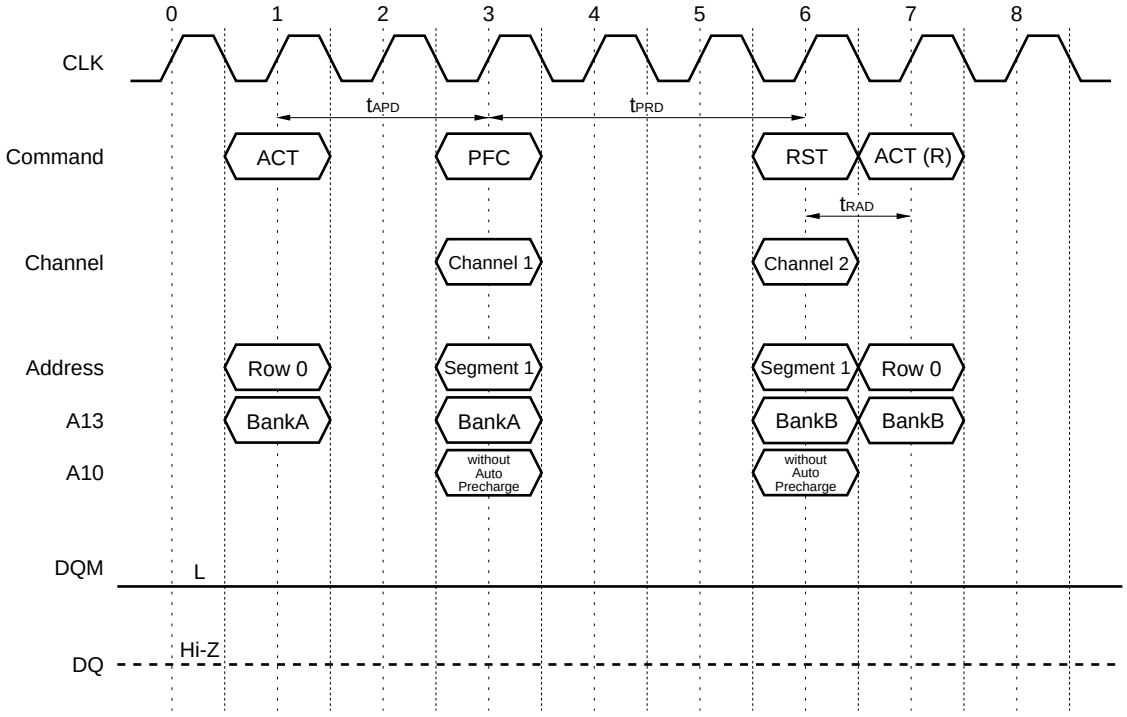


Remark ACT(R) command is ACT command after RST command.

Prefetch to Prefetch Operation without Auto Precharge

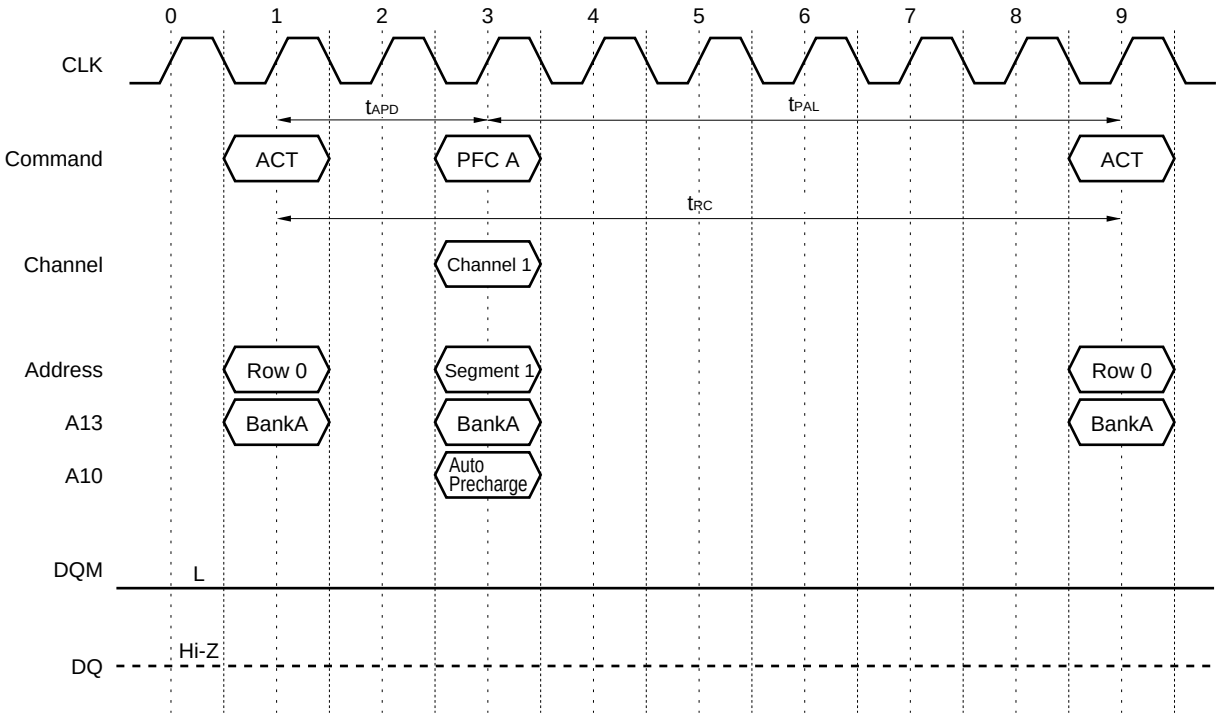


Prefetch to Restore Operation without Auto Precharge (Other Bank Restore)

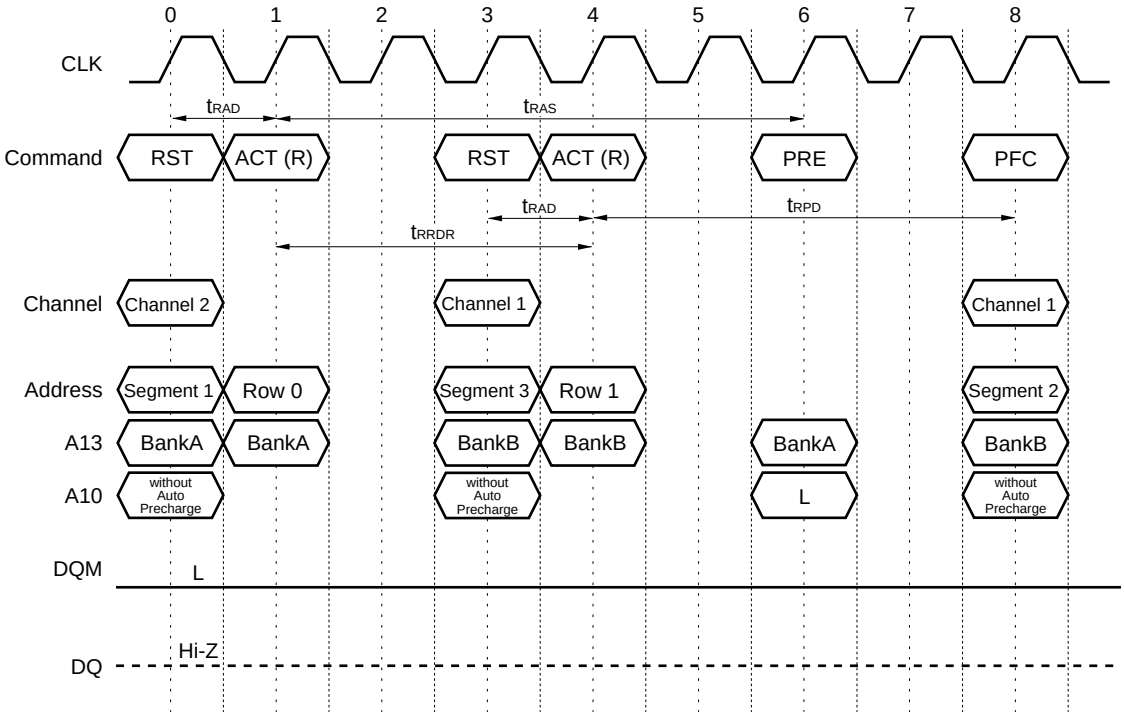


Remark ACT(R) command is ACT command after RST command.

Prefetch Operation with Auto Precharge

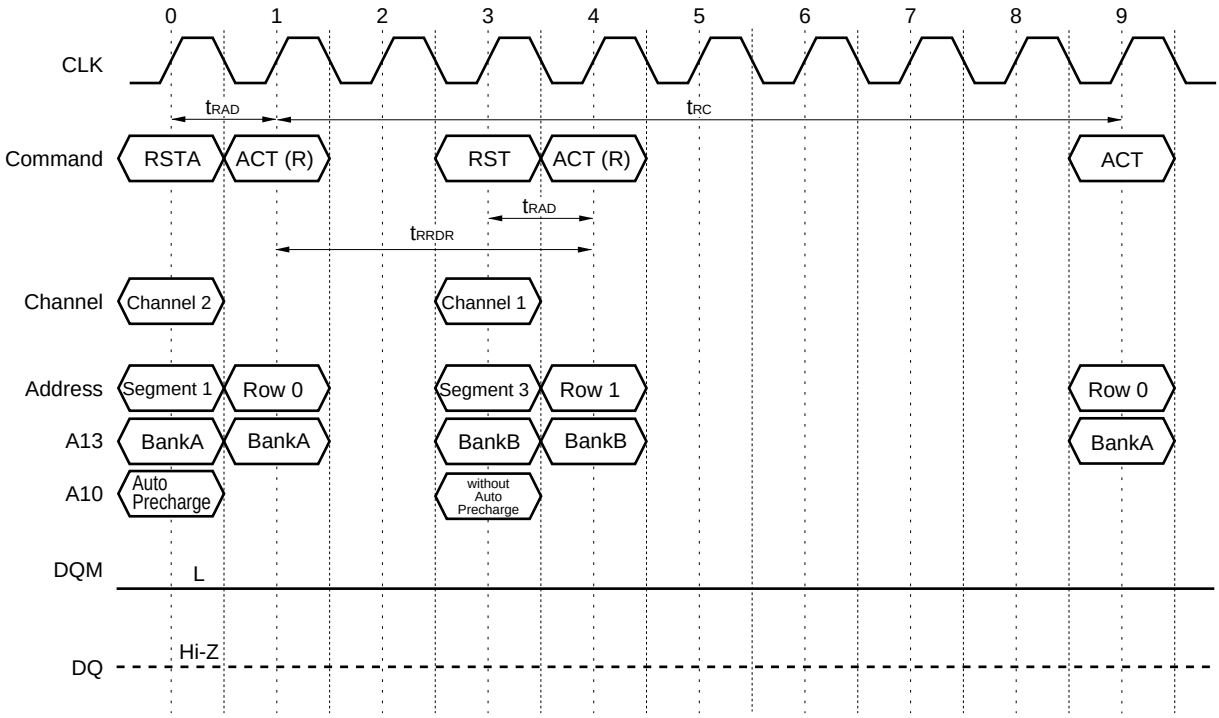


Restore to Prefetch Operation without Auto precharge



Remark ACT(R) command is ACT command after RST command.

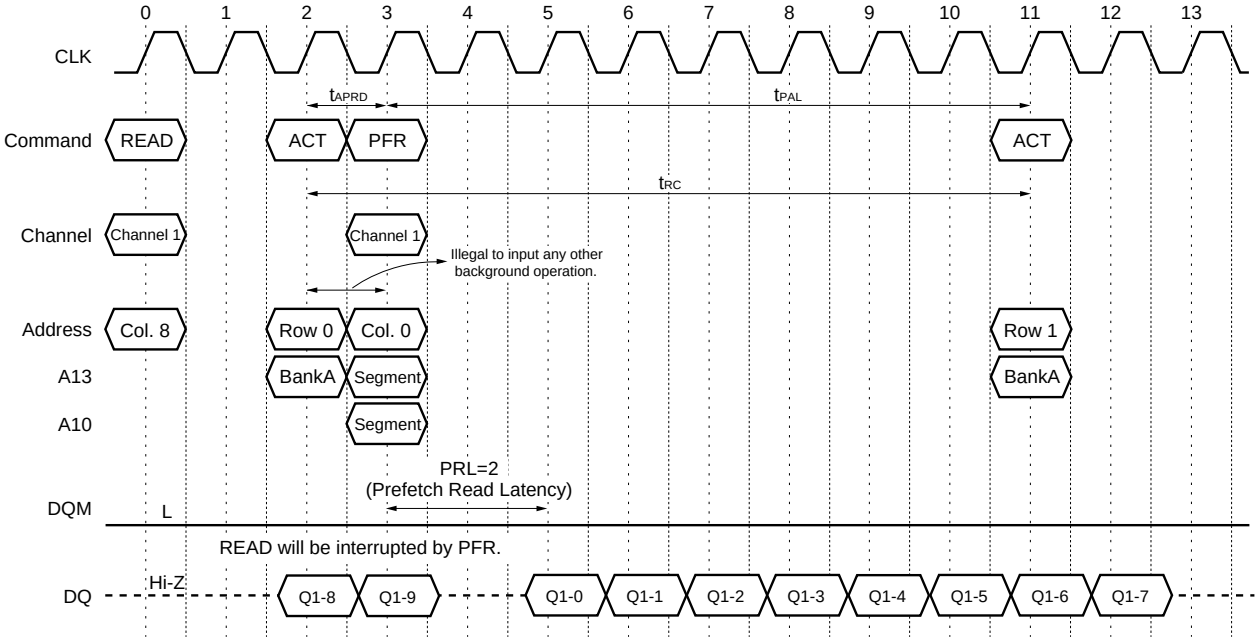
Restore Operation with Auto Precharge



Remark ACT(R) command is ACT command after RST command.

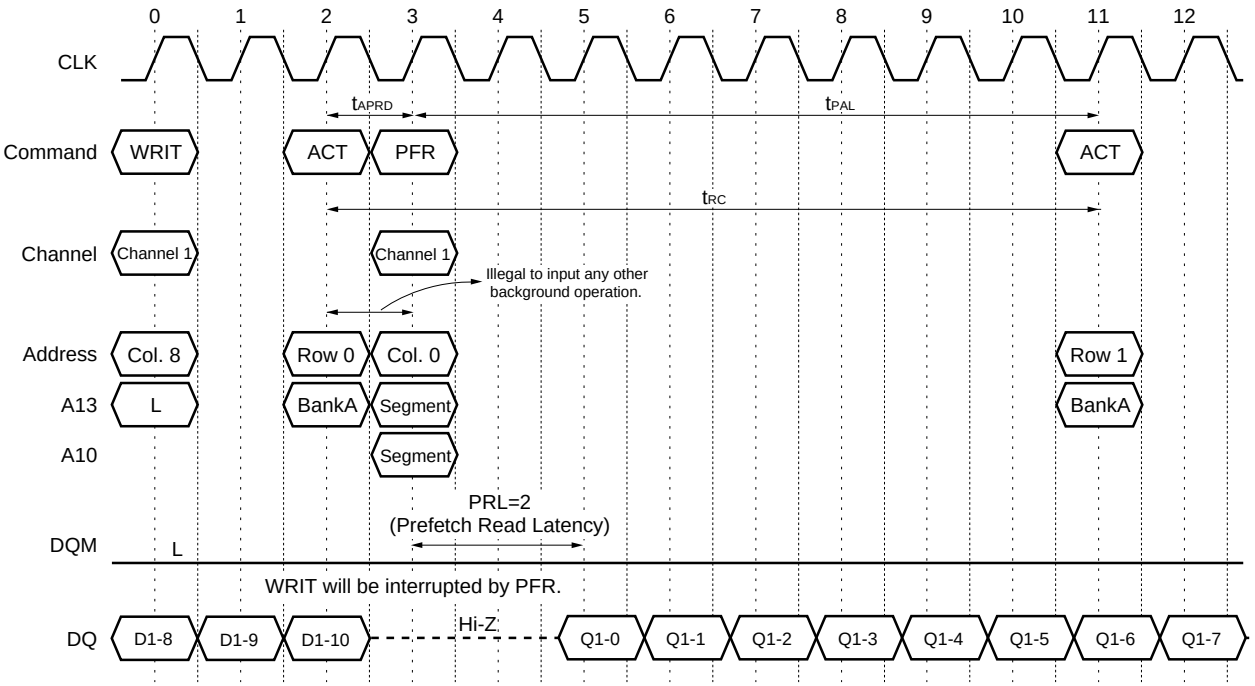
Read to Prefetch Read with Auto Precharge Operation

(Read latency = 1, Prefetch Read latency = 2, Burst length = 8)



Write to Prefetch Read with Auto Precharge Operation

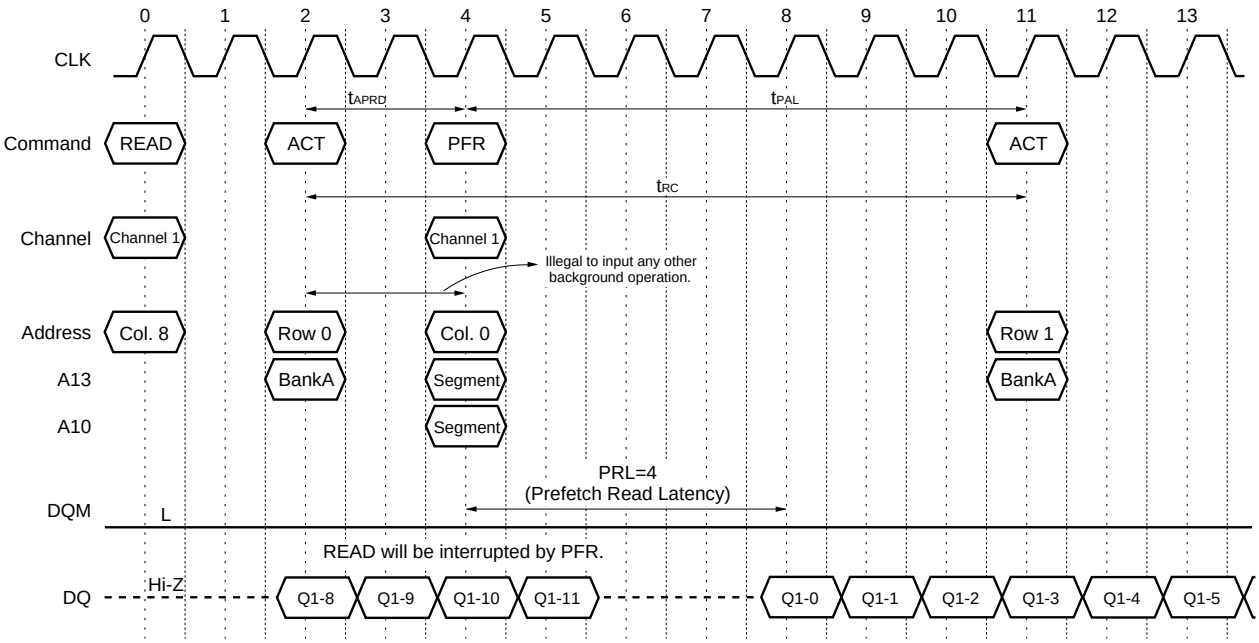
(Read latency = 1, Prefetch Read latency = 2, Burst length = 8)



★

Read to Prefetch Read with Auto Precharge Operation

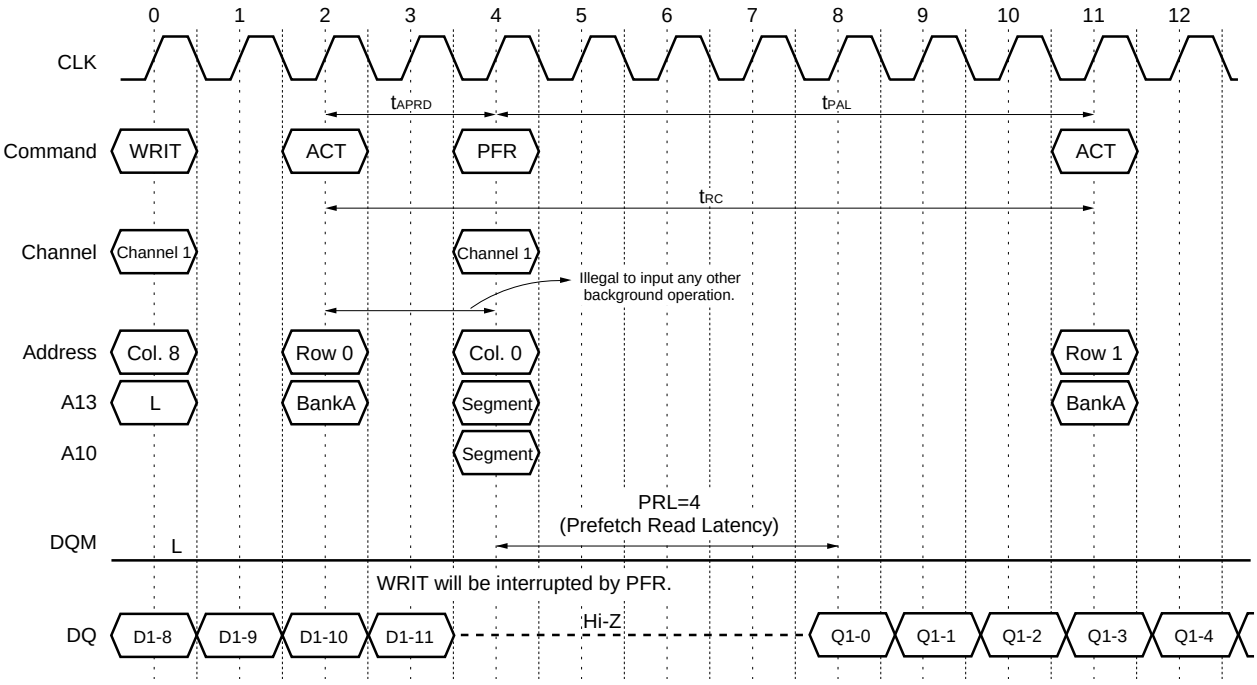
(Read latency = 2, Prefetch Read latency = 4, Burst length = 8)



★

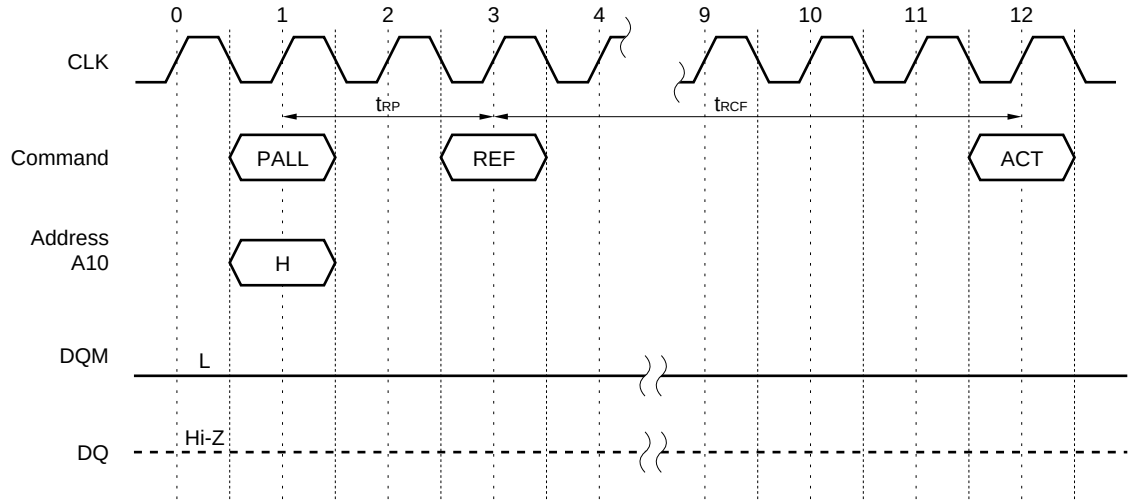
Write to Prefetch Read with Auto Precharge Operation

(Read latency = 2, Prefetch Read latency = 4, Burst length = 8)

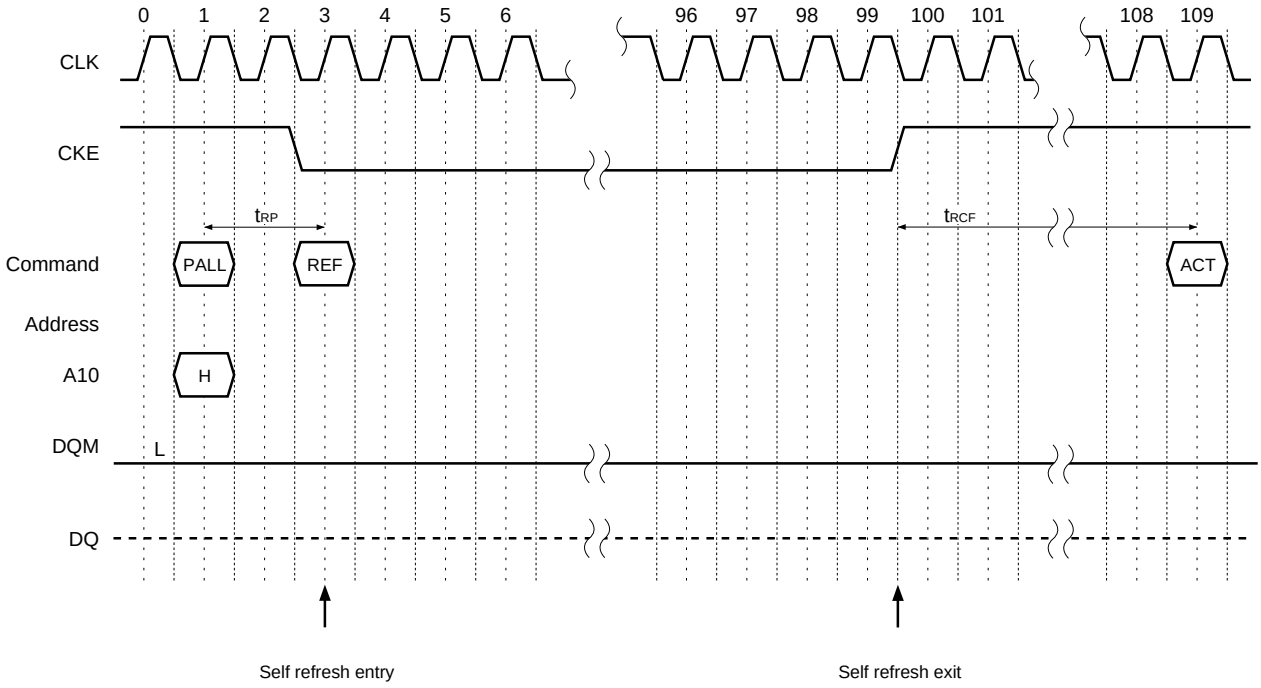


★

Auto Refresh Operation

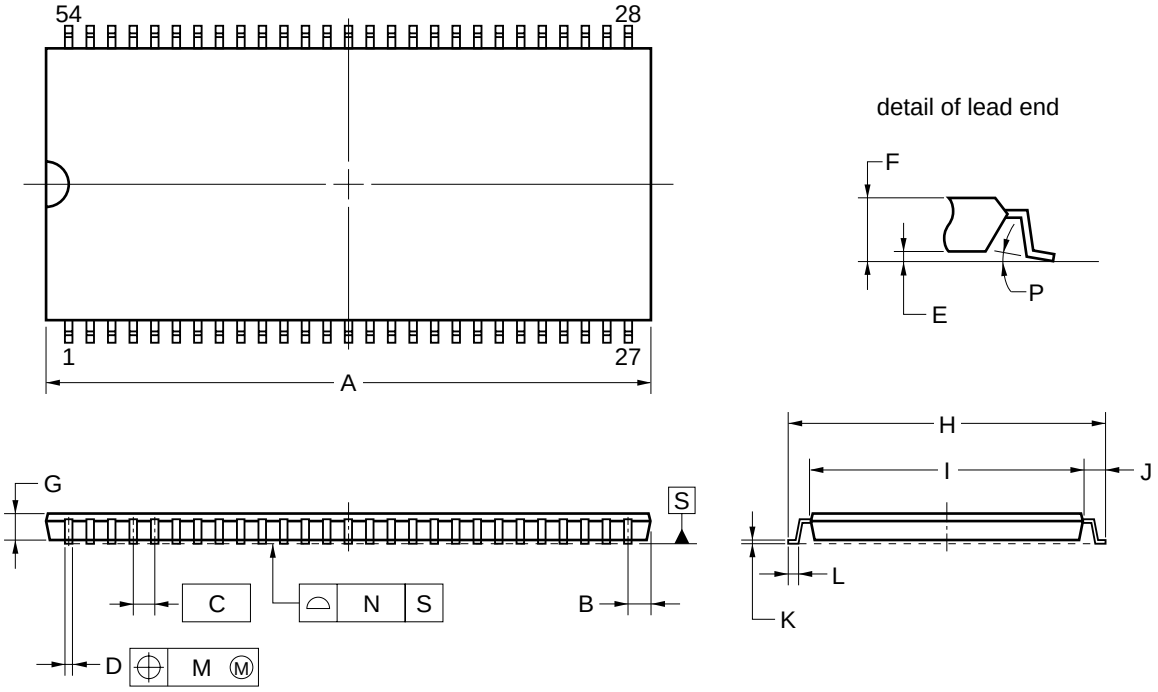


Self Refresh Operation (Entry and Exit)



★ **13. Package Drawing**

54-PIN PLASTIC TSOP (II) (10.16 mm (400))



NOTES

1. Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

2. Dimension "A" does not include mold fiash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

ITEM	MILLIMETERS
A	22.22±0.05
B	0.91 MAX.
C	0.80 (T.P.)
D	$0.32^{+0.08}_{-0.07}$
E	0.10±0.05
F	1.1±0.1
G	1.00
H	11.76±0.20
I	10.16±0.10
J	0.80±0.20
K	$0.145^{+0.025}_{-0.015}$
L	0.50±0.10
M	0.13
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

S54G5-80-9JF-2

14. Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of the μPD45125×××.

Type of Surface Mount Device

μPD45125421G5 : 54-pin Plastic TSOP (II) (10.16mm (400))
μPD45125821G5 : 54-pin Plastic TSOP (II) (10.16mm (400))
μPD45125161G5 : 54-pin Plastic TSOP (II) (10.16mm (400))

15. Revision History

Edition / Date	Page		Description	
	This edition	Previous edition	Type of revision	Location
1st edition / July '99	–	–	–	–
2nd edition / July '99	p.2	p.2	Modification	Organization
	p.2	p.2	Modification	Prefetch read latency for x4 bits organization
	p.5, 6, 7	p.5, 6, 7	Modification	Organization
	p.17	p.17	Addition	Note for Prefetch read with auto precharge
	p.28	p.28	Modification	Text regarding x4 bits organization
	p.36	p.36	Modification	Text regarding x4 bits organization
3rd edition / Nov. '99	p.1	p.1	Addition	Features (Prefetch read latency for x4 bits organization)
	p.2	p.2	Deletion	Low power Operation
	p.3	p.3	Deletion	Low power Operation
	p.4	p.4	Deletion	Low power Operation
	p.44	p.44	Modification	Capacitance
	p.45	p.45	Modification	DC Characteristics 1
	p.47	p.47	Modification	t_{CK1}, t_{CK2}, t_{AC1}, t_{AC2}, t_{HZ1}, t_{HZ2}
	p.58	p.58	Modification	D3-3
	p.71	p.71	Addition	D1-10
	p.72	p.72	Addition	Q1-11 (Read to Prefetch Read with Auto Precharge Operation)
				D1-11 (Write to Prefetch Read with Auto Precharge Operation)
	p.74	p.74	Modification	Package Drawing

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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- NEC devices are classified into the following three quality grades:
  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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