



Microchip

T-46-13-29

27HC416

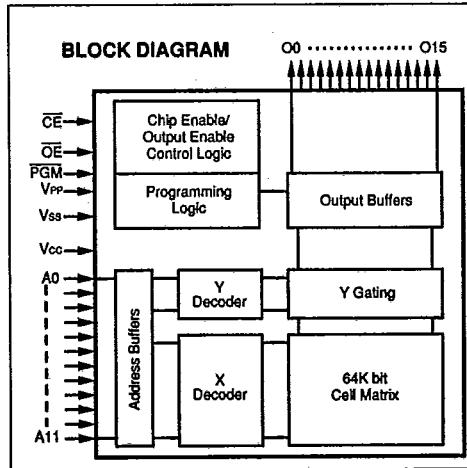
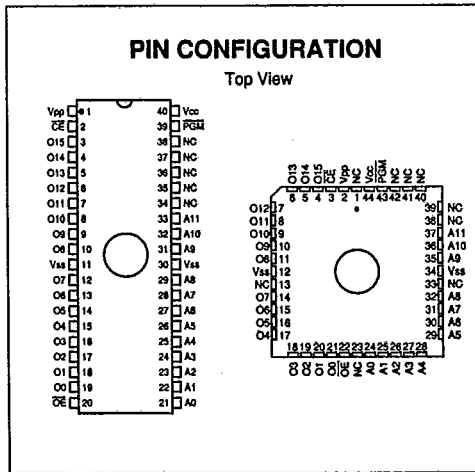
64K (4K x 16) High Speed CMOS UV Erasable PROM

FEATURES

- High speed performance
 - 45ns Maximum access time
- CMOS Technology for low power consumption
 - 90mA Active current
 - 100µA Standby current (low power option)
- OTP (one time programming) available
- WordWide architecture offers a space savings over ByteWide memories
- Two programming algorithms allow improved programming times
 - Fast programming
 - Express
- Organized 4K x 16; JEDEC standard pinouts
 - 40-Pin dual in line package
 - 44-Pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
 - Commercial = 0° C to 70° C
 - Industrial = -40° C to 85° C
 - Military** = -55° C to 125° C

DESCRIPTION

The Microchip Technology Inc. 27HC416 is a CMOS 64K bit (ultraviolet light) Erasable (electrically) Programmable Read Only Memory. The device is organized as 4K words by 16 bits each. Advanced CMOS technology allows bipolar speed with a significant reduction in power. A low power option (L) allows further standby power reduction to 100µA. The 27HC416 is configured in the JEDEC WordWide pinout which allows a two for one package savings over ByteWide memories along with a significant PC board savings. This very high speed single chip solution is ideal for 16/32 bit digital signal processors (DSP) or other sophisticated micro-processors. A complete family of packages is offered to provide the utmost flexibility. One Time Programming (OTP) is available for low cost (plastic) applications.



** See 27HC64 Military Data sheet DS60034

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PIN FUNCTION TABLE	
Name	Function
A0 - A11	Address Inputs
CE	Chip Enable
OE	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O15	Data Output
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc and input voltages w.r.t. Vss-0.6V to +7.0V
 Vpp voltage w.r.t. Vss during programming-0.6V to +14.0V
 Voltage on A9 w.r.t. Vss-0.6V to +13.5V
 Output voltage w.r.t. Vss-0.6V to Vcc +1.0V
 Temperature under bias-65° C to 125° C
 Storage temperature-65° C to 150° C
 ESD protection on all pins2KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION DC Characteristics		VCC = +5V ±10% Commercial: Tamb= 0° C to 70° C Industrial: Tamb= -40° C to 85° C					
Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V _{IH} V _{IL}	2.0 -0.1	V _{CC} +1 0.8	V V	
Input Leakage	all		I _I	-10	10	µA	V _{IN} = -0.1V to V _{CC} + 1.0V
Output Voltages	all	Logic "1" Logic "0"	V _{OH} V _{OL}	2.4	0.45	V V	I _{OH} = -2mA I _{OL} = 8mA
Output Leakage	all		I _O	-10	10	µA	V _{OUT} = -0.1V to V _{CC} + 1.0V
Input Capacitance	all		C _{IN}		6	pF	V _{IN} = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		C _{OUT}		12	pF	V _{OUT} = 0V; Tamb = 25° C; f = 1MHz
Power Supply Current, Active	all	TTL input	I _{CC1}		90	mA	V _{CC} = 5.5V; V _{PP} = V _{CC} f = 2MHz; OE = CE = V _{IL} ; I _{out} = 0mA; V _{IL} = -0.1 to 0.8 V; V _{IH} = 2.0 to V _{CC} ; Note 1
Power Supply Current, Standby	S, SX		I _{CC(S)1}		50	mA	
Power Supply Current, Standby	L, LX L, LX	TTL input CMOS input	I _{CC(S)2}		3 100	mA µA	CE = V _{CC} ±0.2V
I _{PP} Read Current V _{PP} Read Voltage	all all	Read Mode Read Mode	I _{PP} V _{PP}	V _{CC} -0.7	100 V _{CC}	µA V	V _{PP} = 5.5V Note 2

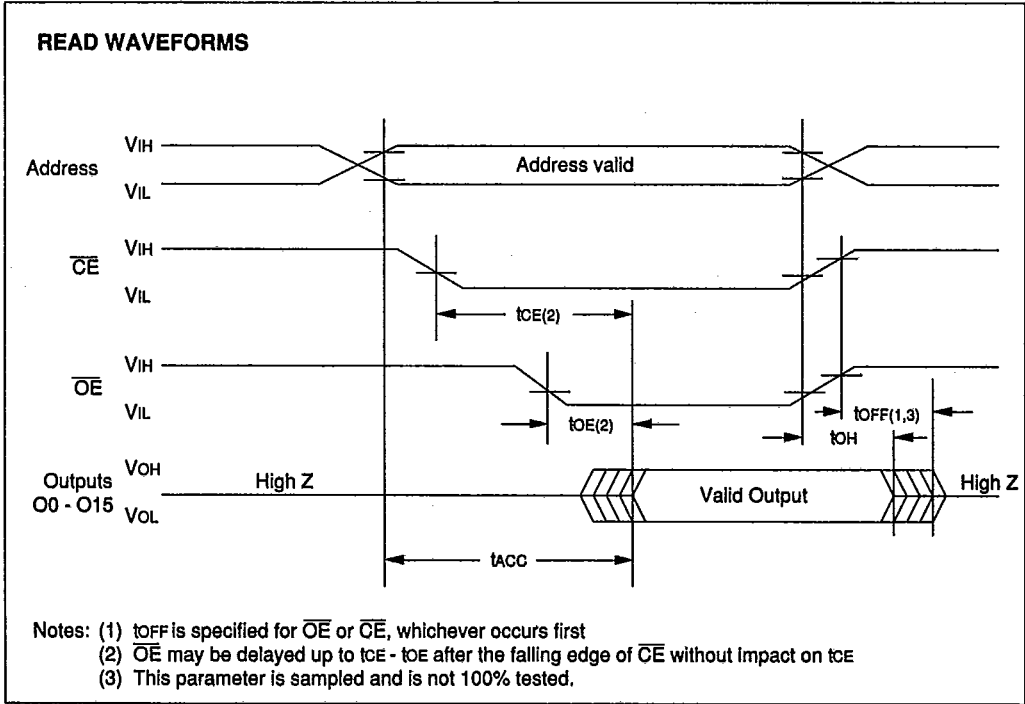
* Parts: S = Standard Power; L = Low Power; X = Industrial Temp Range;
 Notes: (1) AC Power component above 2MHz: 2mA/MHz.
 (2) Vcc must be applied simultaneously or before Vpp and be removed simultaneously or after Vpp.

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READ OPERATION AC Characteristics		AC Testing Waveform: $V_{IH} = 3.0\text{ V}$ and $V_{IL} = 0.0\text{ V}$; $V_{OH} = V_{OL} = 1.5\text{ V}$								
		Output Load: 1 TTL Load + 30 pF								
		Input Rise and Fall Times: 5 nsec								
		Ambient Temperature: Commercial: $T_{amb} = 0^\circ\text{ C}$ to 70° C Industrial: $T_{amb} = -40^\circ\text{ C}$ to 85° C								
Parameter	Part*	Sym	27HC416-45	27HC416-55	27HC416-70	Units	Conditions			
			Min	Max	Min	Max	Min	Max		
Address to Output Delay	all	tACC		45		55		70	ns	$\overline{CE} = \overline{OE} = V_{IL}$
\overline{CE} to Output Delay	L	tCE1		45		55		70	ns	$\overline{OE} = V_{IL}$
	S	tCE2		30		35		45		
\overline{OE} to Output Delay	all	tOE		25		30		35	ns	$\overline{CE} = V_{IL}$
\overline{OE} to O/P High Impedance	all	tOFF	0	20	0	20	0	25	ns	
Output Hold from Address \overline{CE} or \overline{OE} , whichever occurs first	all	tOH	0		0		0		ns	

* Parts: S = Standard Power; L = Low Power



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PROGRAMMING DC Characteristics		Ambient Temperature: 25° C ±5° C For VPP and VCC Voltages refer to Programming Algorithms				
Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V _{IH} V _{IL}	2.0 -0.1	V _{CC} +1 0.8	V V	
Input Leakage		I _{LI}	-10	10	μA	V _{IN} = -.1V to V _{CC} + 1.0V
Output Voltages	Logic "1" Logic "0"	V _{OH} V _{OL}	2.4	0.45	V V	I _{OH} = - 2mA I _{OL} = 8mA
VCC Current, program & verify		I _{CC}		90	mA	
VPP Current,program		I _{PP}		50	mA	Note 1
A9 Product Identification		V _H	11.5	12.5	V	

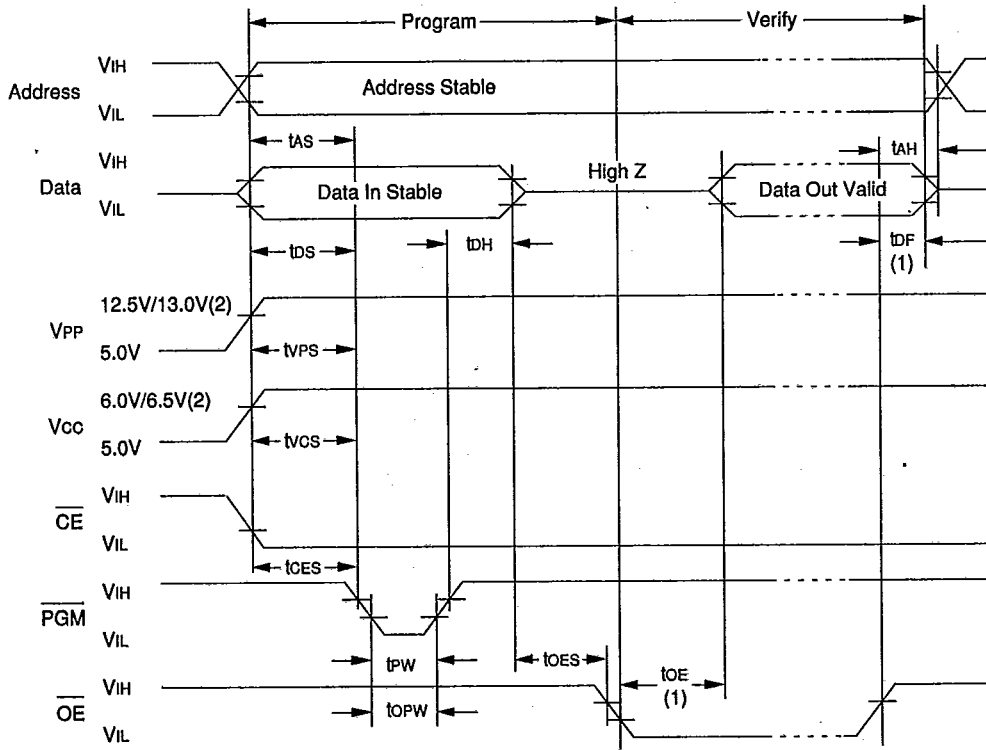
Note: (1) VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP

PROGRAMMING AC Characteristics		AC Testing Waveform: V _{IH} = 2.4 V and V _{IL} = 0.45 V; V _{OH} = 2.0 V; V _{OL} = 0.8 V Output Load: 1 TTL Load + 100 pF Ambient Temperature: 25° C ±5° C For VPP and VCC Voltages, refer to Programming Algorithms				
Parameter	Symbol	Min	Max	Units	Remarks	
Address Set-Up Time	t _{AS}	2		μs		
Data Set-Up Time	t _{DS}	2		μs		
Data Hold Time	t _{DH}	2		μs		
Address Hold Time	t _{AH}	0		μs		
Float Delay (3)	t _{DF}	0	130	ns		
VCC Set-Up Time	t _{VCS}	2		μs		
Program Pulse Width (1)	t _{PW}	0.95	1.05	ms	1 ms typical	
Program Pulse Width (1)	t _{PW}	95	105	μs	100 μs typical	
\overline{CE} Set-Up Time	t _{CES}	2		μs		
\overline{OE} Set-Up Time	t _{OES}	2		μs		
VPP Set-Up Time	t _{VPS}	2		μs		
Overprogram Pulse Width (2)	t _{OPW}	2.85	78.75	ms		
Data Valid from \overline{OE}	t _{OE}		100	ns		

Notes: (1) For express algorithm, initial programming width tolerance is 100 μsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1 msec ± 5%.
 (2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75 msec as a function of the iteration counter value.
 (3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

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PROGRAMMING Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
 (2) VCC = 6.0V ± 0.25V, VPP = VH = 12.5V ± 0.5V for fast programming algorithm
 VCC = 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V for express algorithm



FUNCTIONAL DESCRIPTION

The 27HC416 has the following functional modes:

—Operation: The 27HC416 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.

—Programming: To receive its permanent data, the 27HC416 must be programmed. Both a program and program/verify procedure is available. It can be programmed with Fast or Express algorithm.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

Operation

- Read
- Standby
- Output Disable

For the general characteristics in these operation modes, refer to the table below.

Operation Mode	CE	OE	PGM	VPP	A9	O0 - O15
Read	VIL	VIL	VH	VCC	X	Dout
Program	VIL	VH	VIL	VH	X	Din
Program Verify	VIL	VIL	VH	VH	X	Dout
Program Inhibit	VH	X	X	VH	X	High Z
Standby	VH	X	X	VCC	X	High Z
Output Disable	X	VH	VH	VCC	X	High Z
Identity	VIL	VIL	VH	VCC	VH	Identity Code

X = Don't Care
 VH = 12.0 ± 0.5V

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Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC416's memory data is accessed when

- the chip is enabled by setting the \overline{CE} pin low.
- the data is gated to the output pins by setting the \overline{OE} pin low.

For Read operations on the Low Power version, once the addresses are stable, the address access time (tACC) is equal to the delay from \overline{CE} to output (tCE). A faster \overline{CE} access time (tCE) is available on the standard part to provide the additional time for decoding the \overline{CE} signal. Data is transferred to the output after a delay (tOE) from the falling edge of \overline{OE} .

Standby Mode

The standby mode is entered when the \overline{CE} pin is high, and the program mode is not defined. When these conditions are met, the supply current will drop from 90mA to 100 μ A on the low power part, and to 50mA on the standard part.

Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the \overline{OE} pin is high, and the program mode is not defined.

Programming/Verification

The 27HC416 has to be programmed, and afterward the programmed information verified. Before these operations, the Identity Code can be read to properly set up automated equipment. Multiple devices in parallel can be programmed using the programming and inhibit modes.

Programming Algorithms

Two programming algorithms are available: fast programming and express.

The fast programming algorithm is the industry standard programming mode that requires both initial programming pulses and overprogramming pulses. A flowchart of the algorithm is shown in Figure 1.

Express algorithm has been developed to improve programming through-put times in a production environment. Up to 10 pulses of 100 μ sec each are applied until the byte is verified. No overprogramming is required. A flowchart of this algorithm is shown in Figure 2.

The programming mode is entered when:

- a) VCC is brought to the proper level
- b) VPP is brought to the proper VH level
- c) the \overline{OE} pin is high
- d) the \overline{CE} pin is low, and
- e) the PGM pin is pulsed low.

Since the erase state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A11, and the data is presented to pins O0 - O15. When data and address are stable, a low going pulse on the PGM line programs that memory location.

Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

- a) VCC is at the proper level
- b) VPP is at the proper VH level
- c) the \overline{OE} line is low
- d) the \overline{CE} pin is low, and
- e) the PGM line is high.

Inhibit Mode

When Programming multiple devices in parallel with different data only PGM needs to be under separate control to each device. By pulsing the PGM line low on a particular device, that device will be programmed, and all other devices with corresponding PGM or \overline{CE} held high will not be programmed with the data although address and data are available on their input pins.

Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to VH (11.5V to 12.5V). The \overline{CE} and \overline{OE} pins must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

Pin \rightarrow	Input	Output*								
Identity \downarrow	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
	Manufacturer Device Type*	VIL	0	0	1	0	1	0	0	1
	VIH	0	0	0	1	0	1	1	0	16

*Code subject to change.

Note: O15 - O8 are 00 for the manufacturer and device type code.

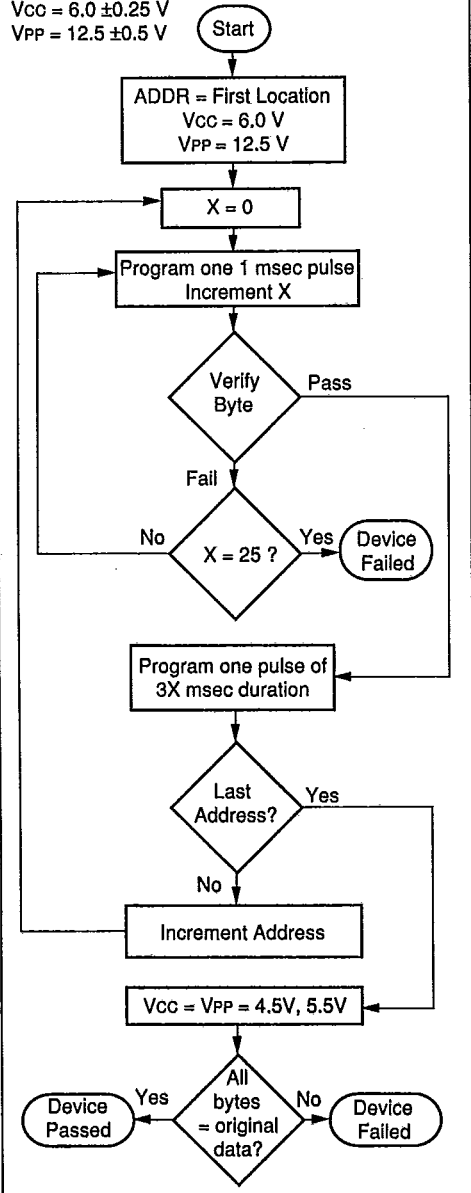
Erase

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultra-violet light at wavelengths ≤ 4000 Angstroms (\AA). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537 \AA with an intensity of 12,000 μ W/cm² at 1". The erasure time at that distance is about 15 to 20 min.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

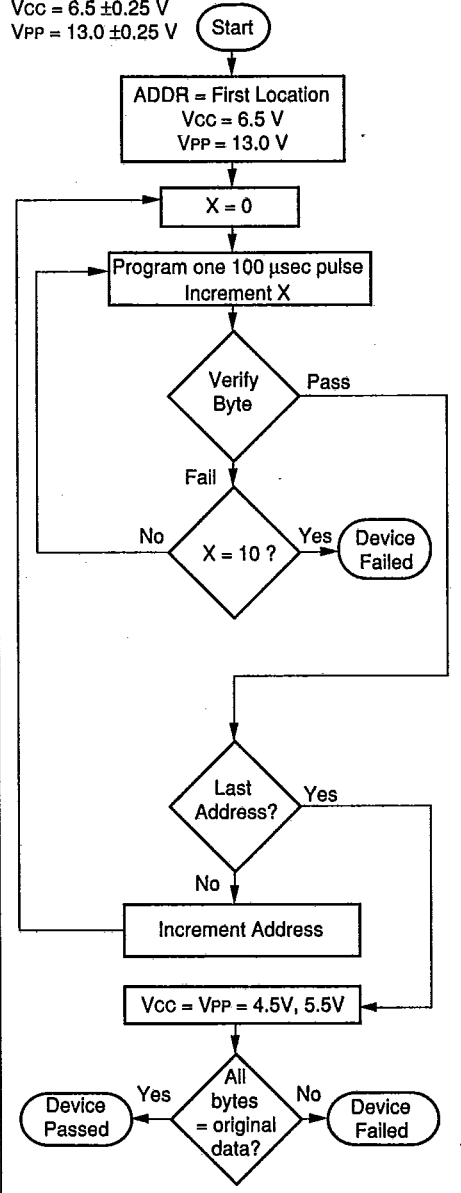
PROGRAMMING - Figure 1
Fast Algorithm

Conditions:
Tamb = 25°C ±5°C
Vcc = 6.0 ±0.25 V
Vpp = 12.5 ±0.5 V



PROGRAMMING - Figure 2
Express Algorithm

Conditions:
Tamb = 25°C ±5°C
Vcc = 6.5 ±0.25 V
Vpp = 13.0 ±0.25 V



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27HC416 - 45 I / J

Package:	J	Cerdip DIP
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
Temperature Range:	Blank	0° C to 70° C
	I	-40° C to 85° C
Access Time:	45	45 nsec
	55	55 nsec
	70	70 nsec
Device	27HC416	64K (4K x 16) High Speed CMOS EPROM
	27HC416L	64K (4K x 16) High Speed Low Power CMOS EPROM