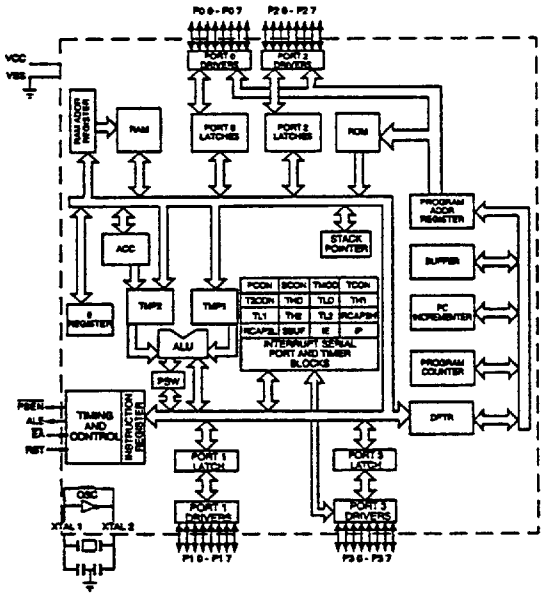
# Radiation Hardened 80C32ERP

High Speed CMOS-epi
8-Bit Microcontroller

*For Space Applications*



SEI's 80C32ERP (RP for RAD-PAK®) high speed CMOS microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 80C32ERP is fully equivalent to Intel's 80C32 8-bit CMOS microcontroller. The 80C32ERP product is manufactured as a CMOS-epi process for improved single event latchup performance. The fully static design of the 80C32ERP allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data. The 80C32ERP features 256 bytes of RAM; 32 I/O lines; three 16 bit timers; a 6-source, 2 level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuits. In addition, the 80C32ERP has two software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the RAM, the timers, the serial port, and the interrupt system continue to function. In the Power Down Mode the RAM is saved and all other functions are inoperative.

SPACE ELECTRONICS INCORPORATED

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9011241 0000275 196

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# 80C32ERP

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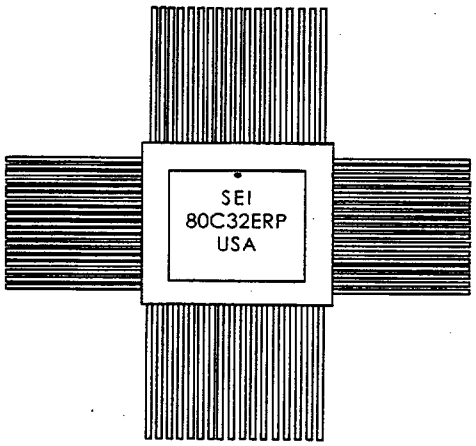


PIN CONFIGURATION
TOP VIEW

## Features

- 8-bit CMOS Microcontroller
- Compatible with Intel 80C32
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
  - Total Dose Hardness >100 krad (Si)
  - Single Event Latchup >100 MeV/mg/cm²
- Package:
  - 44 Pin RAD-PAK® quad flat pack (650 mils x 650 mils)
  - Weight: 12 grams
- Frequency Range:
  - D.C. to 30 MHz
- 80C32ERP: ROMless version of the 80C52
- High Performance CMOS-epi Technology
  - Single 5 Volt Power Supply
  - Low Power Supply Current:
  - Idle: 10 mA
  - Active: 25 mA
- 256 x 8 Bit RAM
- 32 Programmable I/O Lines
- Three 16 Bit Timer/ Controller
- 64K Program/ Data Memory Space
- Boolean Processor
- 6 Interrupt Sources
- Programmable serial port
- Screening per TM 5004
- QCI per TM5005

TQM
Total Quality Management

May 1996

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**80C32ERP EXTERNAL DATA MEMORY CHARACTERISTICS**

| SYMBOL | PARAMETER | 30 MHz MIN | MAX |
|---|---|---|---|
| TRLRH | RD Pulse Width | 180 | |
| TWLWH | WR Pulse Width | 180 | |
| TLLAX | Address Hold After ALE | 55 | |
| TRLDV | RD to Valid Data In | | 135 |
| TRHDX | Data Hold After RD | 0 | |
| TRHDZ | Data Float After RD | | 70 |
| TLLDV | ALE to Valid Data In | | 235 |
| TAVDV | Address to Valid Data In | | 260 |
| TLLWL | ALE to WR or RD | 90 | 115 |
| TAVWL | Address to WR or RD | 115 | |
| TQVWX | Data Valid to WR Transition | 20 | |
| TQVWH | Data Set-Up to WR High | 215 | |
| YWHQX | Data Hold After WR | 20 | |
| TRLAZ | RD Low to Address Float | | 0 |
| TWHLH | RD or WR High to ALE High | 20 | 40 |

80C32ERP AC PARAMETERS:
TA = -55 to + 125°C; Vss = 0 V; VCC = 5 V ± 10%; F = 0 to 30 MHz
( Load Capacitance for PORT0, ALE and PSEN = 100 pf; Load Capacitance for all other outputs = 80 pf.

**EXTERNAL PROGRAM MEMORY CHARACTERISTICS**

| SYMBOL | PARAMETER | 30 MHz MIN | MAX |
|---|---|---|---|
| TLHLL | ALE pulse width | 60 | |
| TAVLL | Address Valid to ALE | 15 | |
| TLLAX | Address Hold after ALE | 35 | |
| TLLIV | ALE to Valid Instr In | | 100 |
| TLLPL | ALE to PSEN | 25 | |
| TPLPH | PSEN Pulse Width | 80 | |
| TPLIV | PSEN to Valid Instr IN | | 65 |
| TPXIX | Input Instr Hold After PSEN | 0 | |
| TPXIZ | Input Instr Float After PSEN | | 30 |
| TPXAV | PSEN to Address Valid | 25 | |
| TAVIV | Address to Valid Instr In | | 130 |
| TPLAZ | PSEN Low to Address Float | | 6 |

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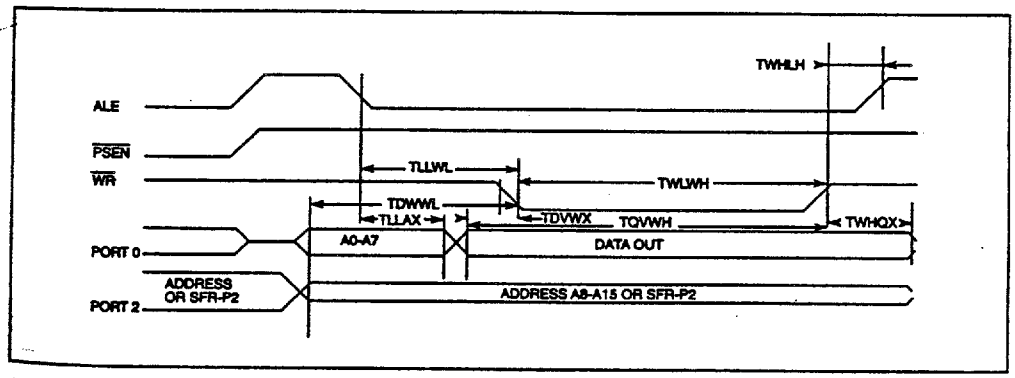
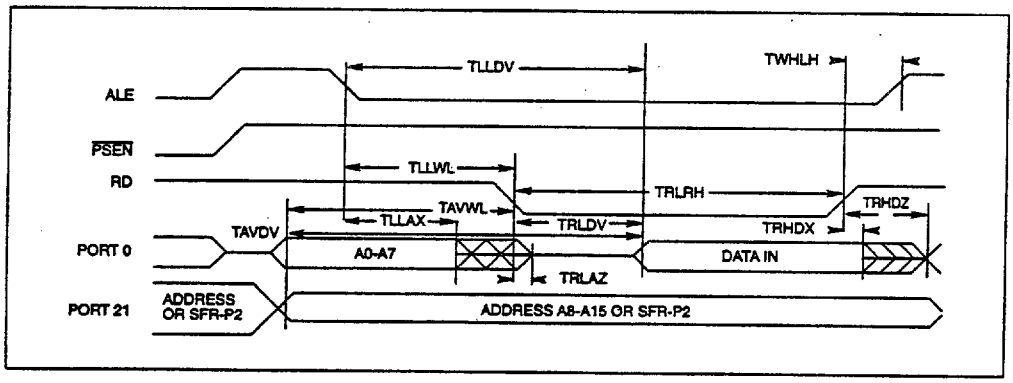
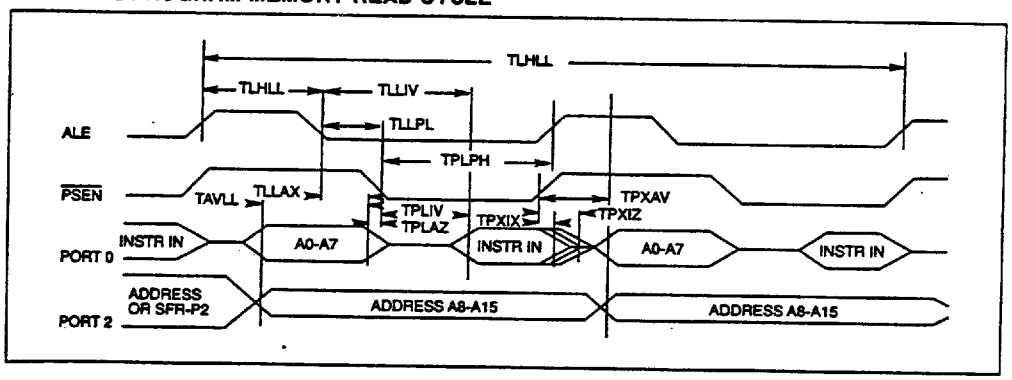
**EXTERNAL DATA MEMORY WRITE CYCLE**




**EXTERNAL DATA MEMORY READ CYCLE**




**EXTERNAL PROGRAM MEMORY READ CYCLE**

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# INSTRUCTION OPCODES

**INSTRUCTION SET DESCRIPTION**

| ARITHMETIC OPERATIONS MNEMONIC | | DESCRIPTION | BYTE | CYC |
|---|---|---|---|---|
| ADD | A, Rn | Add registrer to Accumulator | 1 | 1 |
| ADD | A, direct | Add direct bytes to Accumulator | 2 | 1 |
| ADD | A, @Ri | Add indirect RAM to Accumulator | 1 | 1 |
| ADD | A, #data | Add immediate data ot Accumulator | 2 | 1 |
| ADDC | A, Rn | Add register to Accumulator with Carry | 1 | 1 |
| ADDC | A, direct | Add direct byte to A with Carry flag | 2 | 1 |
| ADDC | A, @Ri | Add indirect RAM to A with Carry flag | 1 | 1 |
| ADDC | A, #data | Add immediate data to A with Carry flag | 2 | 1 |
| SUBB | A, Rn | Subtract register from A with borrow | 1 | 1 |
| SUBB | A, direct | Subtract direct byte from A with Borrow | 2 | 1 |
| SUBB | A, @Ri | Subtract indirect RAM from A with Borrow | 1 | 1 |
| SUBB | A, data | Subtract immed. data from A with Borrow | 2 | 1 |
| INC | A | Increment Accumulator | 1 | 1 |
| INC | Rn | Increment register | 1 | 1 |
| INC | direct | Increment direct byte | 2 | 1 |
| INC | @Ri | Increment indirect RAM | 1 | 1 |
| INC | DPTR | Increment Data Pointer | 1 | 2 |
| DEC | A | Decrement Accumulator | 1 | 1 |
| DEC | Rn | Decrement register | 1 | 1 |
| DEC | direct | Decrement direct byte | 2 | 1 |
| DEC | @Ri | Decrement indirect RAM | 1 | 1 |
| MUL | AR | Multiply A & B | 1 | 4 |
| DIV | AB | Divide A by B | 1 | 4 |
| DA | A | Decimal Adjust Accumulator | 1 | 1 |
| **LOGICAL OPERATIONS MNEMONIC** | | **DESTINATION** | **BYTE** | **CYC** |
| ANL | A, Rn | AND register to Accumulator | 1 | 1 |
| ANL | A, direct | AND direct byte to Accumulator | 2 | 1 |
| ANL | A, @Ri | AND indirect RAM to Accumulator | 1 | 1 |
| ANL | A, #data | AND immediate data to Accumulator | 2 | 1 |
| ANL | direct, A | AND Accumultaor to direct byte | 2 | 1 |
| ANL | direct, #data | AND immediate data to direct byte | 3 | 2 |
| ORL | A, Rn | OR register to Accumulator | 1 | 1 |
| ORL | A, direct | OR direct byte to Accumulator | 2 | 1 |
| ORL | A, @Ri | OR indirect RAM to Accumulator | 1 | 1 |
| ORL | A, #data | OR immediate data to Accumulator | 2 | 1 |
| ORL | direct A | OR Accumulator to direct byte | 2 | 1 |
| ORL | direct, #data | OR immediate data to direct byte | 3 | 2 |
| XRL | A, Rn | Exclusive-OR register to Accumulator | 1 | 1 |
| XRL | A, direct | Exclusive-OR direct byte to Accumulator | 2 | 1 |
| XRL | A, @Ri | Exclusive-OR indirect RAM to A | 1 | 1 |
| XRL | A, #data | Exclusive-OR immediate data to A | 2 | 1 |
| XRL | direct, A | Exclusive-OR Accumulator to direct byte | 2 | 1 |
| XRL | direct, #data | Exclusive-OR immediate data to direct | 3 | 2 |
| CLR | A | Clear Accumulator | 1 | 1 |
| CPL | A | Complement Accumulator | 1 | 1 |
| RL | A | Rotate Accumulator Left | 1 | 1 |
| RLC | A | Rotate A Left through the Carry flag | 1 | 1 |
| RR | A | Rotate Accumulator Right | 1 | 1 |
| RRC | A | Rotate A Flight through Carry flag | 1 | 1 |
| SWAP | A | Swap nibbles within the Accumulator | 1 | 1 |

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**PIN DESCRIPTION**

**$V_{ss}$**
Circuit Ground Potential

**Vcc**
Supply voltage during normal, idle, and Power Down operation.

**PORT 0**
Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.
Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. External pullups are required during program verification. Port 0 can sink 8 LS TTL inputs.

**PORT 1**
Port 1 is an 8 bit bi-directional with internal pullups. Port 1 pins that have 1's written to them are pulled by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.
Port 1 also receives the low-order address byte during program verification. It can drive CMOS inputs without external pullups.
2 inputs of Port 1 are also used for timer/counter 2:
P1.0 [T2]: External clock input for timer/counter 2.
P1.1 [T2EX]: A trigger input for timer/counter 2, to be reloaded or captured causing the timer/counter 2 interrupt.

**PORT 2**
Port 2 is an 8 bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (ILL, on data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16 bit address (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit address (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.

**PORT 3**
Port 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (ILL,on the data sheet) because of the pullups. It also serves the
function of various special features as listed below.

| PORT PIN | Alternate Function |
|---|---|
| P3.0 | RXT (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | INT0 (external interrupt 0) |
| P3.3 | INT1 (external interrupt 1) |
| P3.4 | T0 (Timer 0 external input) |
| P3.5 | T1 (Timer 1 external input) |
| P3.6 | WR\ (external Data Memory write strobe) |
| P3.7 | RD\ (external Data Memory read strobe) |

Port 3 can sink/source three LS TTL inputs. IT can drive CMOS inputs without external pullups.

**RST**
A high level on this for two machines cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to Vcc.

**ALE**
Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 of the oscillator frequency except during an external data memory access at which time on ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

**PSEN**
Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetched from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

**EA**
When EA is held high, the CPU executed out of internal Program Memory (unless the Program Counter exceeds 1FFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

**XTAL 1**
Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

**XTAL 2**
Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. This pin should be floated when an external oscillator is used.

**80C32ERP PINOUT**

| PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|
| 1 | P15 | 23 | P25 |
| 2 | P16 | 24 | P26 |
| 3 | P17 | 25 | P27 |
| 4 | RST | 26 | PSEN\ |
| 5 | P30 | 27 | ALE |
| 6 | NC | 28 | NC |
| 7 | P31 | 29 | EA\ |
| 8 | P32 | 30 | P07 |
| 9 | P33 | 31 | P06 |
| 10 | P34 | 32 | P05 |
| 11 | P35 | 33 | P04 |
| 12 | P36 | 34 | P03 |
| 13 | P37 | 35 | P02 |
| 14 | XTAL2 | 36 | P01 |
| 15 | XTAL1 | 37 | P00 |
| 16 | VSS | 38 | VCC |
| 17 | NC | 39 | NC |
| 18 | P20 | 40 | P10 |
| 19 | P21 | 41 | P11 |
| 20 | P22 | 42 | P12 |
| 21 | P23 | 43 | P13 |
| 22 | P24 | 44 | P14 |

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INSTRUCTION OPCODES IN HEXADECIMAL ORDER

| HEX CODE | NUMB. OF BYTES | MNEM. | OPERANDS |
|---|---|---|---|
| 00 | 1 | NOP | |
| 01 | 2 | AJMP | code addr |
| 02 | 3 | LJMP | code addr |
| 03 | 1 | RR | A |
| 04 | 1 | INC | A |
| 05 | 2 | INC | data addr |
| 06 | 1 | INC | @R0 |
| 07 | 1 | INC | @R1 |
| 08 | 1 | INC | R0 |
| 09 | 1 | INC | R1 |
| 0A | 1 | INC | R2 |
| 0B | 1 | INC | R3 |
| 0C | 1 | INC | R4 |
| 0D | 1 | INC | R5 |
| 0E | 1 | INC | R6 |
| 0F | 1 | INC | R7 |
| 10 | 3 | JBC | bit addr, code addr |
| 11 | 2 | ACALL | code addr |
| 12 | 3 | LCALLRR | code addr |
| 13 | 1 | C | A |
| 14 | 1 | DEC | A |
| 15 | 2 | DEC | data addr |
| 16 | 1 | DEC | @R0 |
| 17 | 1 | DEC | @R1 |
| 18 | 1 | DEC | R0 |
| 19 | 1 | DEC | R1 |
| 1A | 1 | DEC | R2 |
| 1B | 1 | DEC | R3 |
| 1C | 1 | DEC | R4 |
| 1D | 1 | DEC | R5 |
| 1E | 1 | DEC | R6 |
| 1F | 1 | DEC | R7 |
| 20 | 3 | JB | bit addr, code addr |
| 21 | 2 | AJMP | code addr |
| 22 | 1 | RET | |
| 23 | 1 | RL | A |
| 24 | 2 | ADD | A, data |
| 25 | 2 | ADD | A, data addr |
| 26 | 1 | ADD | A, @R0 |
| 27 | 1 | ADD | A, @R1 |
| 28 | 1 | ADD | A, R0 |
| 29 | 1 | ADD | A, R1 |
| 2A | 1 | ADD | A, R2 |
| 2B | 1 | ADD | A, R3 |
| 2C | 1 | ADD | A, R4 |
| 2D | 1 | ADD | A, R5 |
| 2E | 1 | ADD | A, R6 |
| 2F | 1 | ADD | A, R7 |
| 30 | 3 | JNB | bit, addr, code addr |
| 31 | 2 | ACALL | code addr |
| 32 | 1 | RETI | |

| HEX CODE | NUMB. OF BYTES | MNEM. | OPERANDS |
|---|---|---|---|
| 33 | 1 | RLC | A |
| 34 | 2 | ADDC | A, #data |
| 35 | 2 | ADDC | A, data addr |
| 36 | 1 | ADDC | A, @RD |
| 37 | 1 | ADDC | A, @R1 |
| 38 | 1 | ADDC | A, R0 |
| 39 | 1 | ADDC | A, R1 |
| 3A | 1 | ADDC | A, R2 |
| 3B | 1 | ADDC | A, R3 |
| 3C | 1 | ADDC | A, R4 |
| 3D | 1 | ADDC | A, R5 |
| 3E | 1 | ADDC | A, R6 |
| 3F | 1 | ADDC | A, R7 |
| 40 | 2 | JC | code addr |
| 41 | 2 | AJMP | code addr |
| 42 | 2 | ORL | data addr A |
| 43 | 3 | ORL | data addr, #data |
| 44 | 2 | ORL | A, #data |
| 45 | 2 | ORL | A, data addr |
| 46 | 1 | ORL | A, @R0 |
| 47 | 1 | ORL | A, @R1 |
| 48 | 1 | ORL | A, R0 |
| 49 | 1 | ORL | A, R1 |
| 4A | 1 | ORL | A, R2 |
| 4B | 1 | ORL | A, R3 |
| 4C | 1 | ORL | A, R4 |
| 4D | 1 | ORL | A, R5 |
| 4E | 1 | ORL | A, R6 |
| 4F | 1 | ORL | A, R7 |
| 50 | 2 | JNC | code addr |
| 51 | 2 | ACALL | code addr |
| 52 | 2 | ANL | data addr, A |
| 53 | 3 | ANL | data addr, #data |
| 54 | 2 | ANL | A, #data |
| 55 | 2 | ANL | A, data addr |
| 56 | 1 | ANL | A, @R0 |
| 57 | 1 | ANL | A, @R1 |
| 58 | 1 | ANL | A, R0 |
| 59 | 1 | ANL | A, R1 |
| 5A | 1 | ANL | A, R2 |
| 5B | 1 | ANL | A, R3 |
| 5C | 1 | ANL | A, R4 |
| 5D | 1 | ANL | A, R5 |
| 5E | 1 | ANL | A, R6 |
| 5F | 1 | ANL | A, R7 |
| 60 | 2 | JZ | code addr |
| 61 | 2 | AJMP | code addr |
| 62 | 2 | XRL | data addr A |
| 63 | 3 | XRL | data addr, #data |
| 64 | 2 | XRL | A, #data |
| 65 | 2 | XRL | A, data addr |

| HEX CODE | NUMB. OF BYTES | MNEM. | OPERANDS |
|---|---|---|---|
| 66 | 1 | XRL | A, @R0 |
| 67 | 1 | XRL | A, @R1 |
| 68 | 1 | XRL | A, R0 |
| 69 | 1 | XRL | A, R1 |
| 6A | 1 | XRL | A, R2 |
| 6B | 1 | XRL | A, R3 |
| 6C | 1 | XRL | A, R4 |
| 6D | 1 | XRL | A, R5 |
| 6E | 1 | XRL | A, R6 |
| 6F | 1 | XRL | A, R7 |
| 70 | 2 | JNZ | code addr |
| 71 | 2 | ACALL | code addr |
| 72 | 2 | ORL | C, bit addr |
| 73 | 1 | JMP | @A + DPTR |
| 74 | 2 | MOV | A, #data |
| 75 | 3 | MOV | data addr, #data |
| 76 | 2 | MOV | @R0, #data |
| 77 | 2 | MOV | @R1, #data |
| 78 | 2 | MOV | R0, #data |
| 79 | 2 | MOV | R1, #data |
| 7A | 2 | MOV | R2, #data |
| 7B | 2 | MOV | R3, #data |
| 7C | 2 | MOV | R4, #data |
| 7D | 2 | MOV | R5, #data |
| 7E | 2 | MOV | R6, #data |
| 7F | 2 | MOV | R7, #data |
| 80 | 2 | SJMP | code addr |
| 81 | 2 | AJMP | code addr |
| 82 | 2 | ANL | C, bit addr |
| 83 | 1 | MOVC | A, @A + PC |
| 84 | 1 | DIV | AB |
| 85 | 3 | MOV | data addr, data addr |
| 86 | 2 | MOV | data addr, @R0 |
| 87 | 2 | MOV | data addr, @R1 |
| 88 | 2 | MOV | data addr, R0 |
| 89 | 2 | MOV | data addr, R1 |
| 8A | 2 | MOV | data addr, R2 |
| 8B | 2 | MOV | data addr, R3 |
| 8C | 2 | MOV | data addr, R4 |
| 8D | 2 | MOV | data addr, R5 |
| 8E | 2 | MOV | data addr, R6 |
| 8F | 2 | MOV | data addr, R7 |
| 90 | 3 | MOV | DPTR, #data |
| 91 | 2 | ACALL | code adddr |
| 92 | 2 | MOV | bit addr, C |
| 93 | 1 | MOVC | A, @A + DPTR |
| 94 | 2 | SUBB | A, #data |
| 95 | 2 | SUBB | A, data addr |
| 96 | 1 | SUBB | A, @R0 |
| 97 | 1 | SUBB | A, @R1 |
| 98 | 1 | SUBB | A, R0 |

| HEX CODE | NUMB. OF BYTES | MNEM. | OPERANDS |
|---|---|---|---|
| 99 | 1 | SUBB | A, R1 |
| 9A | 1 | SUBB | A, R2 |
| 9B | 1 | SUBB | A, R3 |
| 9C | 1 | SUBB | A, R4 |
| 9D | 1 | SUBB | A, R5 |
| 9E | 1 | SUBB | A, R6 |
| 9F | 1 | SUBB | A, R7 |
| A0 | 2 | ORL | C, bit addr |
| A1 | 2 | AJMP | code addr |
| A2 | 2 | MOV | C, bit addr |
| A3 | 1 | INC | DPTR |
| A4 | 1 | MUL | AB |
| A5 | | reserved | |
| A6 | 2 | MOV | @R0, data addr |
| A7 | 2 | MOV | @R1, data addr |
| A8 | 2 | MOV | R0, data addr |
| A9 | 2 | MOV | R1, data addr |
| AA | 2 | MOV | R2, data addr |
| AB | 2 | MOV | R3, data addr |
| AC | 2 | MOV | R4, data addr |
| AD | 2 | MOV | R5, data addr |
| AE | 2 | MOV | R6, data addr |
| AF | 2 | MOV | R7, data addr |
| B0 | 2 | ANL | C, bit addr |
| B1 | 2 | ACALL | code addr |
| B2 | 2 | CPL | Bit addr |
| B3 | 1 | CPL | C |
| B4 | 3 | CJNE | A, #data, code addr |
| B5 | 3 | CJNE | A, data addr, code addr |
| B6 | 3 | CJNE | @R0, #data, code addr |
| B7 | 3 | CJNE | @R1, #data, code addr |
| B8 | 3 | CJNE | R0, #data, code addr |
| B9 | 3 | CJNE | R1, #data, code addr |
| BA | 3 | CJNE | R2, #data, code addr |
| BB | 3 | CJNE | R3, #data, code addr |
| BC | 3 | CJNE | R5, #data, code addr |
| BD | 3 | CJNE | R4, #data, code addr |
| BE | 3 | CJNE | R6, #data, code addr |
| BF | 3 | CJNE | R7, #data, code addr |
| C0 | 2 | PUSH | data addr |
| C1 | 2 | AJMP | code addr |
| C2 | 2 | CLR | bit addr |
| C3 | 1 | CLR | C |
| C4 | 1 | SWAP | A |
| C5 | 2 | XCH | A, data addr |
| C6 | 1 | XCH | A, @R0 |
| C7 | 1 | XCH | A, @R1 |
| C8 | 1 | XCH | A, R0 |
| C9 | 1 | XCH | A, R1 |
| CA | 1 | XCH | A, R2 |
| CB | 1 | XCH | A, R3 |

| HEX CODE | NUMB. OF BYTES | MNEM. | OPERANDS |
|---|---|---|---|
| CC | 1 | XCH | A, R4 |
| CD | 1 | XCH | A, R5 |
| CE | 1 | XCH | A, R6 |
| CF | 1 | XCH | A, R7 |
| D0 | 2 | POP | data addr |
| D1 | 2 | ACALL | code addr |
| D2 | 2 | SETB | bit addr |
| D3 | 1 | SETB | C |
| D4 | 1 | DA | A |
| D5 | 3 | DJNZ | data addr, code addr |
| D6 | 1 | XCHD | A, @R0 |
| D7 | 1 | XCHD | A, @R1 |
| D8 | 2 | DJNZ | R0, code addr |
| D9 | 2 | DJNZ | R1, code addr |
| DA | 2 | DJNZ | R2, code addr |
| DB | 2 | DJNZ | R3, code addr |
| DC | 2 | DJNZ | R4, code addr |
| DD | 2 | DJNZ | R5, code addr |
| DE | 2 | DJNZ | R6, code addr |
| DF | 2 | DJNZ | R7, code addr |
| E0 | 1 | MOVX | A, @DPTR |
| E1 | 2 | AJMP | code addr |
| E2 | 1 | MOVX | A, @R0 |
| E3 | 1 | MOVX | A, @R1 |
| E4 | 1 | CLR | A |
| E5 | 2 | MOV | A, data addr |

| HEX CODE | NUMB. OF BYTES | MNEM. | OPERANDS |
|---|---|---|---|
| E6 | 1 | MOV | A, @R0 |
| E7 | 1 | MOV | A, @R1 |
| E8 | 1 | MOV | A, R0 |
| E9 | 1 | MOV | A, R1 |
| EA | 1 | MOV | A, R2 |
| EB | 1 | MOV | A, R3 |
| EC | 1 | MOV | A, R4 |
| ED | 1 | MOV | A, R5 |
| EE | 1 | MOV | A, R6 |
| EF | 1 | MOV | A, R7 |
| F0 | 1 | MOVX | @DPTR, A |
| F1 | 2 | ACALL | code addr |
| F2 | 1 | MOVX | @R0, A |
| F3 | 1 | MOVX | @R1, A |
| F4 | 1 | CPL | A |
| F5 | 2 | MOV | data addr, A |
| F6 | 1 | MOV | @R0, A |
| F7 | 1 | MOV | @R1, A |
| F8 | 1 | MOV | R0, A |
| F9 | 1 | MOV | R1, A |
| FA | 1 | MOV | R2, A |
| FB | 1 | MOV | R3, A |
| FC | 1 | MOV | R4, A |
| FD | 1 | MOV | R5, A |
| FE | 1 | MOV | R6, A |
| FF | 1 | MOV | R7, A |

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| ARITHMETIC TRANSFER MNEMONIC | | DESCRIPTION | BYTE | CYC |
|---|---|---|---|---|
| MOV | A, Rn | Move register to Accumulator | 1 | 1 |
| MOV | A, direct | Move direct byte to Accumulator | 2 | 1 |
| MOV | A, @Ri | Move indirect RAM to Accumulator | 1 | 1 |
| MOV | A, #data | Move immediate data to Accumulator | 2 | 1 |
| MOV | Rn, A | Move Accumulator to register | 1 | 1 |
| MOV | Rn, direct | Move direct byte to register | 2 | 2 |
| MOV | Rn, #data | Move immediate data to register | 2 | 1 |
| MOV | direct, A | Move Accumulator to direct byte | 2 | 1 |
| MOV | direct, Rn | Move register to direct byte | 2 | 2 |
| MOV | direct, direct | Move direct byte to direct | 3 | 2 |
| MOV | direct, @Ri | Move indirect RAM to direct byte | 2 | 2 |
| MOV | direct, #data | Move immediate data to direct byte | 3 | 2 |
| MOV | @Ri, A | Move Accumulator to indirect RAM | 1 | 1 |
| MOV | @Ri, direct | Move direct byte to indirect RAM | 2 | 2 |
| MOV | @Ri, #data | Move immediate data to indirect RAM | 2 | 1 |
| MOV | DPTR, #data 16 | Load Data Pointer with a 16-bit constant | 3 | 2 |
| MOVC | A, @A + DPTR | Move Code byte relative to DPTR to A | 1 | 2 |
| MOVC | A, @A + PC | Move Code byte relative to PC to A | 1 | 2 |
| MOVX | A, @Ri | Move External RAM (8-bit addr) to A | 1 | 2 |
| MOVX | A, @DPTR | Move external RAM (16-bit addr) to A | 1 | 2 |
| MOVX | @Ri, A | Move A to External RAM (8-bit addr) | 1 | 2 |
| MOVX | @DPTR, A | Move A to External RAM (16-bit addr) | 1 | 2 |
| PUSH | direct | Push direct byte onto stack | 2 | 2 |
| POP | direct | Pop direct byte from stack | 2 | 2 |
| XCH | A, Rn | Exchange register with Accumulator | 1 | 1 |
| XCH | A, direct | Exchange direct byte with Accumulator | 2 | 1 |
| XCH | A, @Ri | Exchange indirect RAM with A | 1 | 1 |
| XCHD | A, @Ri | Exchange low-order nibble ind RAM with A | 1 | 1 |
| **BOOLEAN VARIABLE MANIPULATION** | | | | |
| **MNEMONIC** | | **DESCRIPTION** | **BYTE** | **CYC** |
| CLR | C | Clear Carry flag | 1 | 1 |
| CLR | bit | Clear direct bit | 2 | 1 |
| SETB | C | Set Carry flag | 1 | 1 |
| SETB | bit | Set direct Bit | 2 | 1 |
| CPL | C | Complement Carry flag | 1 | 1 |
| CPL | bit | Complement direct bit | 2 | 1 |
| ANL | C, bit | AND direct bit to Carry flag | 2 | 2 |
| ANL | C,/bit | AND complement of direct bit to Carry | 2 | 2 |
| ORL | C,bit | OR direct bit to Carry flag | 2 | 2 |
| ORL | C,/bit | OR complement of direct bit to Carry | 2 | 2 |
| MOV | C,bit | Move direct bit to Carry flag | 2 | 1 |
| MOV | bit, C | Move Carry flag to direct bit | 2 | 2 |
| **PROGRAM AND MACHINE CONTROL** | | | | |
| **MNEMONIC** | | **DESCRIPTION** | **BYTE** | **CYC** |
| ACALL | addr 11 | Absolute subroutine Call | 2 | 2 |
| LCALL | addr 16 | Long Subroutine Call | 3 | 2 |
| RET | | Return from subroutine | 1 | 2 |
| RETI | | Return from interrupt | 1 | 2 |
| AJMP | addr 11 | Absolute Jump | 2 | 2 |
| LJMP | addr 16 | Long Jump | 3 | 2 |
| SJMP | rel | Short Jump (relative addr) | 2 | 2 |
| JMP | @A + DPTR | Jump indirect relative to the DPTR | 1 | 2 |
| JZ | rel | Jump if Accumulator is Zero | 2 | 2 |
| JNZ | rel | Jump if Accumulator is Not Zero | 2 | 2 |
| JC | rel | Jump if Carry flag is set | 2 | 2 |
| JNC | rel | Jump if No Carry flag | 2 | 2 |

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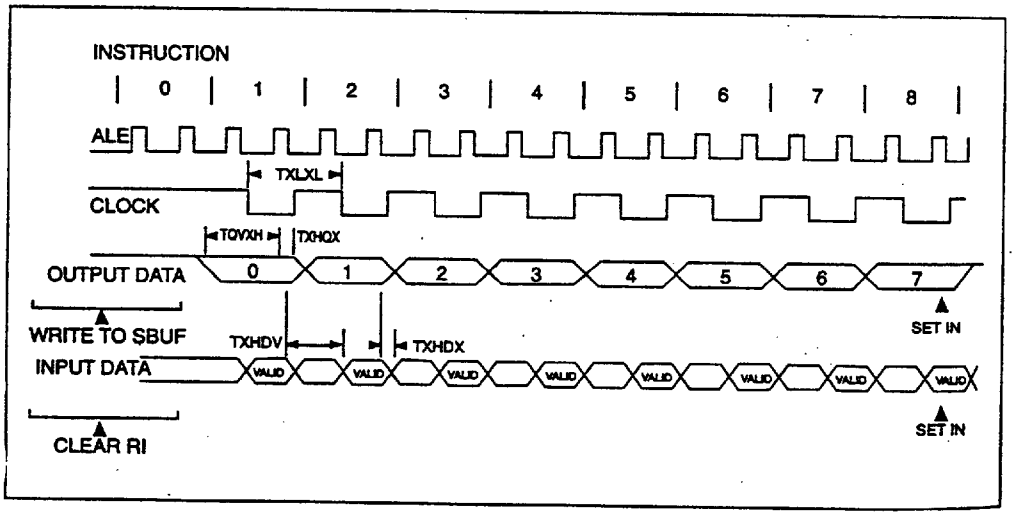
| PROGRAM AND MACHINE CONTROL (cont.) MNEMONIC | | DESCRIPTION | BYTE | CYC |
|---|---|---|---|---|
| JB | bit, rel | Jump if direct Bit set | 3 | 2 |
| JNB | bit, rel | Jump if direct Bit Not sef | 3 | 2 |
| JBC | bit, rel | Jump if direct Bit is set & Clear bit | 3 | 2 |
| CJNE | A, direct, rel | Compare direct to A & Jump if Not Equal | 3 | 2 |
| CJNE | A, #data, ref | Comp. immed. to A & Jump if Not Equal | 3 | 2 |
| CJNE | Rn, #data, rel | Comp. immed. to reg & Jump if Not Equal | 3 | 2 |
| CJNE | @Ri, #data, rel | Comp. immed. to ind. & jump if Not Equal | 3 | 2 |
| DJNZ | Rn, rel | Decrement register & Jump if Not Zero | 2 | 2 |
| DJNZ | direct, rel | Decrement direct & Jump if Not Zero | 3 | 2 |
| NOP | | No operation | 1 | 1 |

**80C32ERP SERIAL PORT TIMING - SHIFT REGISTER MODE**
$T_A$ = -55 TO 125°C; Vss = 0 V; VCC = 5 V ± 10%; F = 0 TO 30 MHz

| SYMBOL | PARAMETER | 30 MHz MIN | MAX |
|---|---|---|---|
| TXLXL | Serial port clock cycle time | 400 | |
| TQVHX | Output data setup to clock rising edge | 300 | |
| TXHQX | Output data hold after clock rising edge | 50 | |
| TXHDX | Input data hold after clock rising edge | 0 | |
| TXHDV | Clock rising edge to input data valid | | 300 |

**SHIFT REGISTER TIMING WAVEFORMS**

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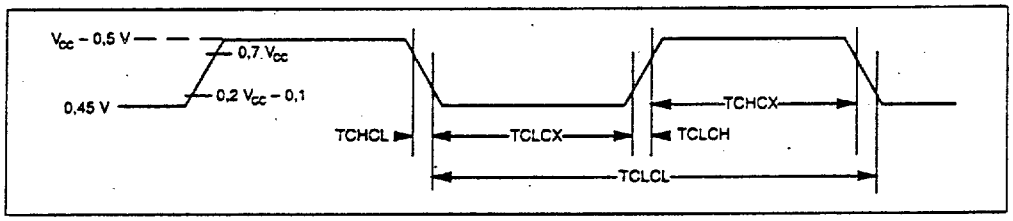
**80C32ERP EXTERNAL CLOCK DRIVE CHARACTERISTICS (XTAL1)**

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| FCLCL | Oscillator Frequency | | 42 | MHz |
| TCLCL | Oscillator Period | 23.8 | | ns |
| TCHCX | High Time | 5 | | ns |
| TCLCX | Low Time | 5 | | ns |
| TCLCH | Rise Time | | 5 | ns |
| TCHCL | Fall Time | | 5 | ns |

**EXTERNAL CLOCK DRIVE WAVEFORMS**







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