■ General Description

The AME9001 controller provides a cost efficient means to drive single or multiple cold cathode fluorescent lamps (CCFL). Specifically the AME9001 drives 3 external MOSFETs that, in turn, drive a wirewound transformer that is coupled to the CCFL.

The AME9001 includes features such as soft start, duty cycle dimming control, and fault detection. It is designed to work with input voltages from 7V up to 24V. When disabled the circuit goes into a zero current mode.

For applications that use a piezoelectric transformer please look at the AME9000.

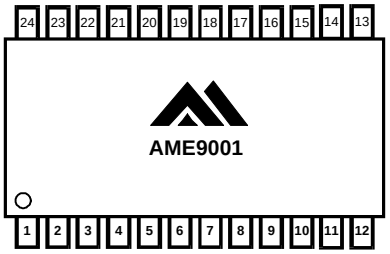
■ Features

- Small package: 24 pin QSOP
- Drives multiple tubes
- Automatically checks for common fault conditions
- 7.0V < Vbatt < 24V
- Low component count
- Low Idd < 3.5mA
- <1uA shutdown mode

■ Applications

- Notebook computers
- LCD/TFT displays

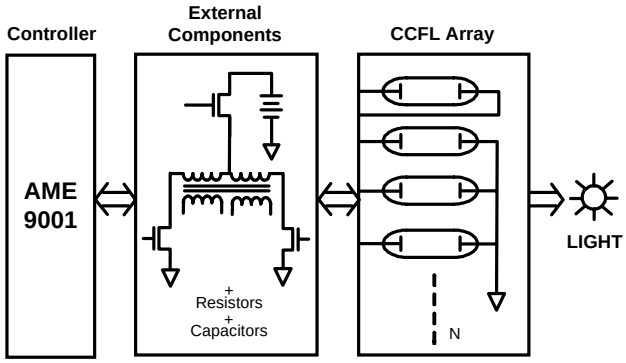
■ Pin Configuration



AME9001
24PIN QSOP

1. VREF
2. CE
3. SSC
4. RDELTA
5. FAULTB
6. RT2
7. VSS
8. OVP
9. CS
10. CSCOMP
11. CSDET
12. NC
13. OUTC
14. OUTAPB
15. OUTA
16. VBATT
17. VDD1
18. VDD
19. CT1
20. FB
21. COMP
22. BRIGHT
23. SSV
24. PNP

■ System Block Diagram



■ Pin Description

Pin #	Pin Name	Pin Description
1	VREF	Reference. Compensation point for the 3.4V internal voltage reference. Must have bypass capacitor connected here to VSS.
2	CE	Chip enable. When low (<0.4V) the chip is put into a low current (~0uA) shutdown mode.
3	SSC	Blanking interval ramp. During the first cycle this pin sources 1μA. During subsequent cycles it sources 150μA. This is primarily used to provide a "blanking interval" at the beginning of every dimming cycle to temporarily disable the fault protection circuitry. (See application notes.)
4	RDELTA	A resistor connected from this pin to VBATT modulates the switching frequency as a function of battery voltage.
5	FAULTB	0.1 μF cap to VSS.
6	RT2	A resistor from this pin to VSS sets the minimum frequency of the VCO. The voltage at this pin is 1.5V
7	VSS	Negative supply. Connect to system ground.
8	OVP	Over voltage protection input. Indirectly senses the voltage at the secondary of the transformer through a resistor (or capacitor) divider. It will immediately turn the circuit off if the voltage at OVP is over 3V. It will also turn the chip off if the voltage at OVP is less than 250mV for 4 successive clock cycles after the voltage at SSC has risen above 3V (SSC>3V).
9	CS	Negative input of the auxiliary error amplifier(EA2). In this application it is normally shorted to CSCOMP
10	CSCOMP	Output of the auxiliary error amplifier(EA2). In this application the auxiliary error amp is in a unity gain configuration and the voltage at CSCOMP =1.25V as long as SSC > 1.25V. Otherwise CSCOMP is clamped to the voltage at SSC.
11	CSDET	Current sense detect. Connect this pin to the CCFL current sense resistor divider. If this pin is below 250mV for 4 consecutive clock cycles after SSC > 3V then the circuit will shutdown.
12	NC	Must float.
13	OUTC	Drives one of the external NFETs, opposite phase of OUTAPB.
14	OUTAPB	Drives one of the external NFETs, opposite phase of OUTC.
15	OUTA	Drives the high side PFET.
16	VBATT	Battery input. This is the positive supply for the OUTA driver.
17	VDD1	Must be tied to VDD.
18	VDD	Regulated 5V supply input.
19	CT1	Sets the dimming cycle frequency. Usually about 100Hz.
20	FB	Negative input of the voltage control loop error amplifier.
21	COMP	Output of the voltage control loop error amplifier.
22	BRIGHT	Brightness control input. A DC voltage on this controls the duty cycle of the dimming cycle. This pin is compared to a 3V ramp at the CT1 pin.
23	SSV	Soft start ramp for the voltage control loop. (20uA source current.)
24	PNP	Drives the base of an external PNP transistor used for the 5V LDO.

■ Ordering Information

Part Number	Marking	Output Voltage	Package	Operating Temp. Range
AME9001AETH	AME9001AETH xxxxxxxxHN yyww	N/A	QSOP-24	- 40°C to + 85°C

" xxxxxxxx HN " for Internal code

■ Absolute Maximum Ratings

Parameter	Maximum	Unit
Battery Voltage (VBATT)	25	V
ESD Classification	B	

Caution: Stress above the listed absolute maximum rating may cause permanent damage to the device

■ Recommended Operating Conditions

Parameter	Rating	Unit
Battery Voltage (VBATT)	7 - 24	V
Ambient Temperature Range	- 40 to + 85	°C
Junction Temperature	- 40 to + 125	°C

■ Thermal Information

Parameter	Maximum	Unit
Thermal Resistance (QSOP - 24)	325	°C / W
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (10 Sec)	300	°C

■ Electrical Specifications

TA= 25°C unless otherwise noted, VBATT = 15V, CT1 = 0.01uF, RT2 = 56K

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
5V supply (VSUPPLY)						
Output voltage	V_{DD}		4.9	5.15	5.35	V
Line regulation	V_{DDLINE}	7<Vbatt<24	-0.5		0.5	%
Load regulation	V_{DDLOAD}	Vbatt=7V, 0mA < Iload < 25mA	-0.2		0.2	%
Temperature drift	V_{DDTC}	-10C < Ta < 70C		0.5		%
3.4V reference (VREF)						
Initial voltage	V_{REF}	Vbatt = 15V, Iref = 0	3.25	3.4	3.525	V
Line regulation	$V_{REFLINE}$	7< Vbatt < 24V	-0.1		0.1	%
Temperature drift	V_{REFTC}	-10C <Ta < 70C		100		ppm/C
Brightness oscillator (CT1, BRIGHT)						
Ramp amplitude	V_{CT1}			3		V
Frequency	F_{CT1}		70		130	Hz
Line regulation	$LINE_{CT1}$	7< Vbatt < 24V	-0.5		0.5	%
Temperature drift	TC_{CT1}	-10C < Ta < 70C		=+-3		%
Comparator offset	VOS_{CT1}			10		mV
Vco oscillator (RT2, RDELTA)						
Initial frequency	$F_{VCO(OUTA)}$	RT2 = 56k	47		52	kHz
Line regulation	$LINE_{VCO}$	7< Vbatt < 24V	-0.8		0.8	%
Temperature drift	TC_{VCO}	-10C < Ta < 70C		+-0.5		%
VCO pullin range	$PULL_{VCO}$		RT2/(RDELTA X 5)			%
Error amplifiers (FB, COMP, CS, CSCOMP)						
Offset voltage, WRT Vref	V_{OS}		-40		40	mV
Input bias current	I_B			1		nA
Input offset current	I_{OS}			1		nA
Open loop gain	A_{OL}			70		dB
Unity gain frequency	F_T			1		Mhz
Output high voltage (comp)	V_{OH}	I_{SOURCE} = 50uA	3.39			V
Output low voltage	V_{OL}	I_{SINK} = 500uA			0.4	V
Output high voltage (cscomp)	V_{OH}	I_{SOURCE} = 50uA	4.77			V

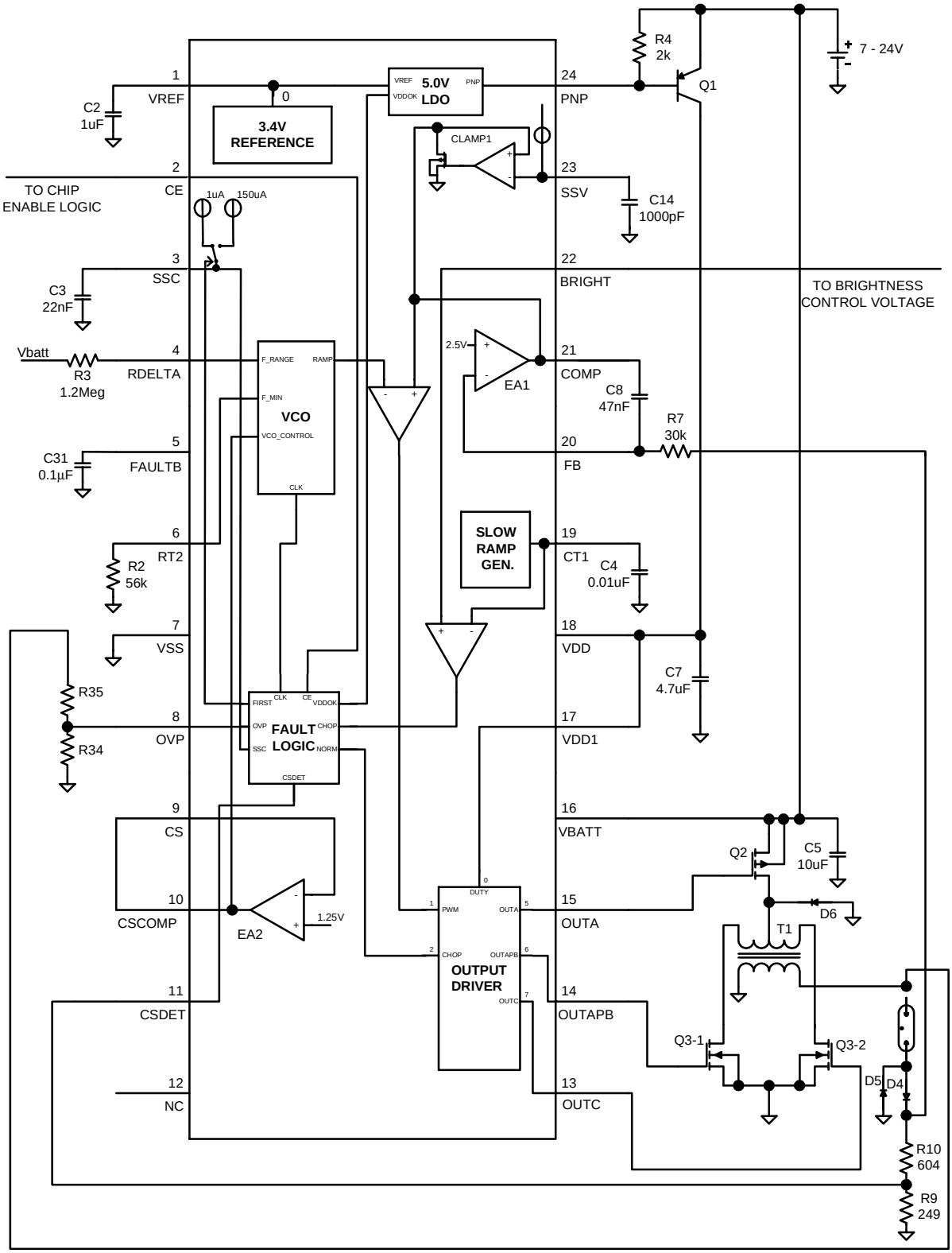
■ Electrical Specifications(contd.)

TA= 25°C unless otherwise noted, VBATT = 15V, CT1=0.01uF, RT2 = 56K

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output A (OUTA)						
Peak current	I_{PEAKA}			1		Amp
Output Low Voltage	V_{OL}	0.2mA			10.8	V
Output High Voltage	V_{OH}	-5mA	14.4			V
Other outputs (OUTAPB, OUTC)						
Peak current	I_{PEAKBC}			1		Amp
Output Low Voltage	V_{OL}	I_{SINK} = 10mA			0.25	V
Output High Voltage	V_{OH}	I_{SOURCE} = 10mA	VDD - .7			V
Soft start clamps (SSC, SSV)						
Initial SSC current	$I_{SSCINIT}$		0.4		1.2	uA
Normal SSC current	I_{SSC}		107		180	uA
SSV current	I_{SSV}		13		25	uA
Other parameters						
CE high threshold	CE_{HIGH}		1.5			V
CE low threshold	CE_{LOW}				0.4	V
OVP high threshold	OVP_{HI}		3.2		3.55	V
OVP low threshold	OVP_{LO}		200		300	mV
CSDET threshold	V_{THCS}		200		300	mV
Average supply current	I_{BATT}	No FET gate current		2.5	6	mA
Average off current	I_{OFF}	In the application			10	uA

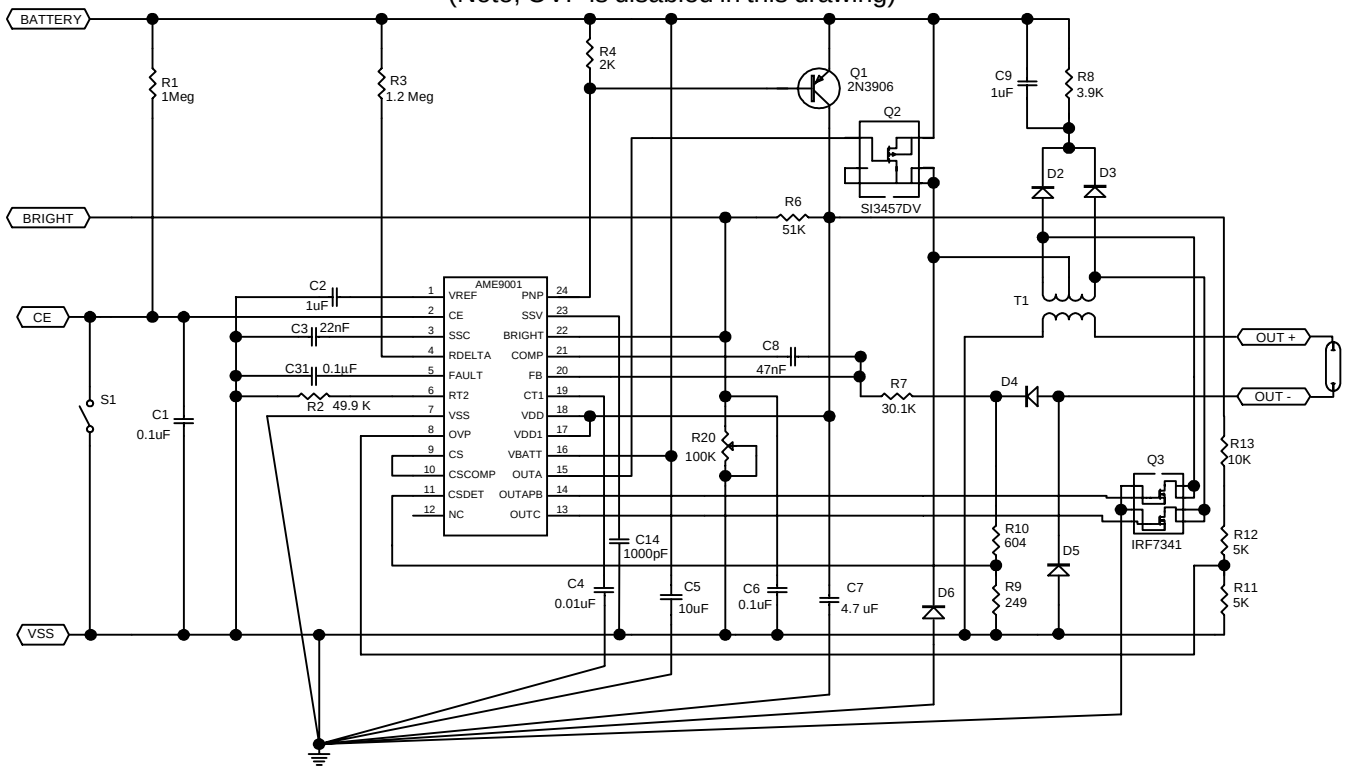
■ Block Diagram

Figure 1. AME9001 Block Diagram



■ Application Schematic

Figure 2. Single Tube Application Schematic (7V < Vbatt < 24V)
(Note, OVP is disabled in this drawing)



Bill of Materials

Part #	Value	Rating	Tolerance
R1	1Meg	1/16 watt	5%
R2	49.9k	1/16 watt	1%
R3	1.2Meg	1/16 watt	5%
R4	2k	1/16 watt	5%
R6	51k	1/16 watt	5%
R7	30.1k	1/16 watt	5%
R8	3.9k	1/4 watt	5%
R9	249	1/16 watt	1%
R10	604	1/16 watt	1%
R11	5k	1/16 watt	5%
R12	5k	1/16 watt	5%
R13	10k	1/16 watt	5%
R20	100k	pot.	

Q1	2N3906	30V	
Q2	Si3457DV	30V	
Q3	IRF7341	60V	

Part #	Value	Rating	Tolerance
C1	0.1uF	25V	20%
C2	1.0uF	6V	20%
C3	22nF	6V	5%
C4	0.01uF	6V	5%
C5	10uF	25V	20%
C6	0.1uF	6V	20%
C7	4.7uF	6V	20%
C8	47nF	6V	5%
C9	1.0uF	25V	10%
C31	0.1uF	6V	20%
D2	1N914		
D3	1N914		
D4	1N914		
D5	1N914		
D6	1N914		
T1	20:20:2200		

■ Application Notes

Overview

The goal of the AME9001 application circuit is to drive a CCFL (cold cathode fluorescent lamp) with a high voltage sine wave in order to produce an efficient and cost effective light source. The most common application for this will be as the backlight of either a notebook computer display, flat panel display, or personal digital assistant (PDA).

The CCFL tubes used in these applications are usually glass rods about a foot long and 0.125”-0.25” in diameter. Typically they require a sine wave of 600V and they run at a current of several milliamperes. However, the starting (or striking) voltage can be as high as 2000V. At start up the tube looks like an open circuit, after the plasma has been created the impedance drops and current starts to flow. The IV characteristic of these tubes is highly non-linear.

Traditionally the high voltage required for CCFL operation has been developed using some sort of transformer-LC tank circuit combination driven by several small power mosfets. The AME9001 application uses one external PMOS, 2 external NMOS and a high turns ratio transformer with a centertapped primary. Lamp dimming is achieved by turning the lamp on and off at a rate faster than the human eye can detect. These "on-off" cycles are known as dimming cycles.

Steady State Circuit Operation

Figure 1 (and 2) shows PMOS Q2 driving the center tap primary of T1. The gate drive of Q2 is a pulse width modulated (PWM) signal that controls the current into the transformer primary and by extension, controls the current in the CCFL. The gate drive signal of Q2 drives all the way up to the battery voltage and down to 7.5 volts below Vbatt so that logic level transistors may be used without their gates being damaged. An internal clamp prevents the Q2 gate drive (OUTA) from driving lower than Vbatt-7.5V.

NMOS transistors Q3-1 and Q3-2 alternately connect the outside nodes of the transformer primary to VSS. These transistors are driven by a 50% duty cycle square wave at one-half the frequency of the drive signal applied to the gate of Q2.

Figure 3 illustrates some ideal gate drive waveforms for the CCFL application. Figure 4 and 5 are detailed views of the power section from Figures 1 and 2. Figure 5 has the transformer parasitic elements added while Figure 4 does not. Referring to Figures 4 and 5, NMOS transistors Q3-1 and Q3-2 are driven out of phase with a 50% duty cycle signal as indicated by waveforms in Figure 3. The frequency of the NMOS drive signals will be the frequency at which the CCFL is driven. PMOS transistor, Q2, is driven with a pulse width modulated signal (PWM) at twice the frequency of the NMOS drive signals. In other words, the PMOS transistor is turned on and off once for every time each NMOS transistor is on. In this case, when NMOS transistor Q3-1 and PMOS transistor Q2 are both on then NMOS transistor Q3-2 is off, the side of the primary coil connected to NMOS transistor Q3-1 is driven to ground and the centertap of the transformer primary is driven to the battery voltage. The other side of the primary coil connected to NMOS transistor Q3-2 (now “off”) is driven to twice the battery voltage (because each winding of the primary has an equal number of turns).

Current ramps up in the side of the primary connected to Q3-1 (the “on” transistor), transferring power to the secondary coil of transformer. The energy transferred from the primary excites the tank circuit formed by the transformer leakage inductance and parasitic capacitances that exist at the transformer secondary. The parasitic capacitances come from the capacitance of the transformer secondary itself, wiring capacitances, as well as the parasitic capacitance of the CCFL. Some applications may actually add a small amount of parallel capacitance (~10pF) on the output of the transformer in order to dominate the parasitic capacitive elements.

When the PMOS, Q2, is turned off, the voltage of the transformer centertap returns to ground as does the drain of NMOS transistor Q3-2 (the drain of Q3-2 was at twice the battery voltage). Halfway through one cycle, NMOS transistor Q3-1 (that was on) turns off and NMOS transistor Q3-2 (that was off) turns on. At this point, PMOS transistor Q2 turns on again, allowing current to ramp up in the side of the primary that previously had no current. Energy in the primary winding is transferred to the secondary winding and stored again in the leakage inductance L_{leak}, but this time with the opposite polarity. The current alternately goes through one primary winding then the other.

The duty cycle of PMOS transistor Q2 controls the amount of power transferred from the primary winding to the secondary winding in the transformer. Note that the CCFL circuit can work with PMOS transistor Q2 on constantly (i.e. a duty cycle of 100%), although the power would be unregulated in this case.

Figure 3. Idealized Gate Drive Waveforms

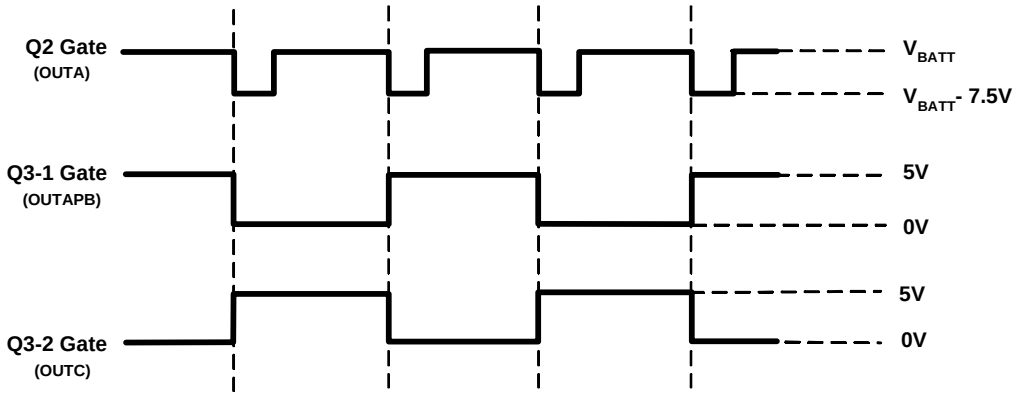


Figure 4.
Power Stage Single Tube Components
(Same component designations used as for Figures 1 and 2)

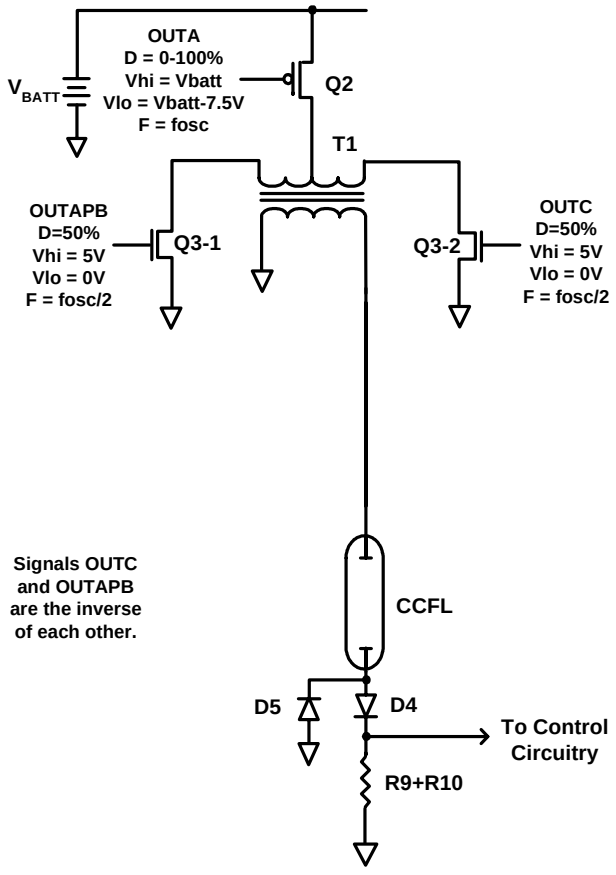
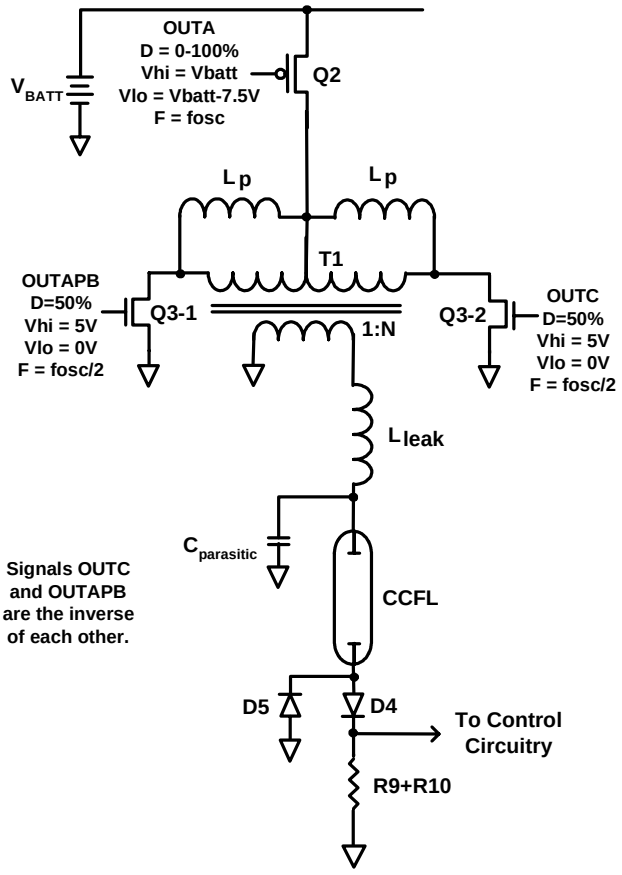


Figure 5.
Power Stage Single Tube Components with parasitic elements
(Same component designations used as for Figures 1 and 2)



Figures 6,7 illustrates various oscilloscope waveforms generated by the CCFL circuit in operation. These figures show that the duty cycle of the gate drive at Q2 decreases as the battery voltage increases from 9 V to 21 V (as one would expect in order to maintain the same output power).

The first three traces in Figures 6 and 7 show the gate drive waveforms for transistors Q2, Q3-1, and Q3-2, respectively. As mentioned before, the gate drive waveform for transistor Q2 drives up to the battery voltage but down only to approximately 7.5 V below the battery voltage. The fourth trace (in Figures 6,7) shows the voltage at centertap of the primary winding (it is also the drain of PMOS transistor, Q2). This waveform is essentially a ground to a battery voltage pulse of varying duty cycle. When the centertap of the primary is driven high, current increases through PMOS transistor, Q2 as indicated by the sixth trace down from the top. In region I the drain current of Q2 is equal and opposite to the drain current of Q3-1 since the gate of Q3-1 is high and Q3-1 is on. In region III the drain current of Q2 will be equal and opposite to the drain current of Q3-2 (not shown). In region II when PMOS transistor Q2 is switched off, the current through this transistor, after an initial sharp drop, ramps back down towards zero.

In Figures 6 and 7 the fifth trace down from the top shows the drain voltage of Q3-1. (The trace for NMOS transistor Q3-2, not shown, would be identical, but shifted in time by half a period.) The seventh trace down from the top shows the current through the NMOS transistor Q3-1, which is equal to the current in PMOS transistor Q2 for the portion of time that PMOS transistor Q2 is conducting (see region I, for example). As the current ramps up in the primary winding, energy is transferred to the secondary winding and stored in the leakage inductance L_{leak} (and any parasitic capacitance on the secondary winding). If the current in the NMOS transistor is close to zero when that NMOS transistor is turned off that means that the CCFL circuit is being driven close to its resonant frequency. If the circuit is being driven too far from its resonant point then there will be large residual currents in the transistors when they are turned off causing large ringing, lower efficiency and more stress on the components. So called "soft switching" is achieved when the MOS drain current is zero while the MOS is being turned off. The driving frequency and transformer parameters should be chosen so that soft switching occurs.

Once PMOS transistor Q2 completes one on/off cycle, it is repeated again with the alternate NMOS transistor conducting. This complementary operation produces a symmetric, approximately sinusoidal waveform at the input to the CCFL load, as shown by the bottom trace in Figures 6 and 7.

The operation of the CCFL circuit can be divided into 4 regions (I, II, III, and IV) as shown in Figures 6 and 7. Figure 8-1 shows the equivalent transformer and load circuit model for region I. During region I, one of the primary windings is connected across the battery, the current in that winding increases and energy is coupled across to the secondary. No current flows in the other winding because its NMOS is turned off and its body diode is reverse biased. The drain of that NMOS stays at twice the battery voltage because both primary windings have the same number of turns and the battery voltage is forced across the other primary winding.

Figure 8-2 shows the equivalent transformer and load circuit model for region II. During region II, the battery is disconnected from the primary winding. In this configuration, current flows through both of the primary windings. The current decreases very quickly at first then ramps down to zero at a rate that is slower than the current ramped up. The initial drop is due to the almost instantaneous change in inductance when current flow shifts from one portion of the primary winding to both portions of the primary.

Figure 8-3 shows the equivalent transformer and load circuit model for region III. During region III, the primary winding opposite from the one used in region I is connected across the battery, increasing current in that primary winding but in a direction opposite to that of region I. Energy is coupled across to the secondary as in region I but with opposite polarity. No current flows in the undriven winding because its NMOS is turned off and its body diode is reverse biased. The drain of that NMOS stays at twice the battery voltage because both primary windings have the same number of turns and the battery voltage is forced on the other primary. Region III is, effectively, the inverse of region I.

Figure 8-4 shows the equivalent transformer and load circuit model for region IV. During region IV, the battery is disconnected from the primary winding. In this configuration, current flows through both of the primary windings with opposite polarity to that in region II. The current decreases very quickly at first then ramps down to zero at a rate that is slower than the current ramped up. Once again, the initial drop is due to the effective change in inductance when current flow shifts from one portion of the primary winding to both portions of the primary. Region IV is effectively the inverse of region II.

Figure 6. Typical Waveforms V_{BATT}=9V

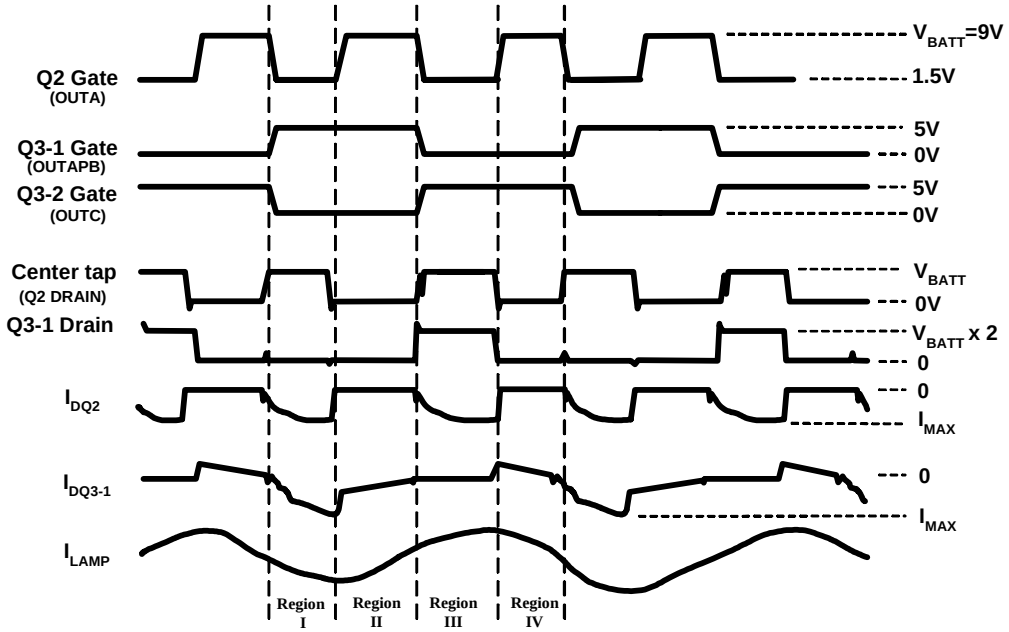


Figure 7. Typical Waveforms V_{BATT}=21V

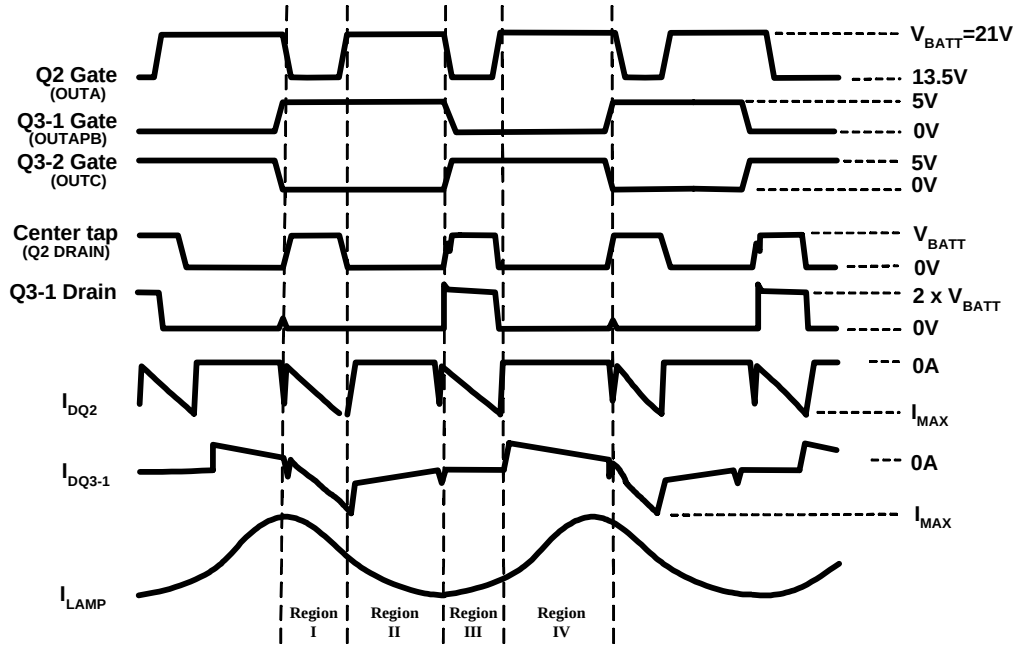


Figure 8-1. Region I

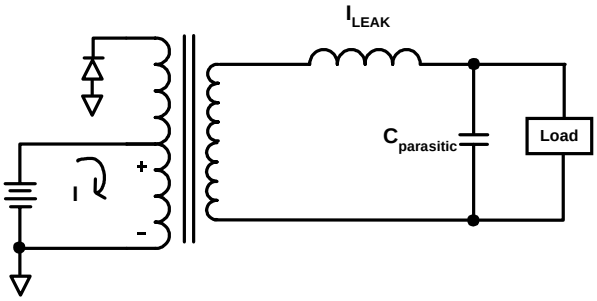


Figure 8-2. Region II

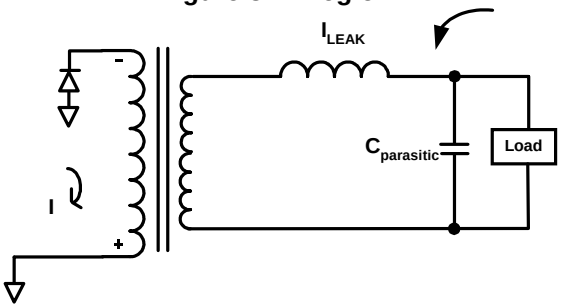


Figure 8-3. Region III

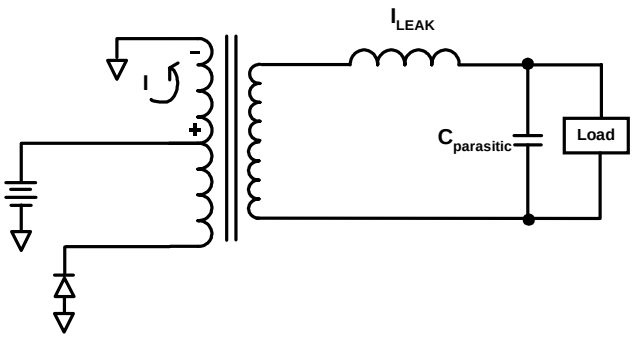


Figure 8-4. Region IV

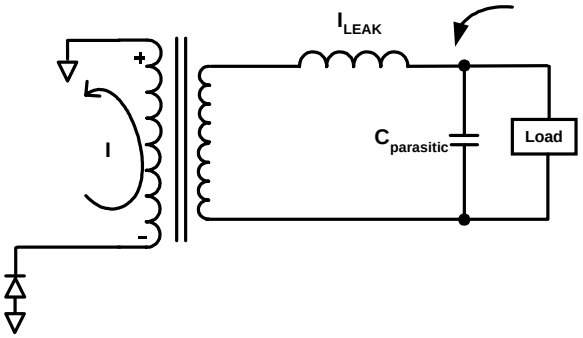
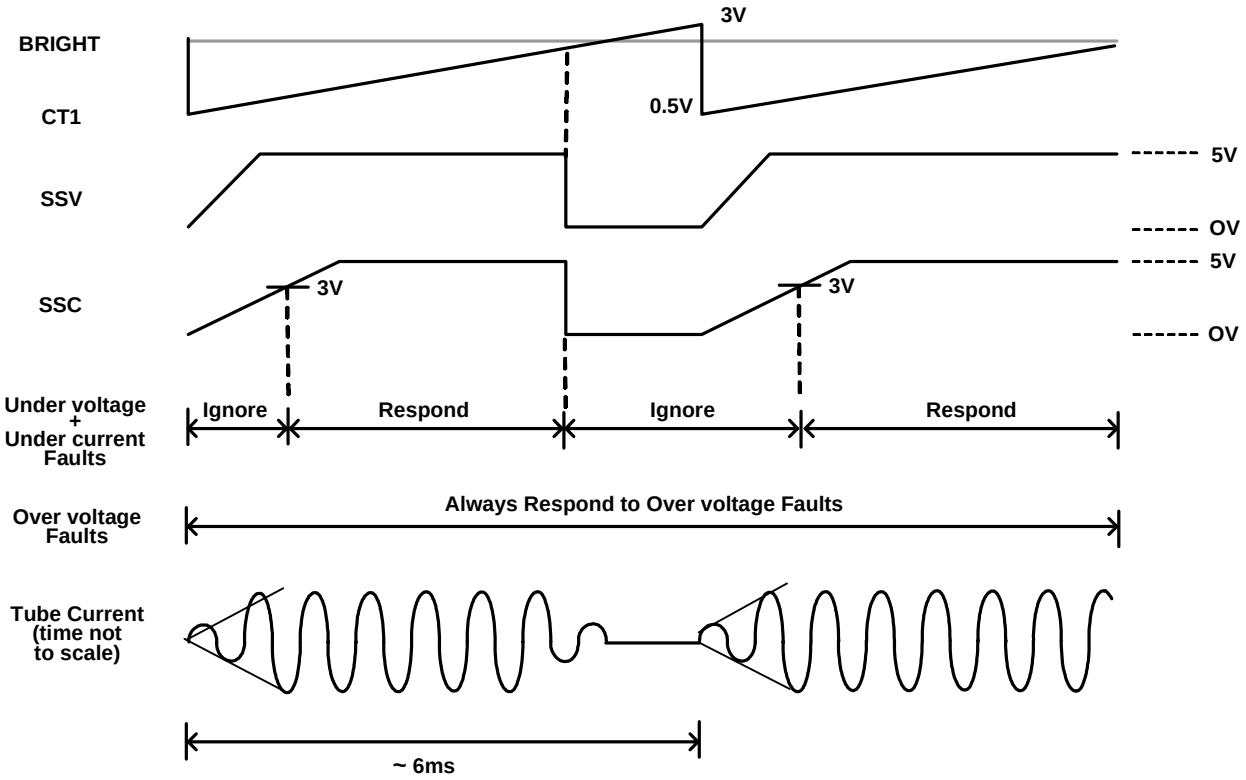


Figure 9. Steady State Dimming Waveforms (1st Cycle Not Show)



Driving the CCFL

Unlike other conventional schemes for driving CCFLs the secondary winding of the AME9001 method is not designed to look like a voltage source to the CCFL lamp. The circuit acts more like a current source (or a power source). The circuit will increase the duty cycle of Q2 thereby dumping more and more energy across to the secondary tank circuit until the CCFL tube current achieves regulation or one of the various fault conditions is met. There is no special "striking period" as is necessary with some other schemes.

When the circuit starts driving the transformer there is initially no arc struck in the CCFL. The CCFL load looks like an open circuit. The voltage across the CCFL will increase with each successive cycle. Two events may then happen:

1) The gas inside the CCFL will ionize, the voltage across the CCFL will drop, the current through the CCFL will increase, and a stable steady state operating point will be reached.

OR....

2) One of the three fault conditions will be met shutting down the circuit:
   a) The CCFL tube voltage continues to rise until the OVP pin is higher than 3.5V at which point the circuit will shut down.
   b) The CCFL voltage fails to rise high enough to keep the undervoltage portion of the OVP pin from tripping.
   c) The CCFL current fails to rise high enough to keep the undercurrent threshold at the CSDET pin from tripping.

Note that condition a) can be met at any time while the AME9001 is enabled. Condition b) and c) can only be met after the SSC pin has crossed 3V AND four successive undervoltage events occur in a row. The SSC pin is pulled to VSS everytime the lamp is turned off, whether for a dimming cycle, user shutdown or fault occurrence. It ramps up slowly depending on the size of capacitor C3 connected to the SSC pin. The period of time when the b) and c) fault checks are disabled is called the "blanking" time. The blanking time occurs from the time SSC starts to ramp up until it reaches 3V. See Figure 9 for some idealized waveforms illustrating the behavior just described.

Control Algorithm

There are 2 major control blocks (loops) within the IC. The first loop controls the duty cycle of the driving waveform. It senses the CCFL current (Figure 1 or 2, resistor R9 and R10) rectifies it, integrates it against an internal reference and adjusts the duty cycle to obtain the desired power. This loop uses error amplifier EA1 whose negative input is pin FB and whose output is COMP. The positive input of EA1 is connected to a 2.5V reference. External components, R7 and C8, set the time constant of the integrator, EA1. In order to slow the response of the integrator increase the value of the product (R7 X C8).

The second control block adjusts the brightness by turning the lamp on and off at varying duty cycles. Each time the lamp turns on and off is referred to as a “dimming cycle”. At the end of each dimming cycle the SSV pin is pulled low, this forces COMP low as well due to the clamping action of Clamp1 shown in Figure 1. At the beginning of a new dimming cycle COMP tries to increase quickly but it is clamped to the voltage at the SSV(soft-start voltage) pin. A capacitor on the SSV pin (C8, Figure 1), which is discharged at the end of every dimming cycle, sets the slew rate of the voltage at the SSV pin, and hence also the maximum positive slew rate of the COMP pin. [“Dimming cycle” is explained more fully below]

The BRIGHT and CT2 pins

A user-provided voltage at the BRIGHT pin is compared with the ramp voltage at the CT1 pin (See Figure 10). As the voltage at BRIGHT increases the duty cycle of the dimming cycle (and the brightness of the CCFL) increase. The frequency of the dimming cycles is set by the value of the capacitor at pin CT1 (C4 in Figure 1 and 2) and it is also proportional to the current set by resistor R2. Setting C4 equal to 0.01uF and R2 equal to 47.5k yields a dimming cycle frequency of approximately 125Hz. The frequency should vary inversely with the value of C4 according to the relation:

$$\text{Frequency(Hz)} = 1/[17 \times R2 \times C4]$$

The brightness may also be controlled by using a variable resistor in place of R10 (See Figure 11). In this case the BRIGHT pin should be pulled to VDD so that the CCFL remains on constantly. This method can lead to flicker at low intensities but it is easy to implement. Harmonic distortion may also increase since the duty cycle of the waveform at the gate of Q2 will vary greatly with brightness. When using burst brightness control the duty cycle of the driving waveforms should not vary because the CCFL is running at 100% power or it is turned off. As long as the battery voltage does not change the duty cycle of the driving waveform also does not change greatly. This means that harmonic distortion can be minimized by optimizing the frequency and transformer characteristics for a particular duty cycle rather than a large range of duty cycle.

Figure 10. Duty Cycle Dimming

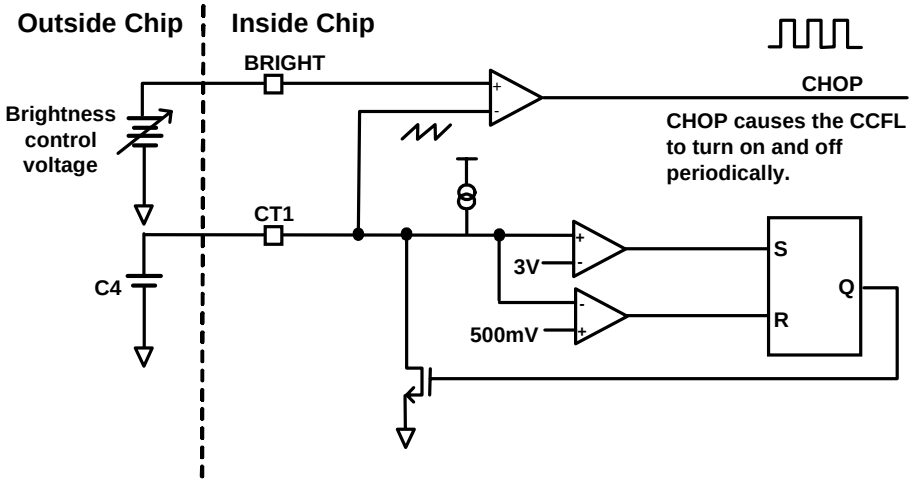
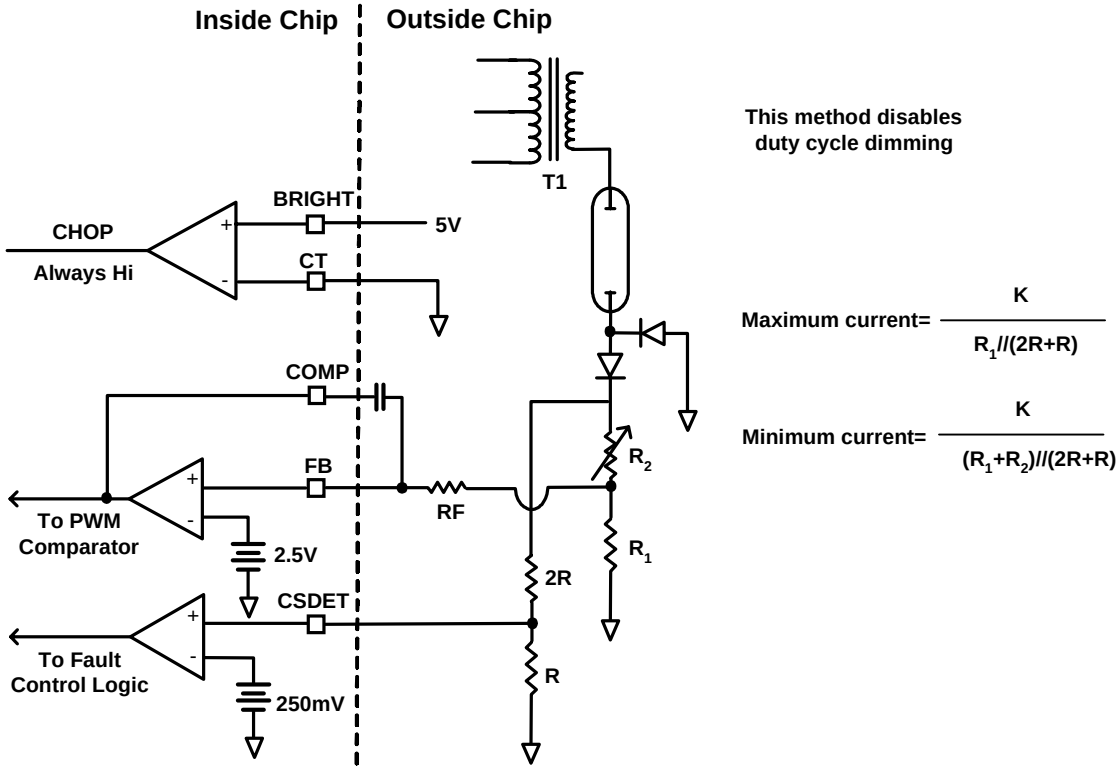


Figure 11. Alternative Brightness Control



RT2, RDELTA pin

The frequency of the drive signal at the gate of Q2 is determined by the VCO shown in Figure1. A detail of the VCO is shown in Figure 12. The user sets the minimum oscillator frequency with the resistor connected to pin RT2 (R2 in the figures). The relation is:

Frequency (Hz) = 2.8E9 / R2 (ohms)

You can see from the formula that as R2 is increased the frequency gets smaller.

All other things being equal, as the battery voltage increases the duty cycle of the driving waveform at the gate of Q2 decreases. Often the waveform becomes less sinusoidal as the duty cycle decreases. To avoid this unwanted effect and to ensure that the FETs remain in a "soft switching mode" the application described here adjusts the oscillator frequency upwards as the battery voltage increases. An increase in driving frequency is desirable to minimize harmonic distortion of the output waveform as the duty cycle of the drive signal at the gate of Q2 decreases. Resistor R3 controls how much the oscillator frequency increases as a function of battery voltage. The relationship is:

Delta frequency (Hz) = 3.44E8 * (Vbatt -1.25) / R3

You can see from the formula that the frequency will increase as the battery voltage increases. The amount of this increase is set by R3. In the current application EA2 (Figure 1) is connected in unity gain which will provide a constant 1.25V at the CSCOMP pin and subsequently at the Vco_control and Rdelta input of the VCO. Even though Vco_control is a fixed voltage the frequency of the VCO still modulates because the current through R3 changes as the battery voltage increases and hence increases the charging current into the timing capacitor of Figure 12 thereby increasing the oscillator frequency.

Supply voltage pins, VDD and PNP

Most of the circuitry of the AME9001 works at 5V with the exception of one output driver. That driver (OUTA) and its power pad (VBATT) must operate up to 24V although the OUTA pad may never be forced lower than 8 volts away from the VBATT pin. The OUTA pin is internally clamped to approximately 7.5 volts below the Vbatt pin.

The AME9001 uses an external PNP device to provide a regulated 5V supply from the battery voltage (See Figure 13). The battery voltage can range from 7V< VBATT < 24V. The PNP pin drives the base of the external PNP device, Q1. The VDD pin is the 5V supply into the chip. A 4.7uF capacitor, C7, bypasses the 5V supply to ground. If an external 5V supply is available then the external PNP would not be necessary and the PNP pin should float.

When the CE pin is low (<0.4V) the chip goes into a zero current state. The chip puts the PNP pin into a high impedance state which shuts off Q1 and lets the 5V supply collapse to zero volts. When low, the CE pin also immediately turns PMOS transistor Q2 off, however transistors Q3-1 and Q3-2 will continue to switch until the 5V has collapsed to 3.5V. Allowing the Q3 transistors to continue to switch for some time after Q2 is turned off permits the energy in the tank circuit to be dissipated gradually without any large voltage spikes.

The VDD voltage is sensed internally so that the switching circuitry will not turn on unless the VDD voltage is larger than 4.5V and the internal reference is valid. Once the 4.5V threshold has been reached the switching circuitry will run until VDD is less than 3.5V (as mentioned before).

Output drivers (OUTA, OUTAPB, OUTC)

The OUTAPB and OUTC pins are standard 5V CMOS driver outputs (with some added circuitry to prevent shoot through current). The OUTA driver is quite different (See Figure 14). The OUTA driver pulls up to VBATT (max 24V) and pulls down to about 7.5 volts below VBATT. It is internally clamped to within 7.5V of VBATT. On each transition the OUTA pad will sink/source about 500mA for 100nS. After the initial 100ns burst of current the current is scaled back to 1mA(sinking) and 12mA(sourcing). This technique allows for fast edge transitions yet low overall power dissipation.

Fault Protection, the OVP and CSDET pins

The AME9001 checks for 3 different fault conditions. When any one of the fault conditions is met then the circuit is latched off. Only a power on reset or toggling the CE pin will restore the circuit to normal operation. (See Figure 15 for a schematic of the FAULT circuitry.)

The first fault condition check can be used to detect overvoltages at the CCFL. Specifically, if the OVP pin is above 3V then this fault condition is detected. The first fault condition is always enabled, thus there is no blanking period, or 4 succesive faults required for shutdown.

The second fault condition check can be used to ensure that the CCFL voltage is above some certain voltage

level on a cycle by cycle basis. If the OVP pin does not cross its 250mV threshold once during four successive clock periods in a row then this fault will be triggered. This protection is disabled while the SSC ramp is below 3V such as during the initial start up and at the beginning of every dimming cycle. The 1st SSC ramp after power on reset (or CE enabled) is 150 times slower than subsequent start up ramps. This slow first ramp allows more time for a cold tube to strike before the chip senses a fault and shuts down.

In order to enable the first two fault condition checks then the OVP pin must, indirectly, sense the high voltage at the input of the CCFL. The actual CCFL voltage must be reduced by using either a resistor or capacitor divider such that in normal operation the voltage at OVP is higher than 250mV but lower than 3V.

The third fault condition check can be used to monitor the CCFL current. Specifically, it checks whether the voltage at the CSDET pin is higher than 250mV. If CSDET does not cross its 250mV threshold once during 4 successive clock cycles then this fault will be triggered. This protection is disabled while the SSC ramp is below 3V, such as during the initial start period, and at the beginning of every subsequent dimming cycle. This fault condition is used to check that a reasonable minimum amount of current is flowing in the tube.

Please note that the application circuit of Figure 2 uses a resistor divider to drive the OVP pin to a voltage above 250mV but below 3V. That effectively disables the first two fault condition checks. Some applications may not require all 3 fault condition checks. The third fault condition is usually sufficient to detect open circuit faults.

Figure 15 is a simplified schematic of the fault protection circuitry used in the AME9001. Most of the signals have been previously defined however some need a little explanation. The VDDOK signal is a power OK signal that goes high when the 5V supply (VDD) is valid. The CHOP signal stops the operation of the switching circuitry once every dimming cycle for burst mode brightness control. The output signal, FIRST, is high during the first burst cycle after power is turned on. It causes the SSC pin to source 150 time less current than on subsequent dimming cycles. The NORM signal is an enable signal to the switching circuitry. When it is high the circuit works normally. When it is low the switching circuitry stops.

SSC and SSV pins

The SSC pin's primary role is to define a time period in which the 2nd and 3rd fault condition (previously described) are disabled. This period of time is called the blanking interval. During the initial start up period after a power on reset or just after a low to high transition on the CE pin the SSC pin sources 1uA into an external capacitor(C3). The voltage on SSC ramps upwards towards VDD. The blanking interval is defined as the time during which V(SSC) < 3V. Once the voltage at SSC crosses 3V the blanking interval is finished and all three fault condition checks are enabled. At the beginning of the next dimming cycle the SSC pin is pulled to VSS then allowed to ramp upwards again, however during all subsequent dimming cycles the SSC pin sources 150uA instead of 1uA as was the case of the first cycle.

In effect, the two different sourcing currents means that the first blanking interval is 150 times as long as all subsequent blanking intervals. This allows a cold tube more time to strike before shutting down due to an undercurrent or undervoltage fault. (Please see figure 9 for further clarification of the blanking function.)

The SSV pin (like the SSC pin) is pulled to ground at the beginning of every dimming cycle then sources 20uA into an external capacitor. This creates a 0 to 5 volt ramp at the SSV pin. This ramp is used to limit the duty cycle of the PWM gate drive signal available at the OUTA pin. The SSV pin accomplishes duty cycle limiting by clamping the COMP voltage to no higher than the SSV voltage. Because the magnitude of the COMP voltage is proportional to the duty cycle of the PWM signal at OUTA the duty cycle starts each dimming cycle at zero and slowly increases to its steady state value as the voltage at SSV increases. (Figure 9 shows this operation.)

This type of duty cycle limiting is commonly called "soft-start" operation. Soft start operation lessens overshoot on start up because the power increases gradually rather than immediately.

Unlike the SSC pin the current sourced by the SSV pin remains approximately 20uA during ALL dimming cycles.

Ringing

Due to the leakage inductances of transformer T1 voltages at the drains of Q3 can potentially ring to values substantially higher than the ideal value (which is twice the battery voltage). The application schematic in figure 2 uses a snubbing circuit to limit the extent of the ringing voltage. Components C9,R8,D2 and D3 make up the snubbing circuit. The nominal voltage at the common

node is approximately twice the battery voltage. If either of the drains of Q3 ring above that voltage then diodes D2 or D3 forward bias and allow the ringing energy to charge capacitor C9. Resistor R8 bleeds off the extra ringing energy preventing the voltage at the common node from increasing substantially higher than twice the battery voltage. The extra power dissipation is:

$$P(dissipated) = Vbatt^2 / R8$$

For the example, in Figure 2, the power dissipation of the snubber circuit with Vbatt=15V is 58mW or approximately 1% of the total input power. The value of R8 can be optimized for a particular application in order to minimize dissipated power.

Excessive ringing is usually a sign that the driving frequency is not well matched to the resonant characteristics of the tank circuit. In a well designed application a snubber circuit will not be necessary.

Layout Considerations

Due to the switching nature of this circuit and the high voltages that it produces this application can be sensitive to board parasitics. In fact, one of the advantages, of this design is that the circuit uses the parasitic elements of the application as resonant components, thus eliminating the need for more added components.

Particular care must be taken with the different gounding loops. The best performance has been obtained by using a “star” ground technique. The star technique returns all significant ground paths back to the center of the “star”. Ideally we would place the center of the star directly on the VSS pin of the AME9001. The bypass capacitors would, ideally, be connected as close to the center of the star as possible. The schematic in Figure 2 attemps to show this star ground configuration by bringing all the ground returns back to the same point on the drawing. Separate ground returns back to the star are especially important for higher current switching paths.

Figure 12. VCO Detail

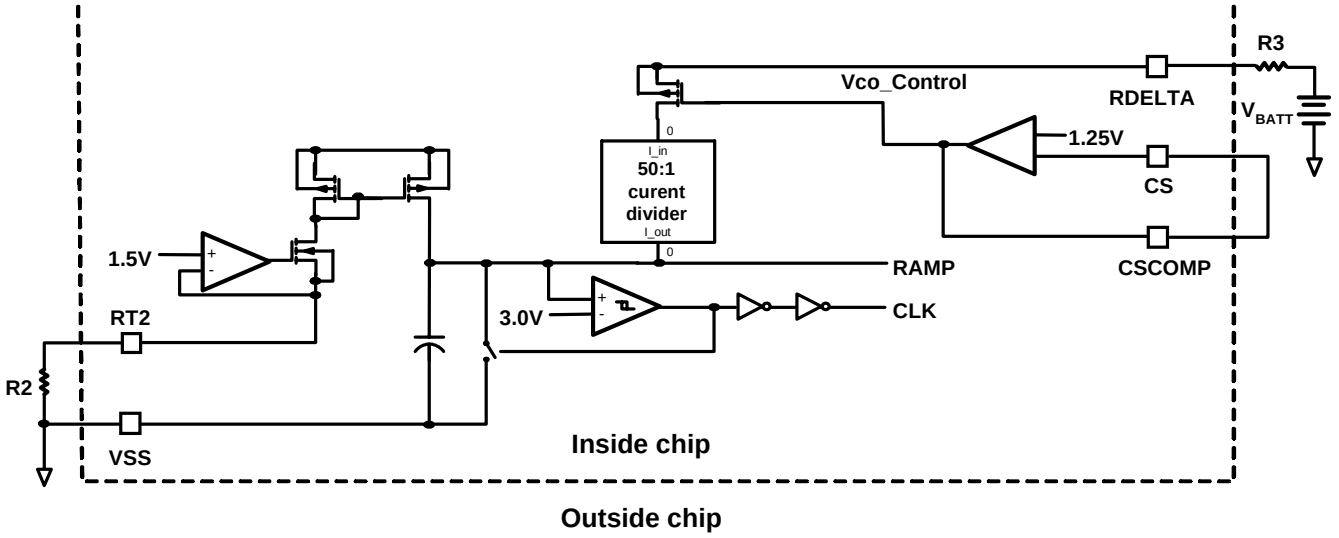


Figure 13. LDO Detail

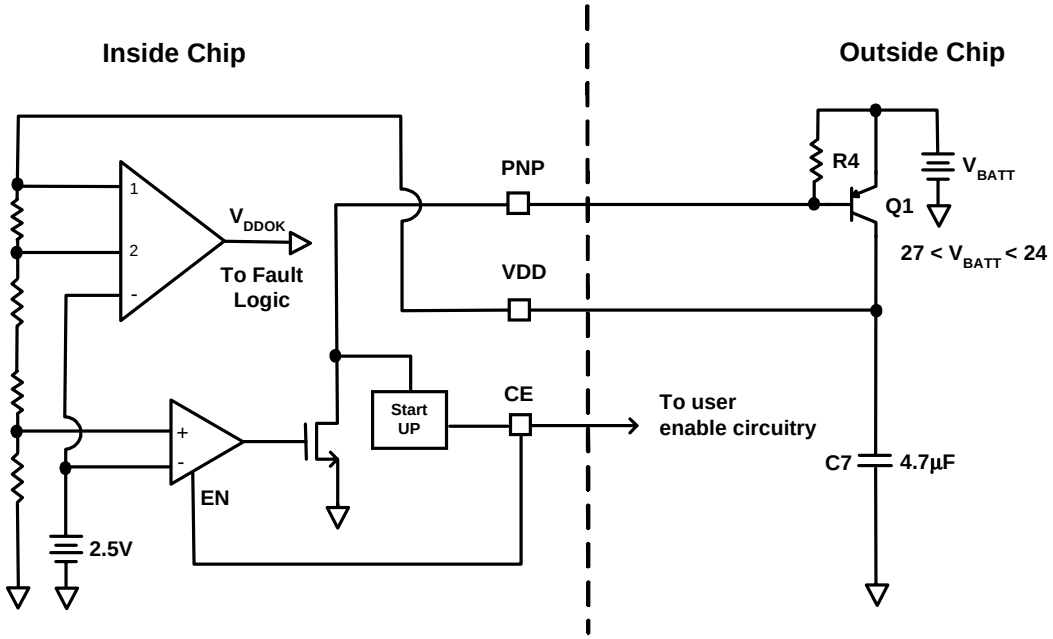


Figure 14. OUTA Driver Circuitry

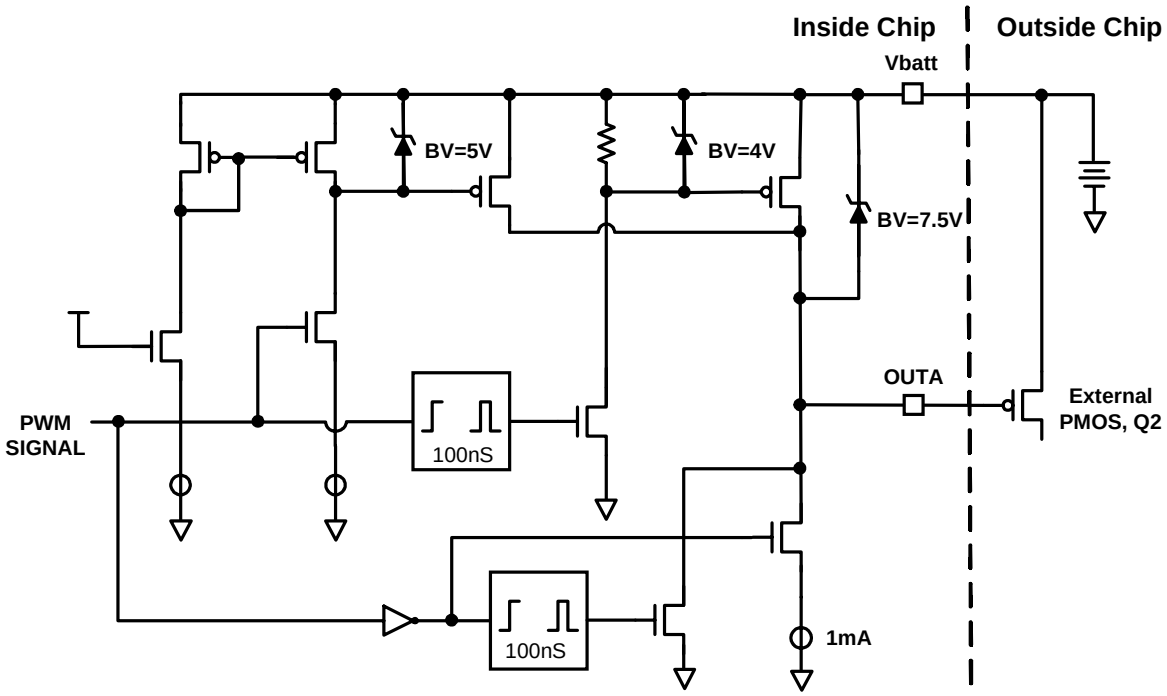
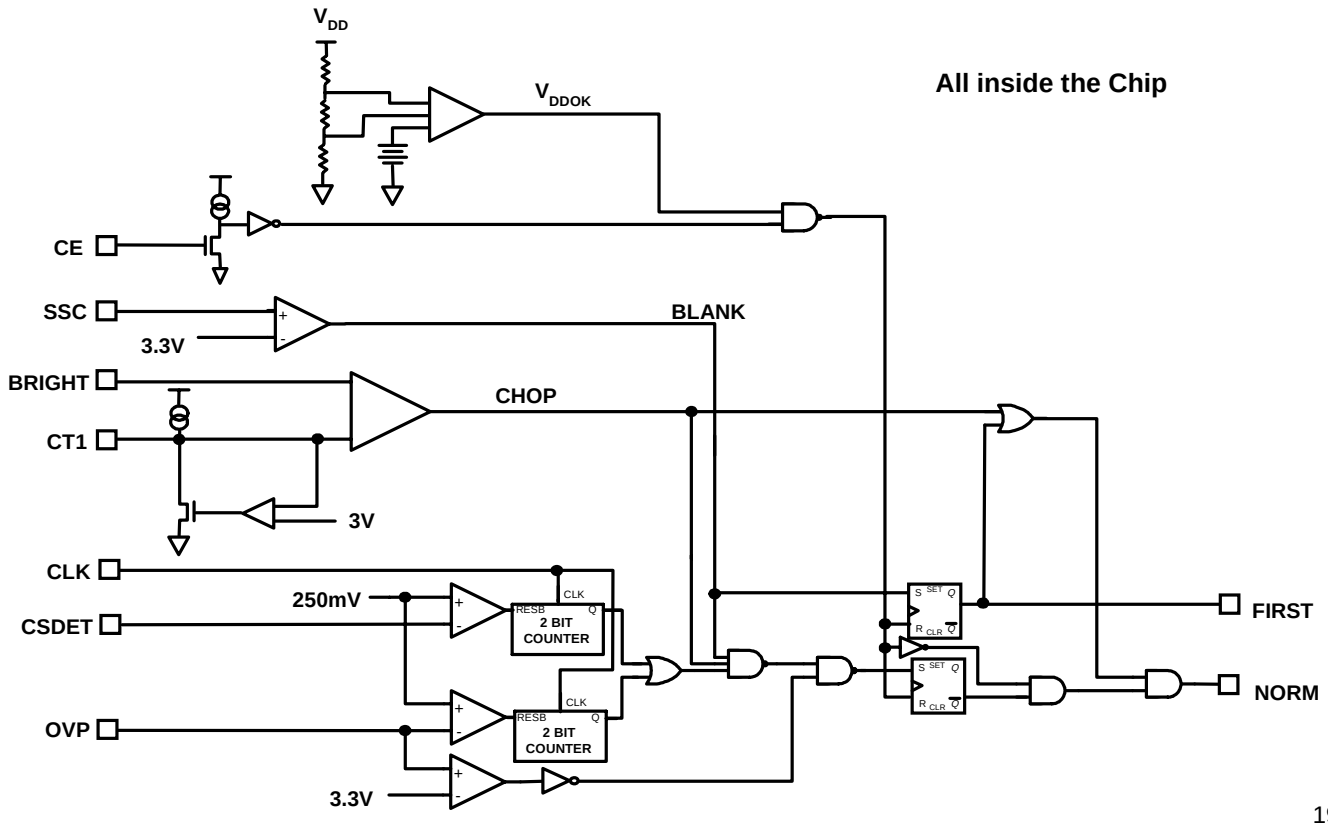


Figure 15. Fault Logic



Application Component Description

Figure 2 shows one typical application circuit for single tube drive. Figure 16 shows a similar application circuit that is optimized for 4 tube operation. Similar component designations are used on similar components both in figure 2 and figure 16 as well as throughout this application note.

R1 - Weak pull up for the chip enable (CE) pin. The voltage at CE will normally rise to 5 volts for a 12V supply. Pull down on the CE node to disable the chip and put it into a zero Idd mode. If the user wishes to drive node CE with 3.3 or 5.5 volt logic then R1 is not necessary

C1 - This capacitor acts to de-bounce the CE pin and to slow the turn on time when using R1 to pull up CE. This can be useful when the battery power is disconnected from the circuit in order to turn the circuit off, when the battery is reconnected the chip does not immediately turn on which allows the battery voltage to stabilize before switching starts. If the user is actively driving the CE pin then the C1 capacitor may not be necessary.

R3 - This resistor connected to the RDELTA pin determines how much the oscillator frequency will change with battery voltage. The relation, which is found earlier in the text, is:

Delta frequency (Hz) = 3.44e8 * (Vbatt-1.25) / R3

C2 - This 1uF capacitor bypasses and stabilizes the internal reference

C3 - This capacitor determines the length of the blanking interval at the beginning of every dimming cycle and when the chip is first powered on. At the end of every dimming cycle this capacitor is discharged to VSS then allowed to charge up at a rate controlled by its internal current source and C3. When the voltage on C3 (pin SSC) crosses 3 volts the blanking interval is over and all fault checks are enabled. The charging current into C3 (out of pin SSC) is normally 150uA but for the very first cycle after the chip is enabled the current is only 1uA. So the blanking interval for the first cycle is:

T(seconds) =(C3) * (3volts) / (1e-6amps)

And for subsequent dimming cycles the blanking interval is:

T(seconds) = (C3) * (3volts) / (150e-6amps)

C31 - This capacitor is used to prevent chatter on the FAULTB pin during start up

R2 - R2 sets the frequency of the oscillator that drives the FETs. The relation between R2 and frequency, that was found previously in the text, is:

Frequency (Hz) = 2.8e9/R2
R2 = 56K yields approximately 50khz

Note: that this is the frequency of the NMOS(Q3) gate drive. The PMOS(Q2) gate drive is exactly twice this value.

C30 - This capacitor filters signals feeding the OVP pin. By increasing C30 the user makes the circuit less sensitive to fast overvoltage conditions.

R4 - This resistors pulls the base of Q1 up to Vbatt. Coupled with Q1 and C7 it is part of the 5V regulator that supplies the working power to the AME9001. When the PNP pin is turned off the base of Q1 is pulled high through R4, turning off Q1 and allowing the voltage at the VDD node (VSUPPLY) to decay towards zero.

Q1 - This common PNP transistor (2n3906 is adequate) forms part of the 5V linear regulator which supplies power to most of the AME9001.

R6 - This resistor, together with adjustable resistor R20, form a resistor divider that divides the regulated 5V down to some lower voltage. That lower voltage is used to drive the BRIGHT pin which, in turn, determines the duty cycle of the the dimming cycles and therefore the brightness of the lamps. If the user is driving the BRIGHT pin with his/her own voltage source then R6 and R20 are not necessary.

C6 - This capacitor bypasses the BRIGHT pin. A noisy BRIGHT pin can cause unwanted flicker.

R20 - see description of R6

C14 - This capacitor sets the slope of the soft-start ramp on pin SSV. The voltage at SSV limits the duty cycle of the Q2 gate drive signal available at pin OUTA. The voltage at the COMP node is internally clamped to the SSV node. Therefore the C14 cap limits how fast SSV, and hence, COMP can increase. The charging current out of SSV is approximately 20uA so the rate of change of the SSV voltage is:

SSV(Volts/sec) = (20e-6amps) / C14

C5 - This is the main battery bypass capacitor.

C4 - This capacitor sets the frequency of the dimming cycles according to the relation:

Dim Cycle Freq(Hz) = 1 / [(17) * (R2) * (C4)]

Note that the frequency is also a function of R2. So the frequency of the main oscillator and the frequency of the dimming oscillator are not independent.

C7 - This capacitor is the load capacitor for the 5V linear regulator. As such it also bypasses the 5V supply and should be laid out as close to the AME9001 as possible.

C8 - This capacitor, in combination with resistor R7, determines the time constant for the error amplifier (integrator) EA1. The integrator is the primary loop stabilizing element of the circuit. In general this application is tolerant of a large range of integrator time constants. Increase the (C8 X R7) product to slow down the loop response.

R7 - see C8

D6 - This diode can catch any negative going spikes on the drain of Q2. This diode is NOT strictly necessary. This is NOT a freewheeling diode such as in a buck regulator. Since the primary windings are tightly coupled to each other the body diodes of Q3-1 and Q3-2 keep their own drains clamped to VSS as well as the drain of Q2. The spikes that diode D6 may catch are of short duration and small energy.

Q2 - This is a PMOS device. By modulating its gate drive duty cycle the power into the transformer, and then into the load, can be controlled. The breakdown of this device must be higher than the highest battery voltage that the application will use. The peak current load is roughly twice the average current load.

Q3-1, Q3-2 - These are NMOS devices. They are driven alternately with 50% duty cycle gate drive. The frequency of the gate drive is one half of the gate drive frequency of Q2. The gate drive is from 0 to 5 volts. The breakdown voltage of these devices must be at least twice the highest battery voltage. Peak current is roughly twice the average supply current.

C9,R8,D2,D3 - These devices form a snubber circuit that can dissipate ringing energy. The snubber circuit is not strictly necessary. In fact a well designed circuit should not require these devices. (These elements were described in more detail earlier.)

R9, R10 - The sum of R9 and R10 sets the current in one CCFL tube. As the sum of R9 and R10 decreases the tube current goes up, as the sum of R9 and R10 increase the tube current goes down. The RMS tube current is roughly:

Irms = 6V / (R9 + R10)

R9 and R10 also form a voltage divider that drives the CSDET pin. The purpose of the voltage divider is to keep the maximum voltage at CSDET under 5 volts under all conditions. The CSDET pin checks to see if there is any current in the CCFL. If the voltage at CSDET is larger than 250mV once every clock cycle then the AME9001 assumes there is current in the CCFL and allows operation to continue.

D4,D5 - These diodes rectify the current through the CCFL to provide a positive voltage for regulation by the error amplifier, EA1.

The following components are only used for multiple tube operation:

Q4,Q5 - These bipolar devices buffer the gate of Q2. That allows Q2 to be made much bigger without dissipating more power or increasing the cost of the AME9001. Q4 is an NPN transistor and Q5 is a PNP transistor.

R35,R36,D16 - These devices form a voltage divider and rectifier combination to sense higher than normal

transformer operating voltages. (This operation is explained in more detail below.)

R38,R39,D17 - See R35,R36,D16 description above. You can diode "OR" as many of these divider/rectifier circuits as you have different transformers. Each time you add another double output transformer you must add another set of these resistors and diode networks. (This operation is explained in more detail in the next section.)

Multiple Tube Operation

The AME9001 is particularly well suited for multiple tube applications. Figure17 shows the power section of a two tube application. The major difference between this application and the single tube application is the addition of another secondary winding on the transformer. The primary side of the transformer and its associated FETs are exactly the same as the single tube case although the FETs may need to be resized due to the increased current in two tube applications.

The secondaries are wound so that the outputs to the CCFL are of opposite phase (see Figure 18). When the voltage at one secondary output is high (+600 volts) the other secondary output should be low (-600 volts). The other secondary terminals are connected to each other. In a balanced circuit the voltage at the connection of the two secondaries will, ideally, be zero. Of course in a real application the voltage at the connection of the two secondaries will deviate somewhat from zero.

The common connection of the secondaries offers us an excellent method to check for high voltage fault conditions. As previously mentioned, when the CCFL loads are balanced then the voltage at the common connection of the secondaries will remain relatively low compared to the high voltages available at the other terminals of the secondaries. However, when the loads become unbalanced, as would be the case if a tube was broken or there was a bad connection, then the voltage at the common point of the secondaries will be much higher than its normal value. It is simple to size resistors R35 and R36 in Figure17 such that in normal operation the OVP voltage remains below 3 volts while during abnormal operation the OVP voltage goes above 3 volts causing a system fault.

The multi-tube configuration is modular. Since each double transformer can drive two CCFLs it is possible to construct 2, 4, 6..... tube solutions using the basic architecture. Of course the FETs must be properly sized to handle the increased current. Figure19 shows a 4 tube application. In this configuration the common secondary connection (the node NOT connected to the lamp) is made with the opposite transformer. In this way the secondary current from the winding on the first transformer should be equal to the secondary current of its companion winding on the second transformer. In the case of 4 lamps driven by two transformers there are two sets of common secondary nodes. Each set drives a resistor divider (in this case R35/R36 and R38/R39) whose outputs are diode "OR'd" together at the OVP node. That way either transformer that experiences an overvoltage fault condition will be able to pull up the OVP node and cause the system to shut down.

The concept can be expanded for more than four tubes. For every 2 extra tubes that need to be added the user must add one more transformer, a resistor divider, and a small diode such as a 1N914.

Figure 16 shows a complete multi-tube architecture schematic. Analogous components have been given the same numbers as in the single tube schematic. There is really very little difference between the the single tube configuration and the multi-tube version. Transistors Q4 and Q5 are added to buffer the high side drive OUTA. This may be necessary because the PMOS devices for larger current applications have larger gate drive requirements. Capacitor C30 is added to the OVP node so that unwanted high frequency signals do not couple to the OVP node and cause an undesired shutdown.

The MOS transistors are sized bigger for the 4 tube application as would be expected. The peak currents are much higher so the Vbatt bypassing capacitor must be increased as well. The schematic shows C5 as a 100uF capacitor but higher values such as 220uF are not uncommon in order to minimize ripple on Vbatt.

Figure 16. Four Tube Application Schematic

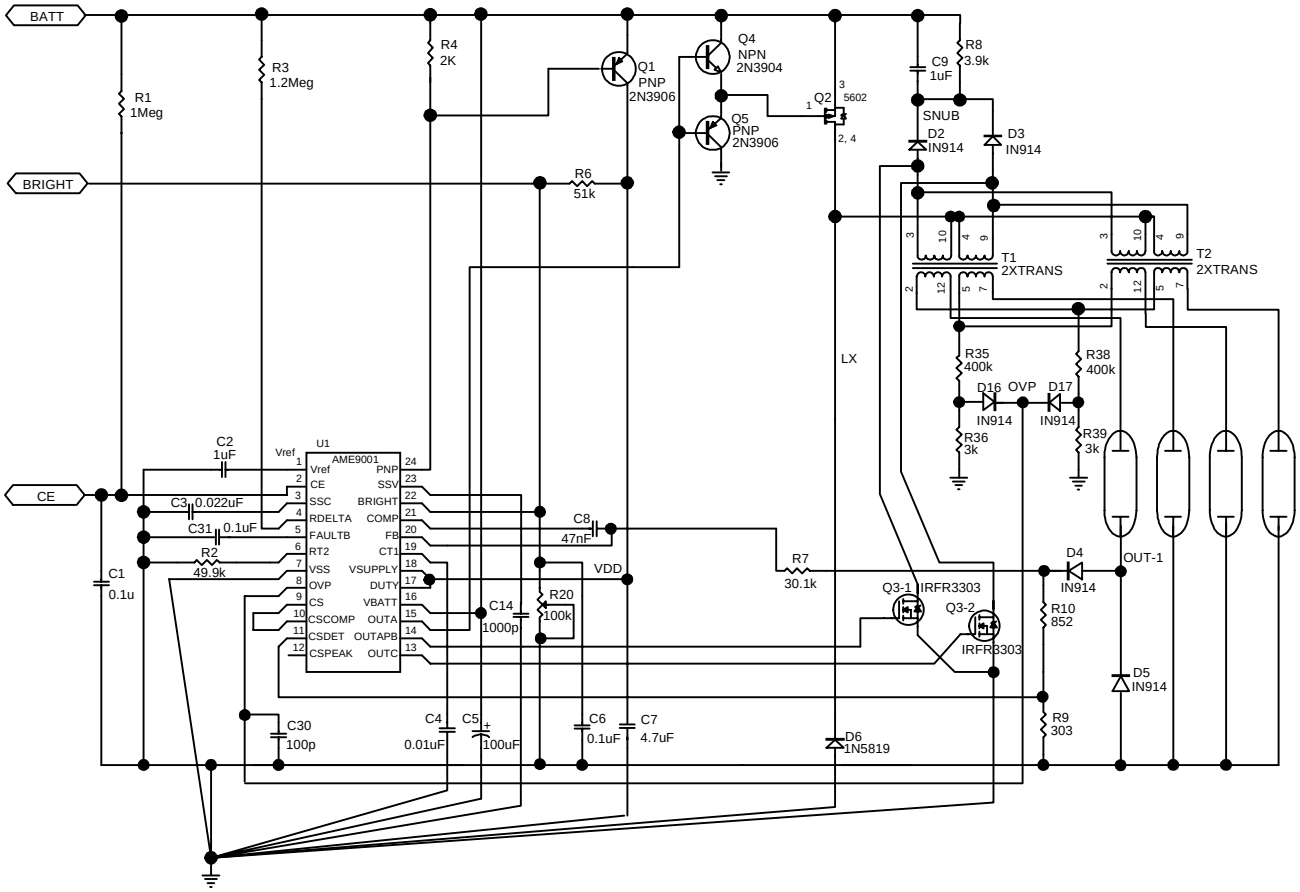


Figure 17. Double CCFL Power Section

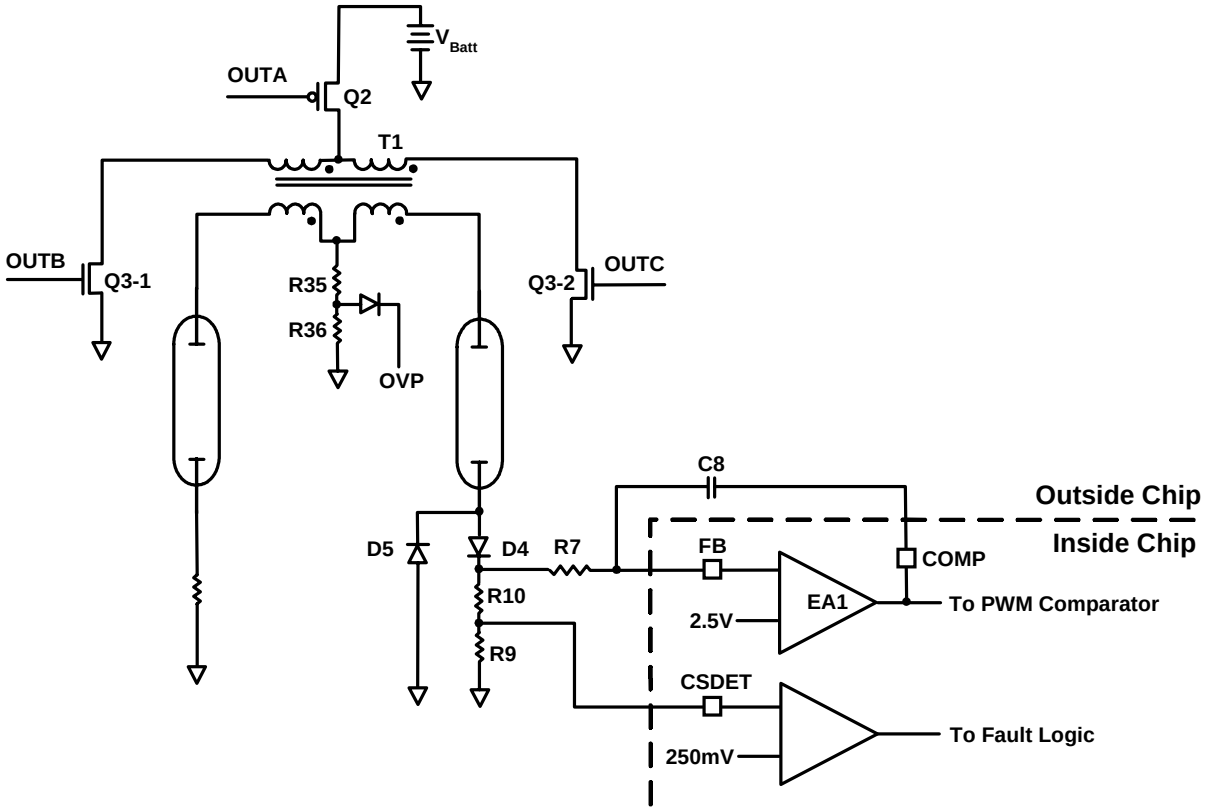


Figure 18. Double transformer construction detail

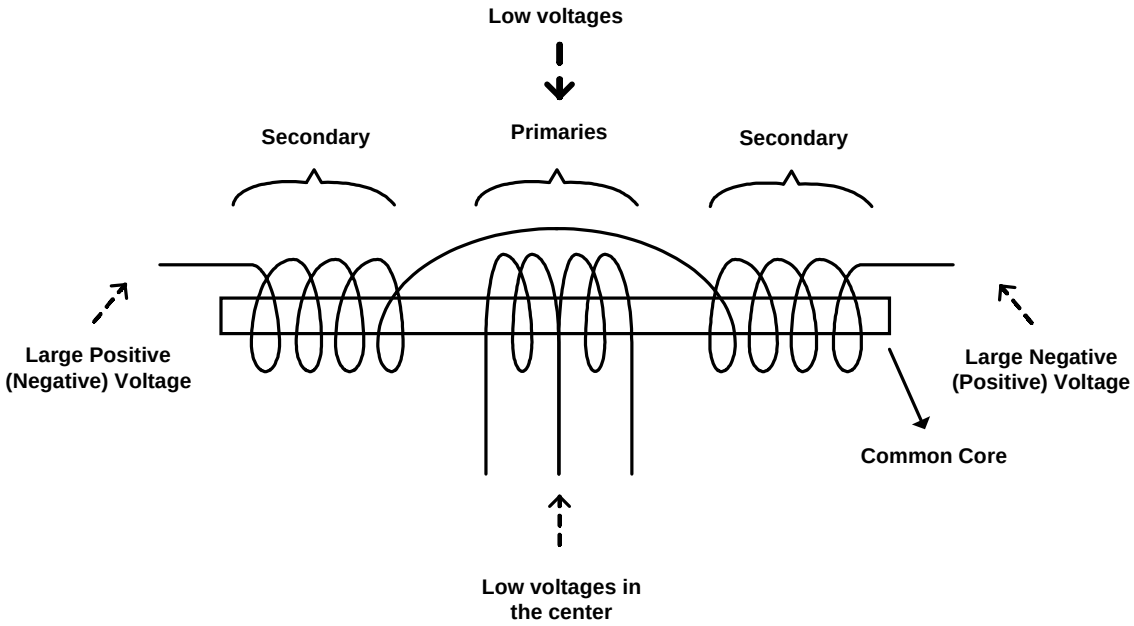
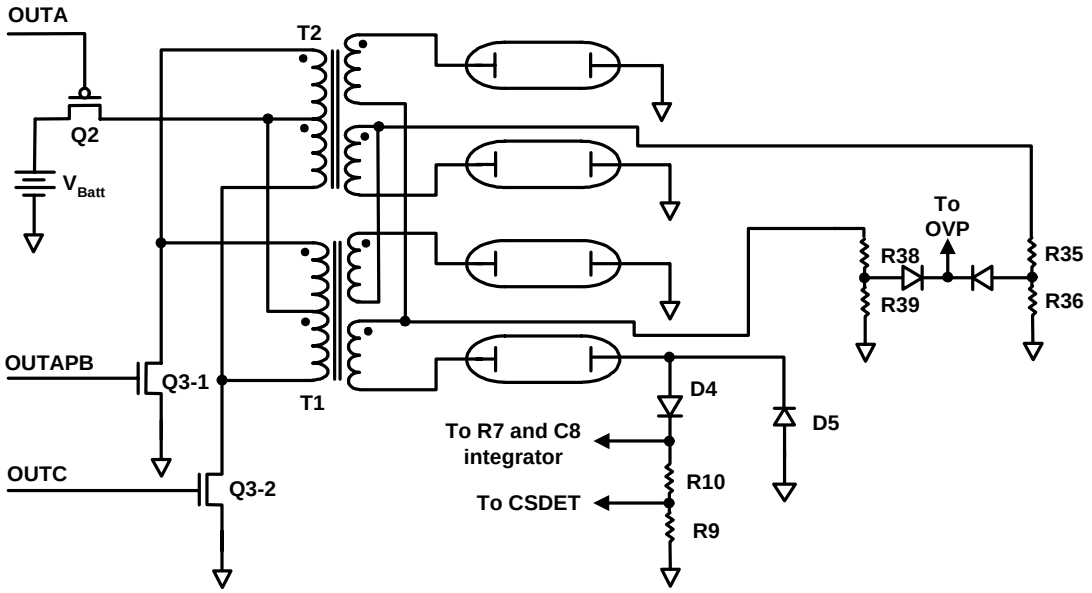
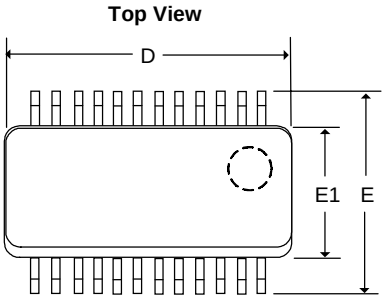


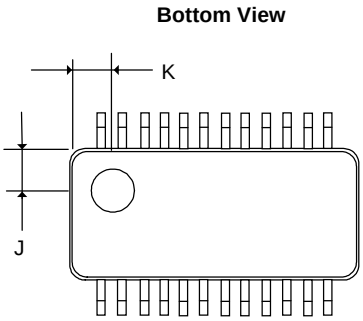
Figure 19. Four Tube Power Section

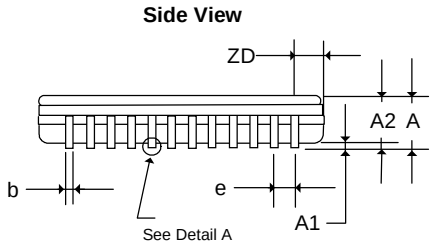


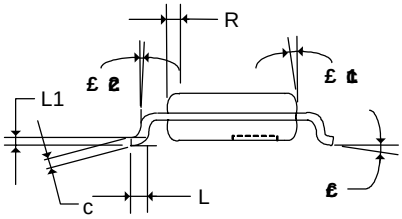
■ Package Dimension

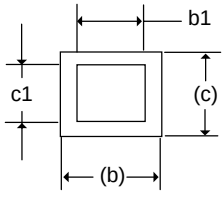
QSOP24











SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.524	1.752	0.060	0.069
A1	0.101	0.228	0.004	0.009
A2	1.473REF		0.058REF	
b	0.203	0.304	0.008	0.012
b1	0.203	0.279	0.008	0.011
c	0.177	0.254	0.007	0.010
c1	0.177	0.228	0.007	0.009
D	8.559	8.737	0.337	0.344
ZD	0.838REF		0.033REF	
E	5.791	6.197	0.228	0.244
E1	3.810	3.987	0.150	0.157
L	0.406	1.270	0.016	0.050
L1	0.254BSC		0.010BSC	
e	0.635BSC		0.025BSC	
J	1.27REF		0.050REF	
K	1.27REF		0.050REF	
θ	0^o	8^o	0^o	8^o
θ1	5^o	15^o	5^o	15^o
θ2	0^o	-	0^o	-
R	0.33 x 45^o		0.013 x 45^o	

Life Support Policy:

These products of AME, Inc. are not authorized for use as critical components in life-support devices or systems, without the express written approval of the president of AME, Inc.

AME, Inc. reserves the right to make changes in the circuitry and specifications of its devices and advises its customers to obtain the latest version of relevant information.

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