



No. 1824A

DM4020

**LIQUID CRYSTAL
DOT MATRIX DISPLAY MODULE**
40 characters x 2 lines

General Description

The DM4020 is a liquid crystal dot matrix display module that consists of LCD panel (LCD-5421), LCD control driver HD44780, driver LC7930 and is capable of providing 40 characters x 2 lines display. It contains a controller, a data RAM, and a character generator ROM required for providing display. Data interfacing is in 8-bit parallel or 4-bit parallel and data can be written in or read from a microprocessor.

General Specifications

- | | |
|--------------------------------|---|
| 1. Display system | 1/5bias 1/16duty |
| 2. Display content | 40 characters x 2 lines |
| 3. Dots organizing 1 character | 5 x 7 dots/character + cursor |
| 4. Display data RAM | 80 x 8 bits |
| 5. Character generator ROM | 160-character JIS font set + 32-character special font set
Refer to Table 1. |
| 6. Character generator RAM | 64 x 8 bits 5 x 7 dots 8 characters |
| 7. Instruction function | Refer to Table 2. |
| 8. Circuit diagram | Refer to Fig. 3. |

Outline

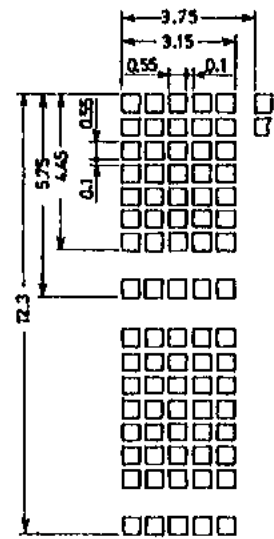
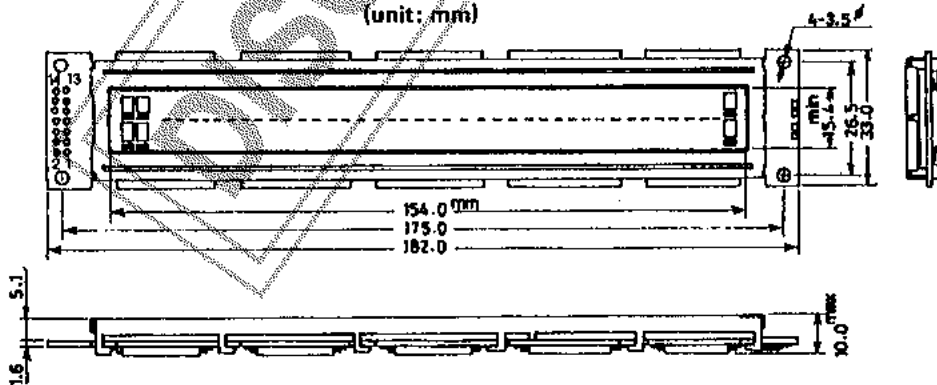
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|-------------------|---------------------------------|
| 1. Module outline | 33.0(W) x 182.0(L) x 10(T) (mm) |
| 2. View area | 154.0 x 15.4 (mm) |
| 3. Dot size | 0.55 x 0.55 (mm) |
| 4. Dot pitch | 0.85 x 0.65 (mm) |
| 5. Character size | 3.15 x 4.45 (mm) |

Absolute Maximum Ratings/T_a=25°C

		unit
Supply Voltage	V _{DD} -V _{SS}	-0.3 to +7 V
Input Voltage	V _I	-0.3 to V _{DD} +0.3 V
Drive Voltage	V _{DD} -V _O	-0.3 to +13.5 V
Operating Temperature	T _{opg}	0 to 50 °C
Storage Temperature	T _{stg}	-20 to 60 °C

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Case Outline 5005
(unit: mm)



Display pattern

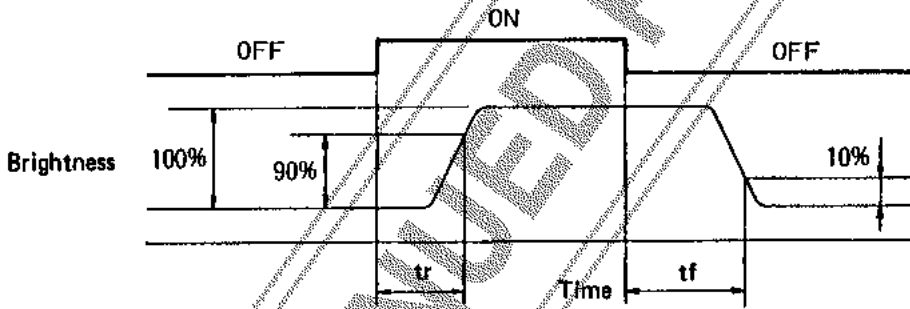
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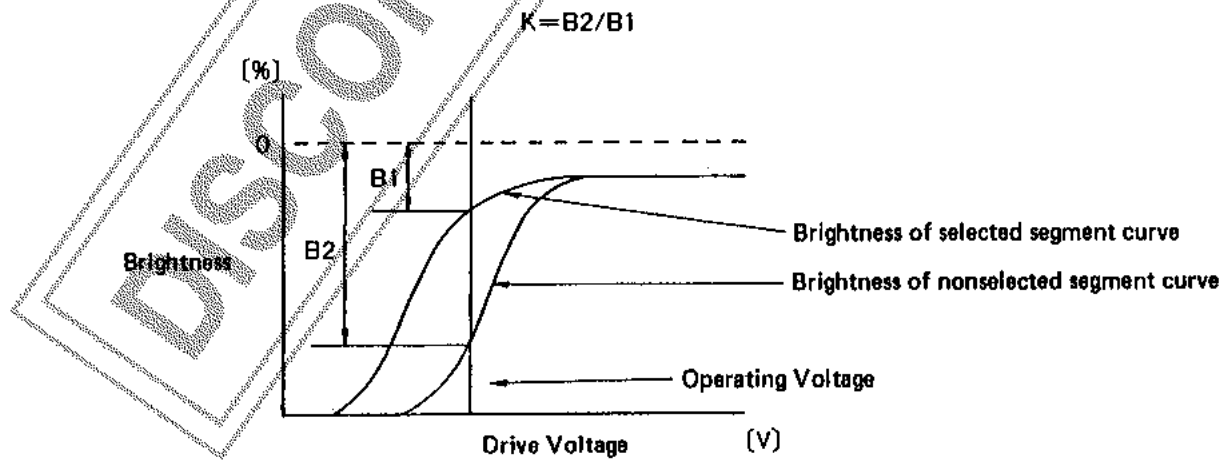
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Electro-optical Characteristics/ $V_{DD}=5.0V$, $T_B=25^\circ C$ unless otherwise specified				min	typ	max	unit
Input "High" Voltage	V_{IH}			2.2		5.0	V
Input "Low" Voltage	V_{IL}			0		0.5	V
Output "High" Voltage	V_{OH1}	DB0 to DB7, $-I_{OH}=0.2mA$		2.4			V
	V_{OH2}	Other than DB0 to DB7, $I_{OH}=40\mu A$		$0.9V_{DD}$			V
Output "Low" Voltage	V_{OL1}	DB0 to DB7, $-I_{OL}=1.2mA$				0.4	V
	V_{OL2}	Other than DB0 to DB7, $I_{OL}=40\mu A$				$0.1V_{DD}$	V
Input/Output Leakage Current	I_{IL}	$V_{in}=0$ to V_{DD}				1.0	μA
Input Current	I_p	Pull-up MOS $V_{DD}=5V$		50	125	250	μA
Current Dissipation	I_{DD}	No input/output current included			(1.2)	2.5	mA
Oscillation Frequency	F_{OSC}			190	270	350	kHz
Viewing Angle	$\phi_2 - \phi_1$	$K=1.4$ $\theta=0^\circ$		20			degree
Contrast Ratio	K	$\phi=20^\circ$ $\theta=0^\circ$		3.0			
Rise Time	t_r	$\phi=20^\circ$ $\theta=0^\circ$			150	250	mS
Fall Time	t_f	$\phi=20^\circ$ $\theta=0^\circ$			150	250	mS
LCD Drive Voltage (Recommend Value) 1/16 duty	$V_{DD}-V_0$	$T_B=0^\circ C$ $\phi=20^\circ$, $\theta=0^\circ$, $K \geq 3$		4.2	4.3	4.4	V
	$V_{DD}-V_0$	$T_B=25^\circ C$ " " " "		3.8	3.9	4.0	V
	$V_{DD}-V_0$	$T_B=50^\circ C$ " " " "		3.4	3.5	3.6	V

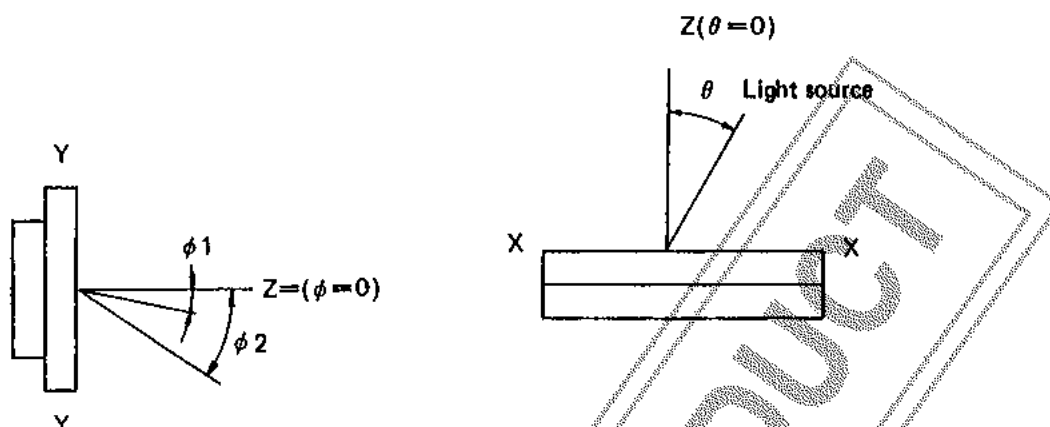
(1) Test Condition for Response Time (t_r , t_f)



(2) Definition of Contrast (K)



(3) Contrast Ratio Measuring Method



Angles ϕ and θ are defined shown above.

The light source is placed in the θ direction at an angle of 30° and the sensor is placed in the ϕ direction to measure the contrast.

Pin Description

No.	Pin Name	Function
1	VSS	(-) power supply pin 0V
2	VDD	(+) power supply pin +5V
3	VO	Pin for applying LCD drive voltage
4	RS	Input pin HI=Data LOW=Instruction
5	R/W	Input pin HI=Read LOW=Write
6	E	Input pin Enable signal
7	DB0	Data bus line
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	

Note 1. The LCD drive voltage can be varied from 3V to 5V by a variable resistor of 5kohm connected across VSS and VO.

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Timing Characteristics

		min	typ	max	unit
Enable Cycle Time	t_{cycE}	1000			ns
Enable Pulse Width High level	P_{WEH}	450			ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}			25	ns
Set up Time RS/RW-E	t_{As}	140			ns
Address Hold Time	t_{AH}	10			ns
Data Delay Time	t_{DDR}			320	ns
Data Set up Time	t_{DSW}	195			ns
Data Hold Time	$t_H(t_{DHR})$	10(20)			ns

Figs. 1, 2

Writes Operation

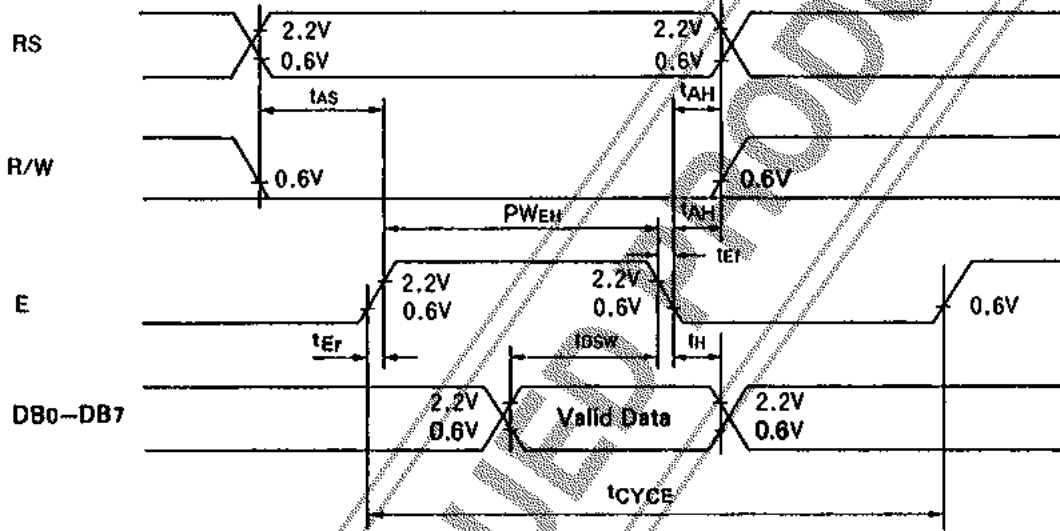


Fig. 1 Interface Timing (Data Write)

Read Operation

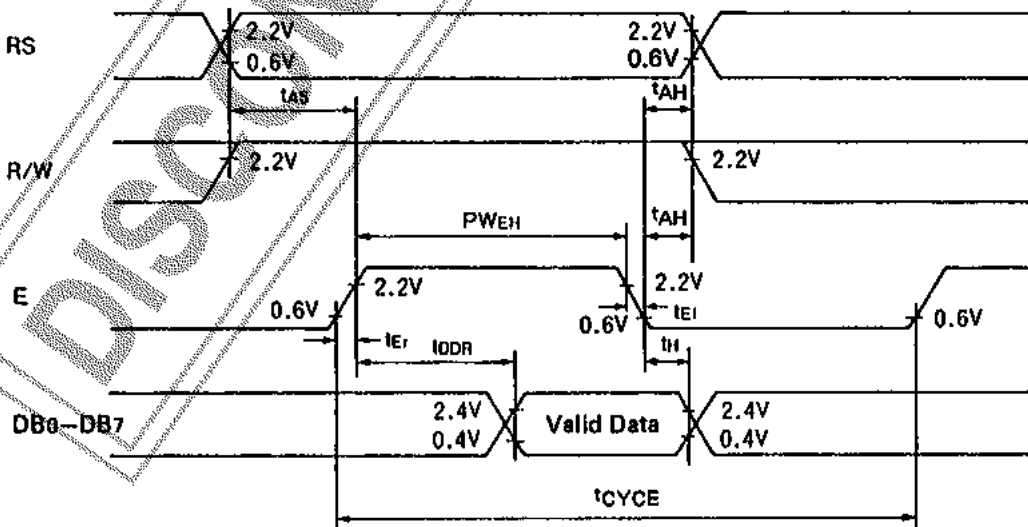


Fig. 2 Interface Timing (Data Read)

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Table 1 Character code

Low-order 4 bits \ HI-order 4 bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	1	2	3	4	5	6	7	8	9	0
xxxx0001	(2)	!	1	2	3	4	5	6	7	8	9	0	1
xxxx0010	(3)	"	2	3	4	5	6	7	8	9	0	1	2
xxxx0011	(4)	#	3	4	5	6	7	8	9	0	1	2	3
xxxx0100	(5)	*	4	5	6	7	8	9	0	1	2	3	4
xxxx0101	(6)	%	5	6	7	8	9	0	1	2	3	4	5
xxxx0110	(7)	&	6	7	8	9	0	1	2	3	4	5	6
xxxx0111	(8)	'	7	8	9	0	1	2	3	4	5	6	7
xxxx1000	(1)	(8	9	0	1	2	3	4	5	6	7	8
xxxx1001	(2))	9	0	1	2	3	4	5	6	7	8	9
xxxx1010	(3)	*	0	1	2	3	4	5	6	7	8	9	0
xxxx1011	(4)	+	1	2	3	4	5	6	7	8	9	0	1
xxxx1100	(5)	=	2	3	4	5	6	7	8	9	0	1	2
xxxx1101	(6)	-	3	4	5	6	7	8	9	0	1	2	3
xxxx1110	(7)	.	4	5	6	7	8	9	0	1	2	3	4
xxxx1111	(8)	/	5	6	7	8	9	0	1	2	3	4	5

(Note) The CG RAM is a character generator RAM used to store the character patterns that can be program-rewritten, as desired, by the user.

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Table 2 Instruction function

Instruction	Code										Contents	Execution Time (f _{OSC} =250kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (address 0).	82μs ~ 1.64ms
Cursor home	0	0	0	0	0	0	0	0	0	1 *	Returns the cursor to the home position (address 0). Also returns the display being shifted to the original position. The DD RAM contents remain unaffected.	40μs ~ 1.6ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies whether to or not to shift the display. These operations are performed during data write and read.	40μs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets all display ON/OFF(D), cursor ON/OFF(C), cursor position character blink (B).	40μs
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without affecting the DD RAM contents.	40μs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets the interface data length (DL), number of display lines (L), and character font (F).	40μs
CG RAM address set	0	0	0	1	A _{CG}					Sets the CG RAM address. RAM data is sent/received after this setting.		40μs
DD RAM address set	0	0	1	A _{DD}					Sets the DD RAM address. DD RAM data is sent/received after this setting.		40μs	
Busy flag/address read	0	1	BF	AC					Reads the contents of busy flag (BF) indicating internal operation is in progress and reads the contents of address counter.		1μs	
CG RAM/DD RAM data write	1	0	Write Data					Writes data into the DD RAM or CG RAM.		40μs		
CG RAM/DD RAM data read	1	1	Read Data					Reads data from the DD RAM or CG RAM.		40μs		
	I/D = 1 : Increment (+1) I/D = 0 : Decrement (-) S = 1 : Accompanied by display shift S/C = 1 : Display shift S/C = 0 : Cursor move R/L = 1 : Right shift R/L = 0 : Left shift DL = 1 : 8 bits DL = 0 : 4 bits N = 1 : 2 lines N = 0 : 1 line F = 1 : 5 x 10 dots F = 0 : 5 x 7 dots BF = 1 : Internally operating BF = 0 : Possible to accept instruction										DD RAM : Display data RAM CG RAM : Character generator RAM A _{CG} : CG RAM address A _{DD} : DD RAM address Corresponds to cursor address. AC : Address counter used for both DD RAM and CG RAM.	The change in the frequency (f _{OSC}) also causes the execution time to be changed. (Example) When f _{OSC} =270kHz, 40μs x 250/270 = 37μs.

Fig. 3 Circuit Diagram DM4020

