Digital Video Camera Chip Set
Product Brief

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HITACHI

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Section 1 Introduction

Video cameras are becoming more compact and producing better image quality. Hitachi's Digital Video Camera Chip Set is a new product aimed at the developing market for video cameras. It converts analog video camera signals to digital signals. This product brief introduces the integrated circuits and applications code which make up the Digital Video Camera Chip Set.

1.1 Description

The basic chipset includes a correlated double sampling/auto gain control (CDS/AGC) IC, a timing generator (TG) IC, an analog to digital converter (ADC), a digital signal processor (DSP), and an H8/337 microcontroller. If analog output (typically composite or S-Video) is needed, a digital to analog converter (DAC) can be added to the chipset. If electronic zoom and pan is desired, an electronic zoom (EZ) IC can be added to the chipset.

The CDS/AGC conditions the analog signal from a CCD image sensor and passes the conditioned output to the ADC. The analog signal is converted to a digital signal by the ADC, and the resulting digital signal is input to the DSP, which allows electronic manipulation of the image quality controls. The signal conditioning in the CDS/AGC and the electronic manipulation of the image in the DSP are controlled by the H8/337 microcontroller, which communicates with the CDS/AGC and the DSP via a serial interface.

Figure 1.1 depicts the system block diagram of a camera designed with Hitachi's Digital Video Camera Chip Set.

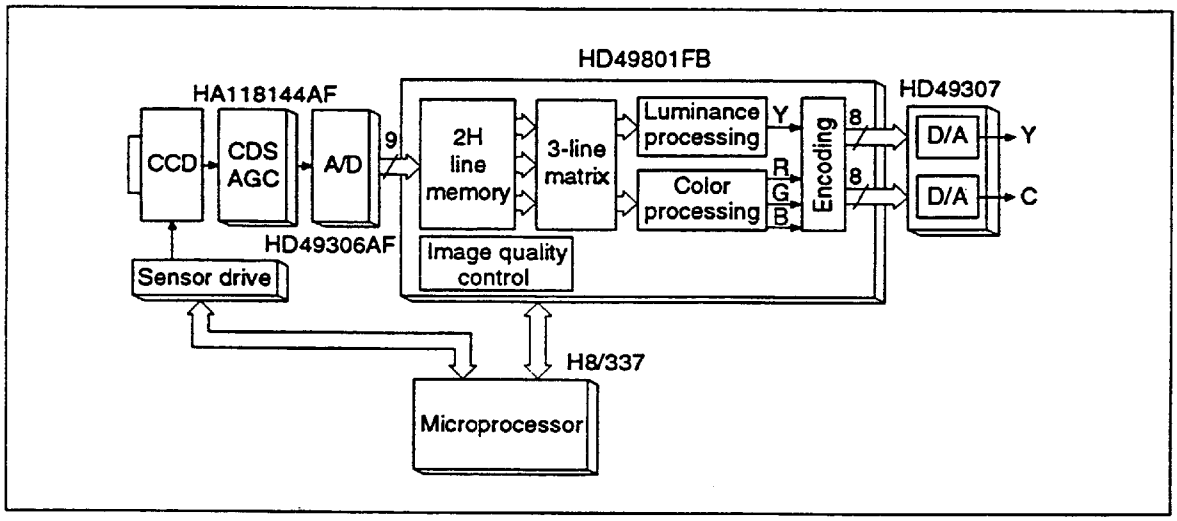


Figure 1.1 System Block Diagram of a Camera Designed with the Digital Video Camera Chip Set

The applications code which manipulates the image quality controls including color clipping level, gamma compensation, and color gain, and controls the white balance detection circuit and iris data collection circuit in the HD49801FB, is written in H8 assembly code. Table 1 shows the standard software features of the digital camera.

Table 1.1 Standard Software Features

Item	Feature
Auto iris control (AE)	The AE function distinguishes back light from front light using DSP iris data and controls the iris according to the scene being photographed.
AGC-related controls	By controlling the chroma gain and enhancer level according to the AGC gain, this function reduces S/N deterioration at low luminances.
Auto white balance (AWB)	Infers the color temperature from the white balance data of the DSP and alters the intake range of the white center and white balance according to the color temperature. This provides appropriate color reproducibility corresponding to environmental changes.
Auto setup	By automatically setting up as soon as the camera power supply is turned on (Y, R, G, and B setup adjustment), auto setup creates a black level that is not affected by temperature drift and aging.
Adjustment software	Adjustment software allows changes to the state data of the DSP (via up/down keys of a personal computer) to personal specifications.
Display functions	Provides AGC gain, color temperature, electronic shutter speed, and other display functions. These functions are useful for evaluating image quality.

Table 1.2 shows the ROM and RAM capacities of the standard software (MV-SF1A).

Table 1.2 MV-SF1A ROM and RAM Capacities

Item	Application	Module Size	Total Size
ROM	OS (μITRON)	1.96 kbyte	12.8 kbyte
	State data transfer	4.3 kbyte (including auto setup EPROM read)	
	Mode management	0.55 kbyte	
	Fade	0.25 kbyte	
	Adjustment	0.85 kbyte	
	Electronic shutter	0.062 kbyte	
	AE	2.26 kbyte	
	AWB	1.2 kbyte	
	Display	0.83 kbyte	
	Interrupt	0.52 kbyte	
RAM	OS (μITRON)	360 byte	746 byte
	Applications	386 byte	

Section 2 Integrated Circuits

2.1 HA118144AF Video Camera CDS/AGC

2.1.1 Description

The HA118144AF is a bipolar IC that was developed to perform the analog signal processing between the CCD and the ADC in a CCD camera, and is optimal for use in CCD camera digital signal processing systems.

2.1.2 Function

- Correlated double sampling
- AGC
- Sample and hold
- Gain select
- Knee processing
- Serial interface control

2.1.3 Features

- A high S/N ratio by using dual (pre- and post-) AGC amplifiers and high sensitivity based on increased coverage.
- Provides compensation for IC variations and imaging device sensitivity variations with an 8 state gain select circuit.
- Allows the AGC and gain select to be controlled from the system microprocessor over a serial interface.

2.1.4 Pin Arrangement

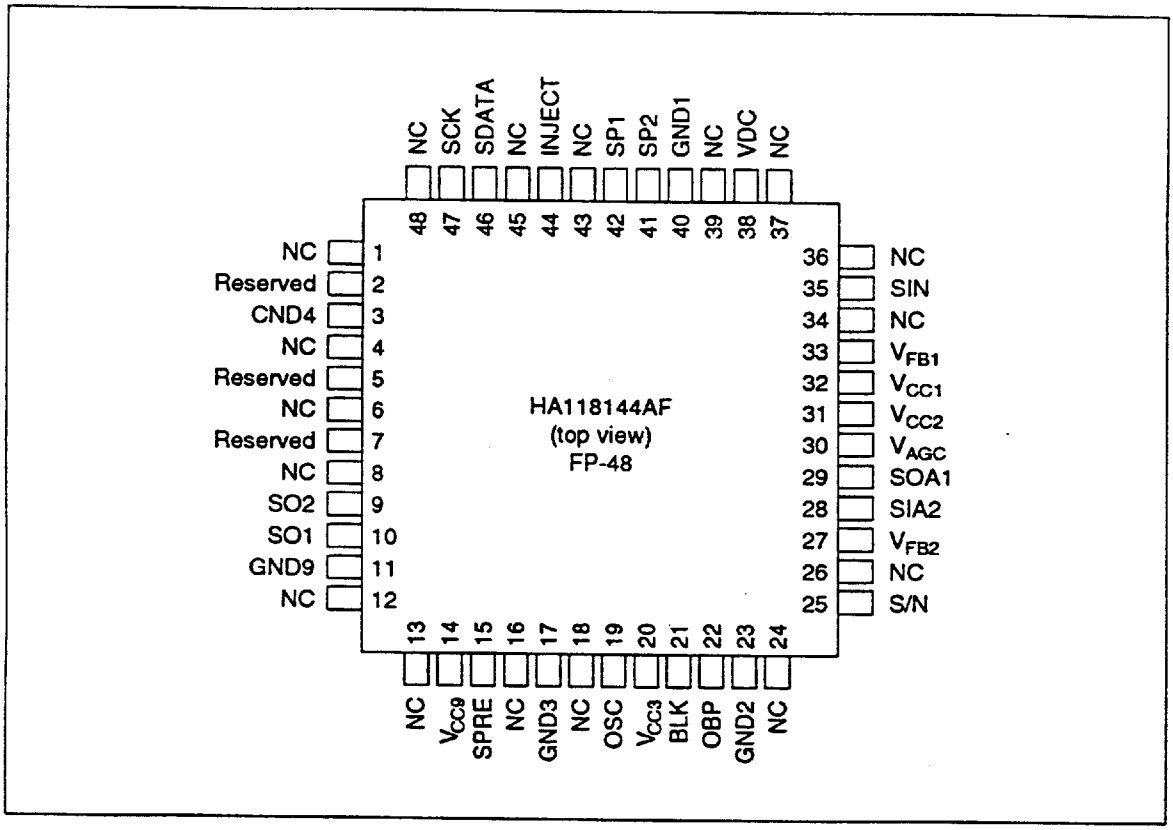


Figure 2.1 HA118144AF Pin Arrangement

2.1.5 Block Diagram

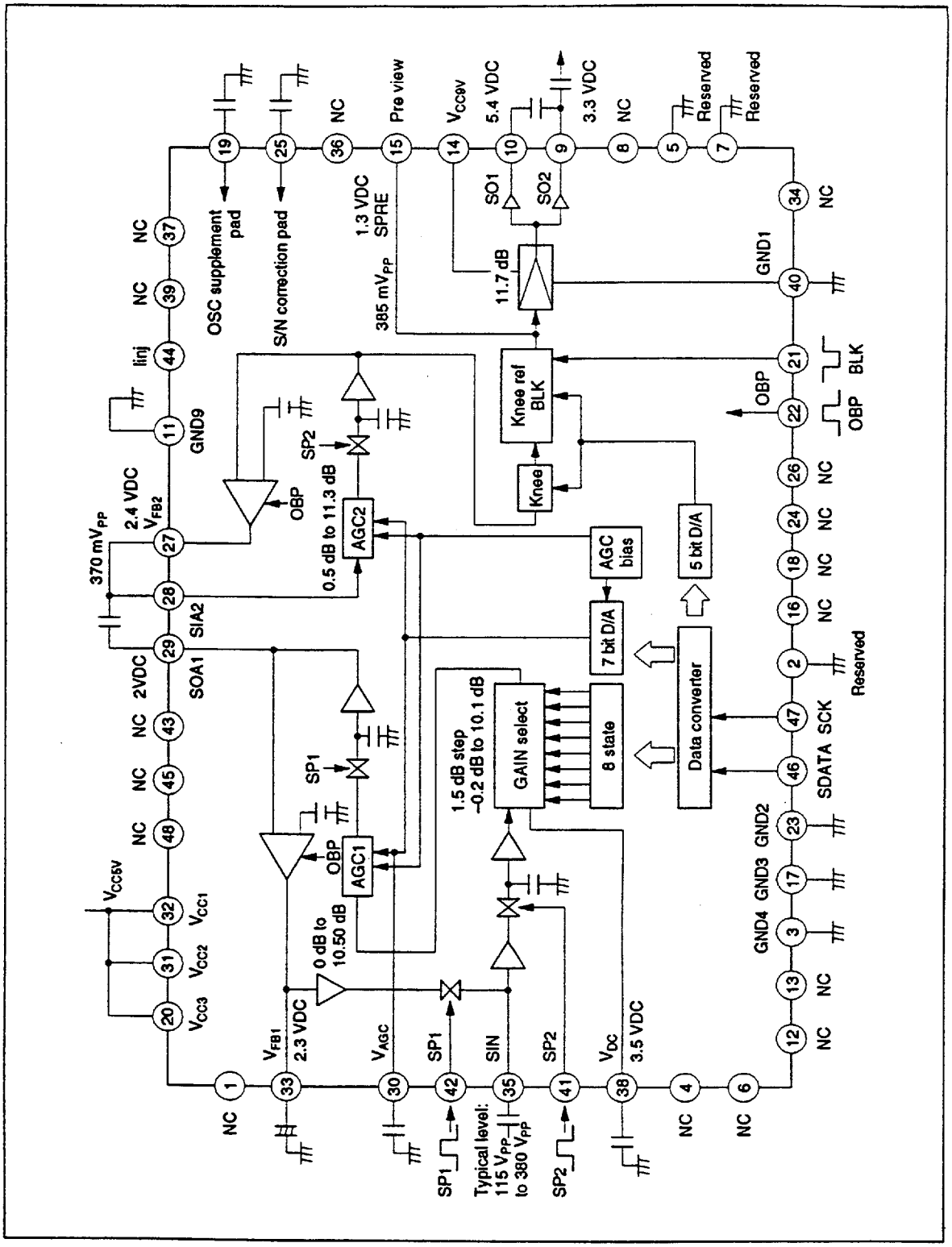


Figure 2.2 HA118144AF Block Diagram

2.2 HD49306AF CMOS 9-Bit A/D Converter

2.2.1 Description

The HD49306AF is a high-speed, low-power monolithic CMOS 9-bit A/D converter LSI.

2.2.2 Features

- Resolution: 9 bits (with overflow)
- Single +5.0 V power supply
- Output codes: binary/gray, selectable
- Digital output: 3-state TTL/ CMOS compatible
- Sleep mode provided (low-power waiting mode)

2.2.3 Pin Arrangement

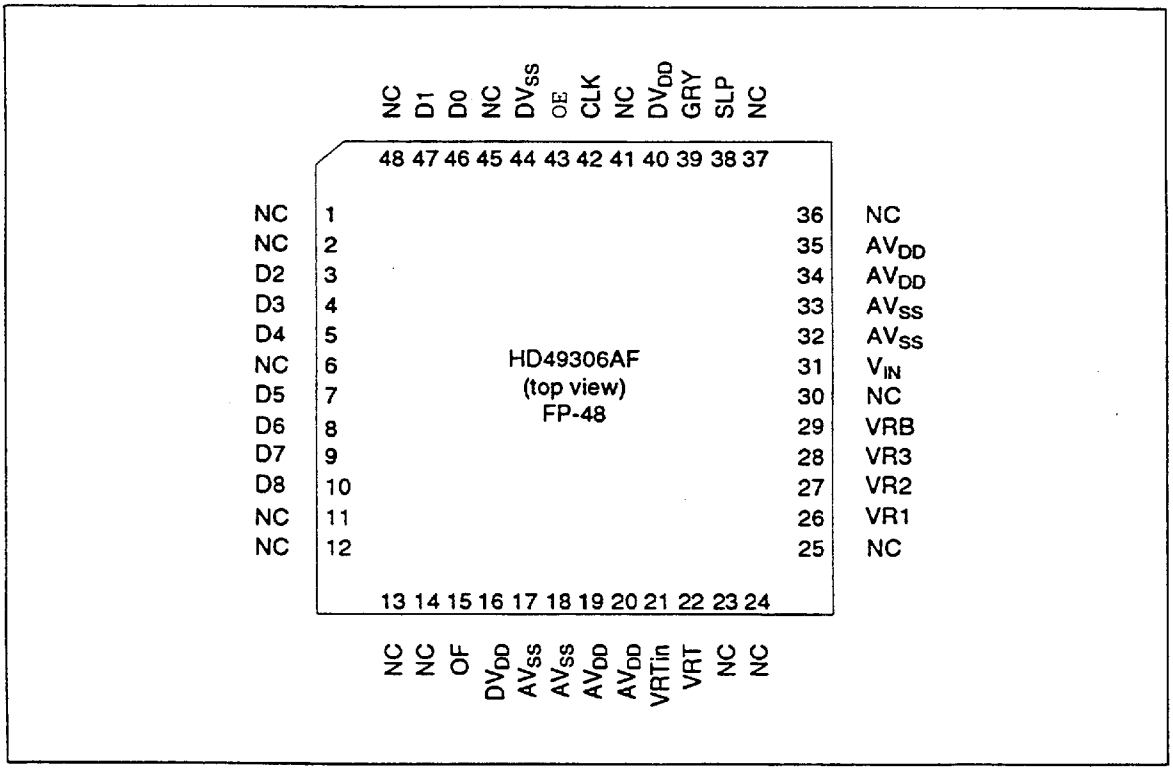


Figure 2.3 HD49306AF Pin Arrangement

2.2.5 Block Diagram

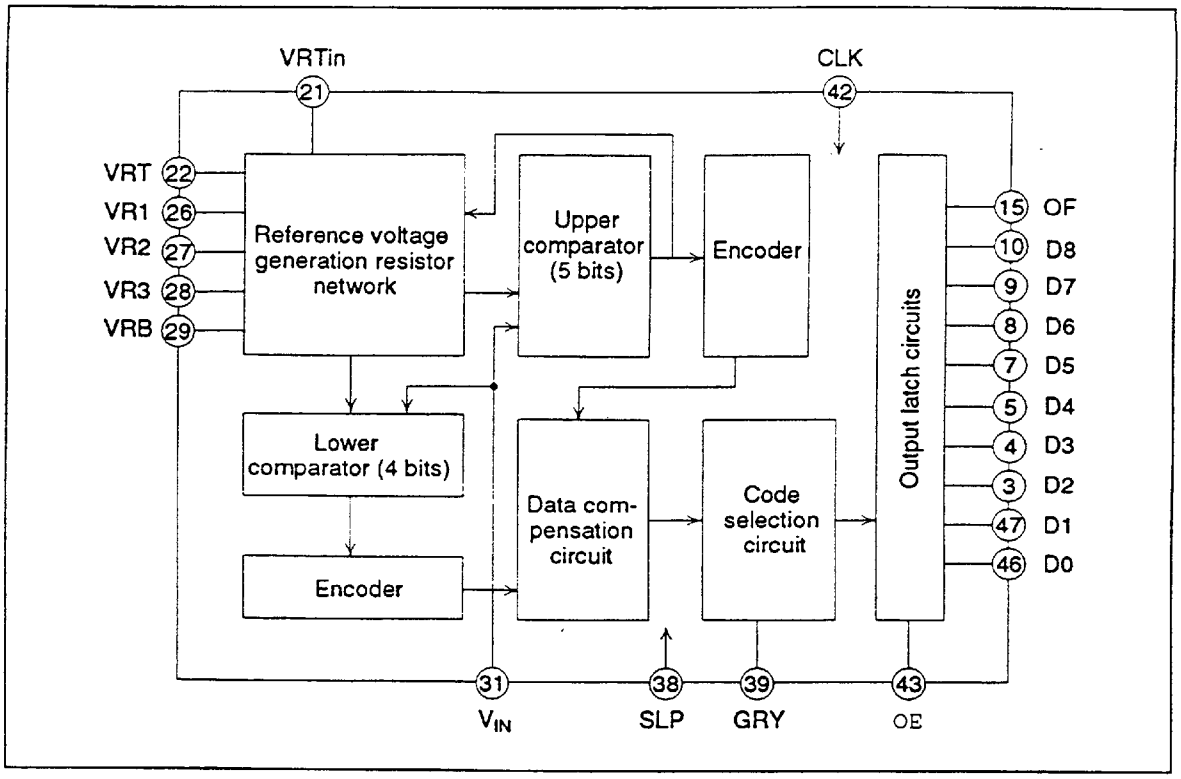


Figure 2.4 HD49306AF Block Diagram

2.3 HD49801FB Digital Signal Processor for CCD Video Cameras

2.3.1 Description

The HD49801FB is an IC that integrates all the functions required for CCD camera signal processing (except the CDS and AGC blocks) in a single chip.

2.3.2 Features

- Generates high quality chroma and luminance signals using three-line matrix processing supported by a built-in line memory (1H × 2).
- Allows microprocessor control (over a serial interface) of all image quality controls.
- Handles all formats; NTSC, PAL, SECAM (however, does not include a SECAM encoder).
- Handles 510H/768H CCD image sensors.

2.3.3 Pin Arrangement

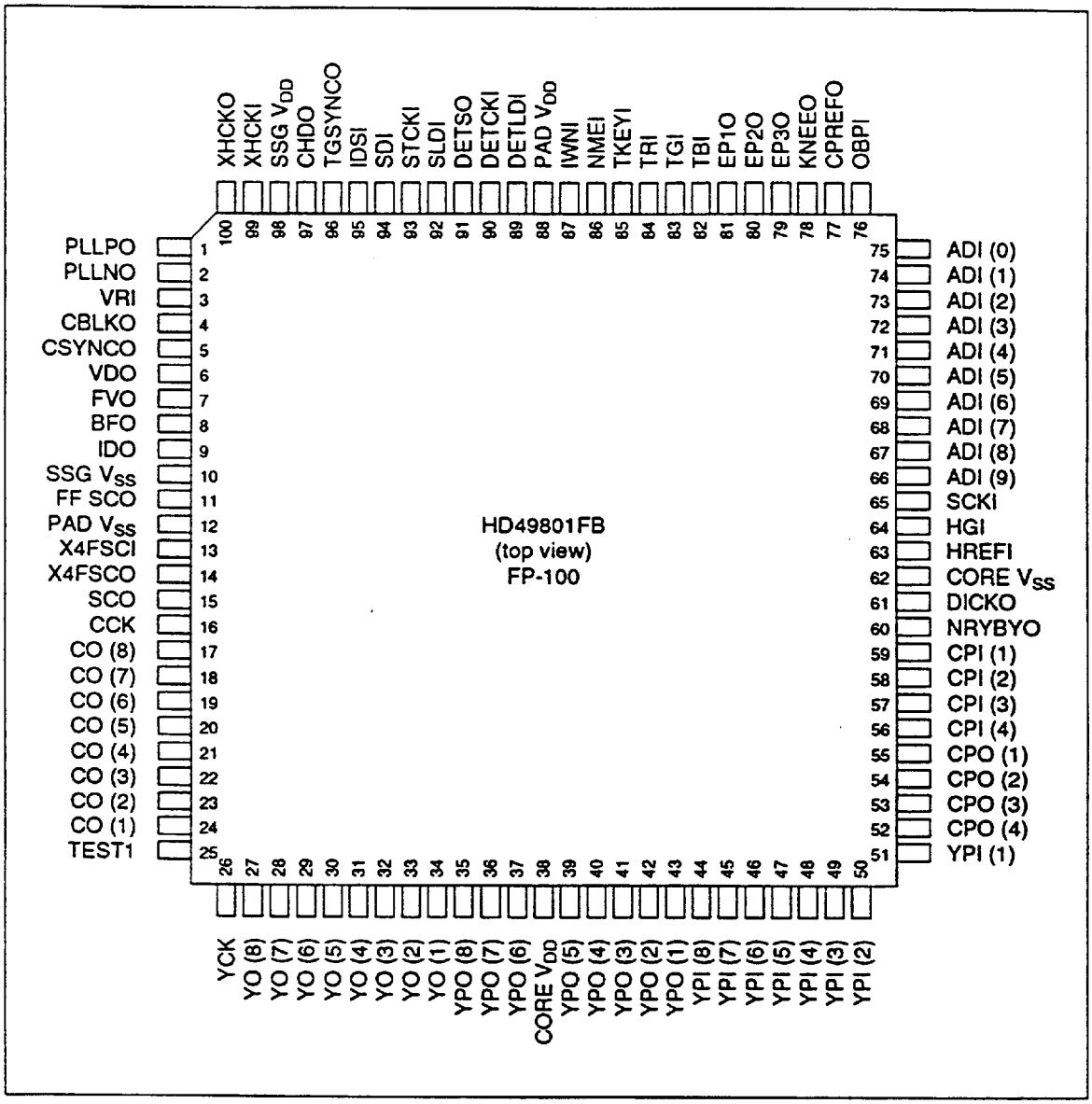
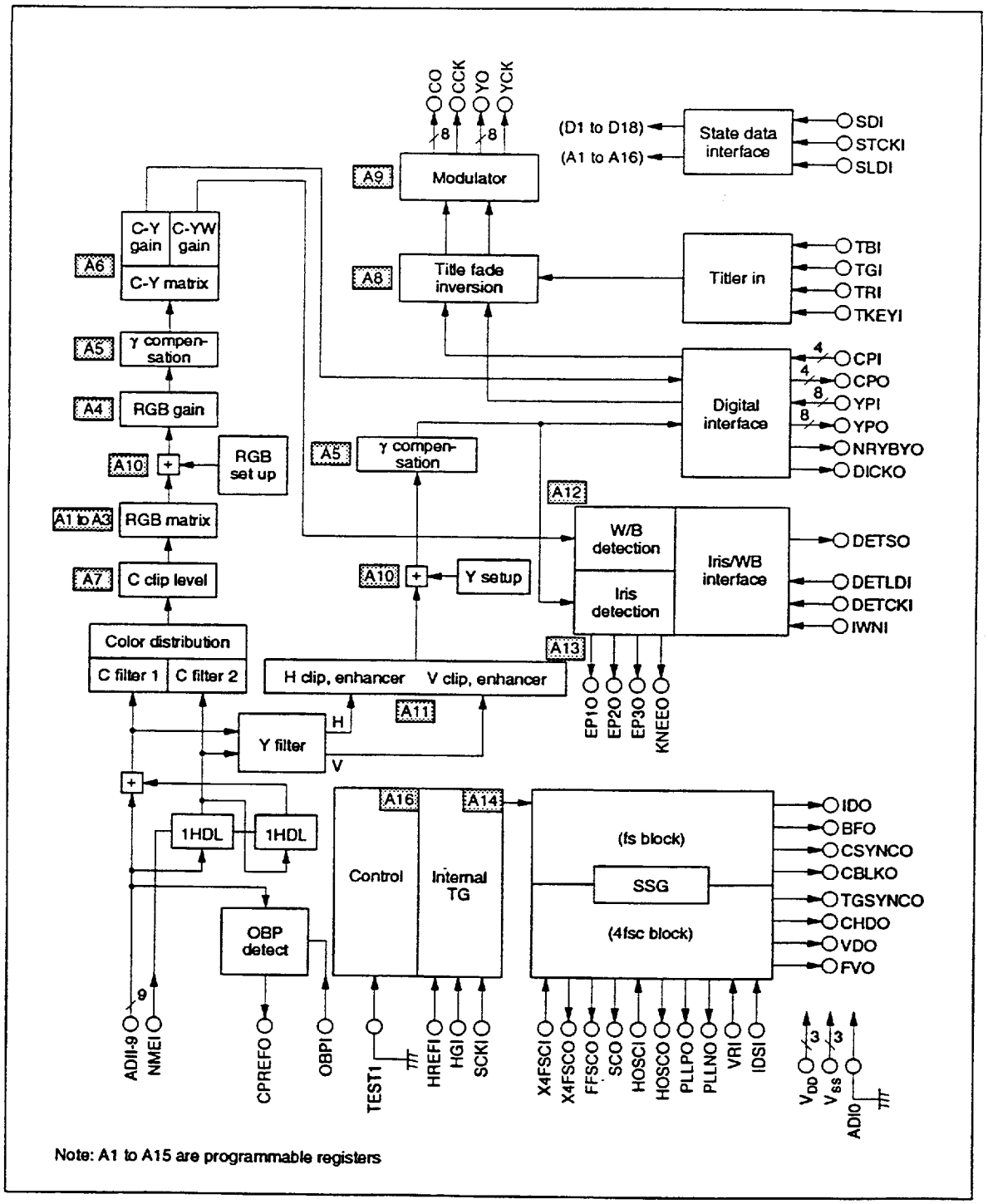


Figure 2.5 HD49801FB Pin Arrangement

2.3.4 Block Diagram



Note: A1 to A15 are programmable registers

Figure 2.6 HD49801FB Block Diagram

2.4 HD49307 Three Channel 8-Bit D/A Converter

2.4.1 Description

The HD49307 is a high-speed, low-power 8-bit D/A converter monolithic CMOS LSI which has three channels of clock and RGB data inputs. It is appropriate for applications which require three channel systems, such as digital TV and graphical displays.

2.4.2 Features

- Resolution: 8 bits
- Linearity error: ±0.2%
- Current output type: 13.3 mA × 3 channels
- Maximum conversion rate: 30 MHz (min)
- Analog output voltage range: V_{DD} to V_{DD} – 1 V
- Digital input voltage: TTL and CMOS level
- Power supply voltage: +5.0 V
- Power consumption: 300 mW (typ)

2.4.3 Pin Arrangement

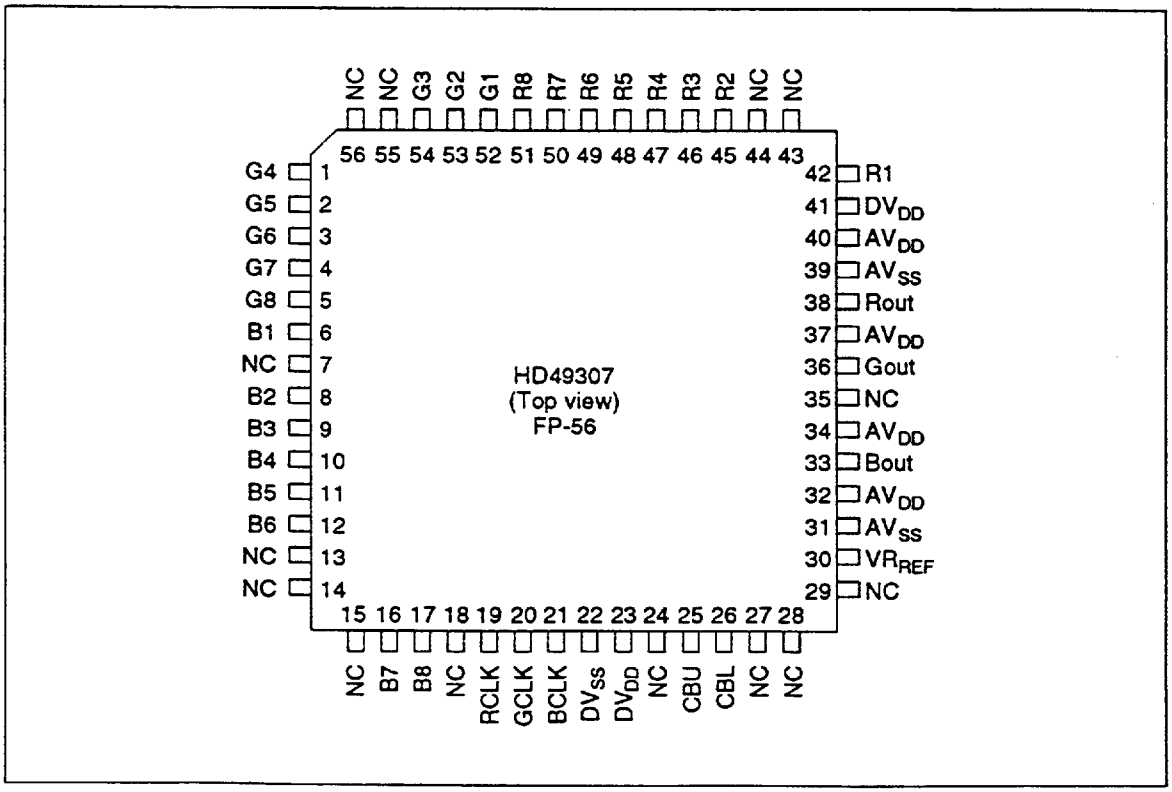


Figure 2.7 HD49307 Pin Arrangement

2.4.4 Block Diagram

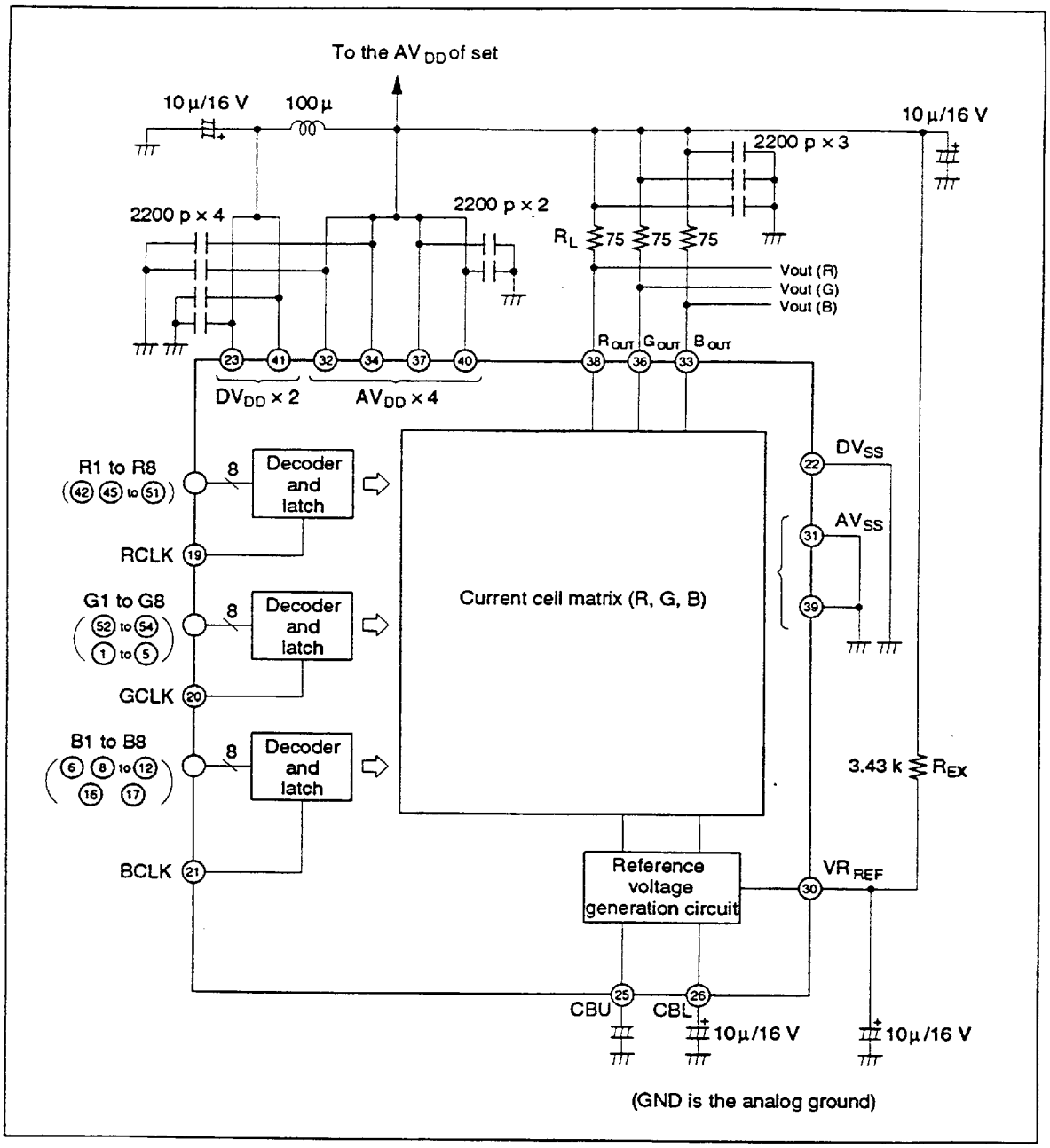


Figure 2.8 HD49307 Block Diagram