HD64540

LAPB Controller

Description

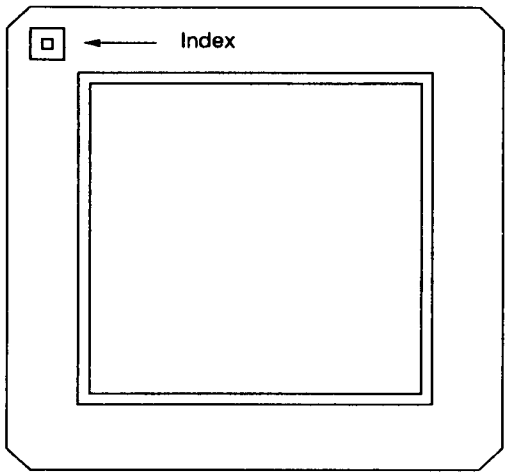
The HD64540 one-chip CMOS communications device supports the LAPB protocols described by CCITT recommendation X.25. Because of its asynchronous bus interface, the HD64540 can be used with 16-bit external microprocessors.

Features

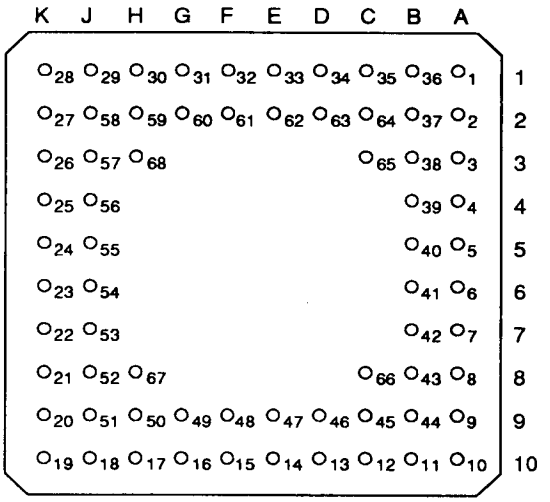
- CCITT recommendation X.25 procedure support
  - — Processes X.25 layer 2 protocols (LAPB single link)
  - — Reduces main processor load, improving system throughput
- Protocol processing operations
  - — HDLC framing, zero insertion/deletion, flag control, retransmission control, and state transition control
- Statistical counters
  - — Includes seventeen counters for statistical information: counters for specific frame types transmitted or received, transmission errors, etc.
  - — Reports counter status to host processor
- Selectable mode and parameters
  - — Terminal (DTE)/network (DCE) mode/transparent mode
  - — System parameters programmable
- Chained transmit/receive function
  - — Long frames may be stored in multiple data buffers that are chained together and, except for UI, TEST, and XID frames, may be transmitted or received.
  - — Transmitted UI, TEST, and XID frame lengths are limited to a single buffer
- High throughput through unique architecture
  - — High performance protocol processing and data transmission

Pin Arrangement (ceramic pin grid array)

PGA-68 pin



(Top view)



(Bottom view)

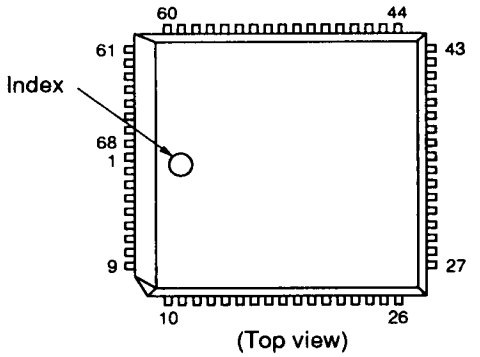
Pin Code	Pin No.	Name
A1	1	$\overline{IRQ}$
A2	2	S/$\overline{U}$
A3	3	NUM
A4	4	A_1
A5	5	V_{SS}
A6	6	ϕ
A7	7	A_4
A8	8	A_5
A9	9	A_7
A10	10	A_9/D_1
B1	36	$\overline{READY}$
B2	37	$\overline{IACK}$
B3	38	PF
B4	39	A_2
B5	40	V_{CC}
B6	41	A_3
B7	42	A_6
B8	43	A_8/D_0
B9	44	A_{11}/D_3
B10	11	A_{12}/D_4
C1	35	$\overline{HDS}$
C2	64	$\overline{AIN}$
C3	65	NC

Pin Code	Pin No.	Name
C8	66	A_{10}/D_2
C9	45	A_{13}/D_5
C10	12	A_{14}/D_6
D1	34	R/$\overline{W}$
D2	63	$\overline{LDS}$
D9	46	A_{15}/D_7
D10	13	A_{16}/D_8
E1	33	V_{SS}
E2	62	V_{CC}
E9	47	V_{SS}
E10	14	A_{17}/D_9
F1	32	$\overline{DBEN}$
F2	61	$\overline{DIN}$
F9	48	A_{19}/D_{11}
F10	15	A_{18}/D_{10}
G1	31	NC
G2	60	$\overline{AS}$
G9	49	A_{22}/D_{14}
G10	16	A_{20}/D_{12}
H1	30	$\overline{ABEN}$
H2	59	$\overline{BACK}$
H3	68	NUM
H8	67	$\overline{BRTRY}$

Pin Code	Pin No.	Name
H9	50	V_{SS}
H10	17	A_{21}/D_{13}
J1	29	$\overline{CS}$
J2	58	TXC
J3	57	V_{SS}
J4	56	V_{CC}
J5	55	PI2
J6	54	PO1
J7	53	NUM
J8	52	V_{CC}
J9	51	V_{CC}
J10	18	A_{23}/D_{15}
K1	28	$\overline{BREQ}$
K2	27	TXD
K3	26	RXD
K4	25	RXC
K5	24	PI1
K6	23	PI0
K7	22	PO0
K8	21	NUM
K9	20	$\overline{RES}$
K10	19	$\overline{BERR}$

NUM: Not Users Mode NC: No Connection

Pin Arrangement (plastic PLCC)



Pin No.	Names
1	V_{SS}
2	V_{CC}
3	R/$\overline{W}$
4	$\overline{HDS}$
5	$\overline{LDS}$
6	$\overline{READY}$
7	$\overline{AIN}$
8	$\overline{IRQ}$
9	$\overline{IACK}$
10	NC
11	S/$\overline{U}$
12	PF
13	NUM
14	A1
15	A2
16	V_{SS}
17	V_{CC}
18	ϕ
19	A3
20	A4
21	A5
22	A6
23	A7

Pin No.	Names
24	A8/D0
25	A9/D1
26	A10/D2
27	A11/D3
28	A12/D4
29	A13/D5
30	A14/D6
31	A15/D7
32	A16/D8
33	V_{SS}
34	A17/D9
35	A18/D10
36	A19/D11
37	A20/D12
38	A21/D13
39	A22/D14
40	A23/D15
41	V_{SS}
42	V_{CC}
43	V_{CC}
44	$\overline{BRTRY}$
45	$\overline{BERR}$
46	$\overline{RES}$

Pin No.	Names
47	NUM
48	NUM
49	PO0
50	PO1
51	PI0
52	PI1
53	PI2
54	RXC
55	RXD
56	V_{SS}
57	V_{CC}
58	TXD
59	TXC
60	NUM
61	$\overline{BREQ}$
62	$\overline{BACK}$
63	$\overline{CS}$
64	$\overline{AS}$
65	$\overline{ABEN}$
66	NC
67	$\overline{DIN}$
68	$\overline{DBEN}$

NUM: Not Users Mode
NC: No Connection

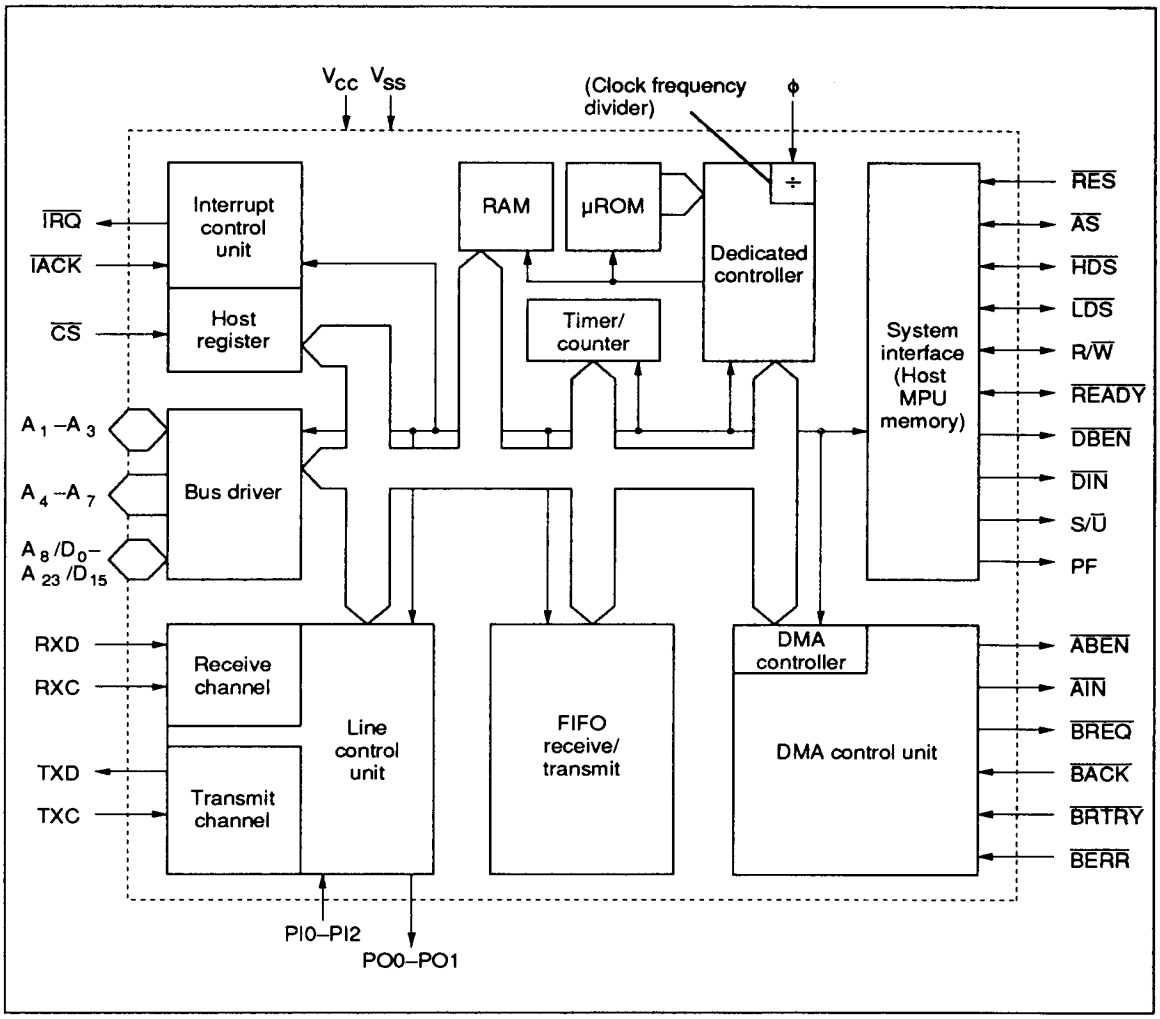
Function Summary

Table 2 summarizes HD64540 functions.

Table 2 HD64540 Function Summary

Feature	Function
Communication protocol	CCITT X.25 layer 2 (LAPB)
Line rate (data rate)	Max 5 Mbps (HD64540R) Max 64 kbps (HD64540)
Number of lines	One full duplex line
Operation mode	Terminal (DTE) mode/network (DCE) mode/transparent mode
Selectable parameters	Maximum number of retransmissions: N2
	Maximum number of octets in an information field: N1
	Maximum time allowed without receiving acknowledgement to transmitted frames (0.1 to 25.5 seconds, 0.1 second steps): T1
	Maximum time allowed for idle state (0.1 to 25.5 seconds, 0.1 second steps or 1 to 255 seconds, 1 second steps): T3
	Maximum number of outstanding I frames (1 to 127): K
	Time for delayed acknowledgement: T2
Diagnostics	Auto-echo
	Local loopback
	Auto-echo and local loopback
Peripheral I/O ports	3 inputs, 2 outputs (general-purpose I/O, level detection)
Data encoding	NRZ serial data
Data transfer with memory	DMA
Address space	16 Mbyte
Data bus width	16 bits (multiplexed with address bus)
Power supply	Single +5 V
Power consumption	130 mW (typ)
Process	CMOS 1.3-μm
Package	68-pin ceramic PGA (pin grid array), 68-pin plastic PLCC
Ordering code	HD64540B03CP, HD64540B03Y, HD64540RB04Y

Block Diagram



System Configuration

Figure 19 is an example of a system configuration using the HD64540. The HD64540 processes the signal received from the line according to protocol procedure. The processed result is sent to the host MPU. Transmit data is transferred to the line according to commands from the host MPU.

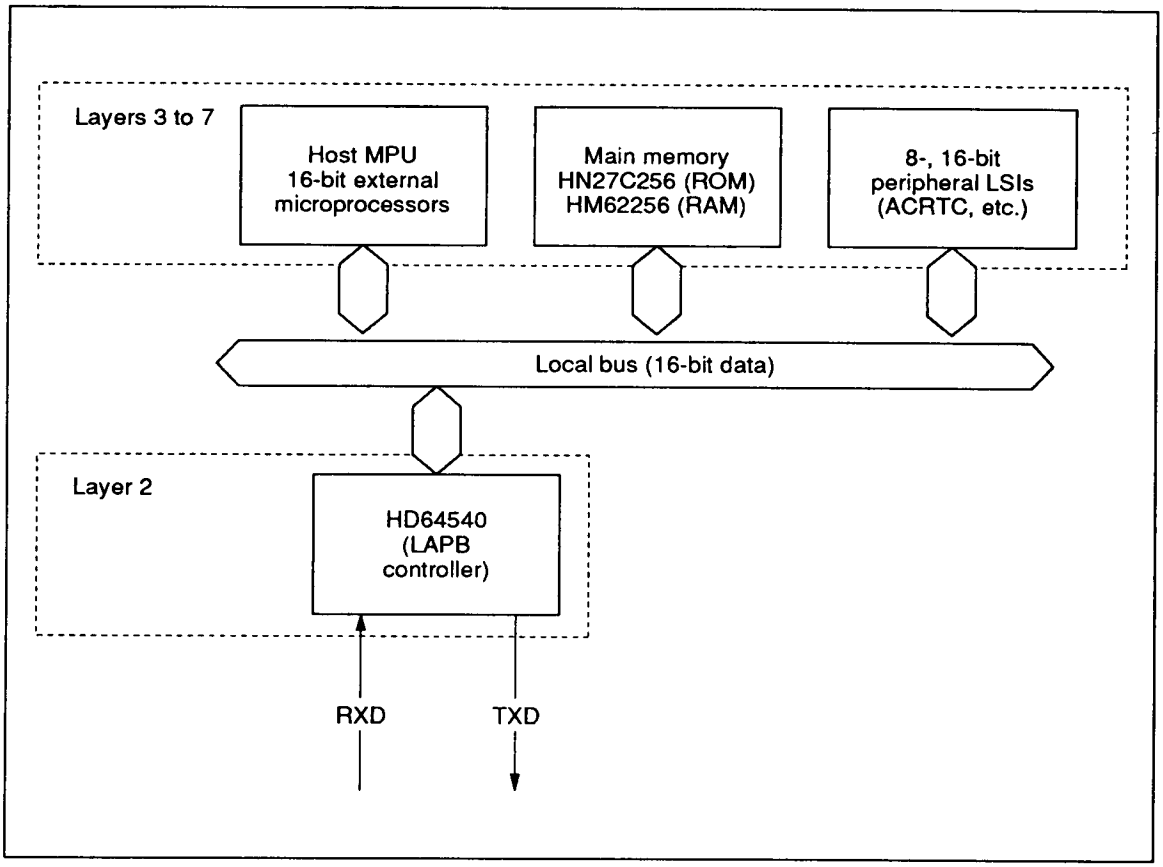


Figure 19 System Configuration Block Diagram

Absolute Maximum Ratings

Table 14 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}*2	7.0	V
Input voltage	V_{in}*2	V_{SS} – 0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	–55 to +150	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect the reliability of the LSI.
2. With respect to V_{SS} (system ground).

Recommended Operating Conditions

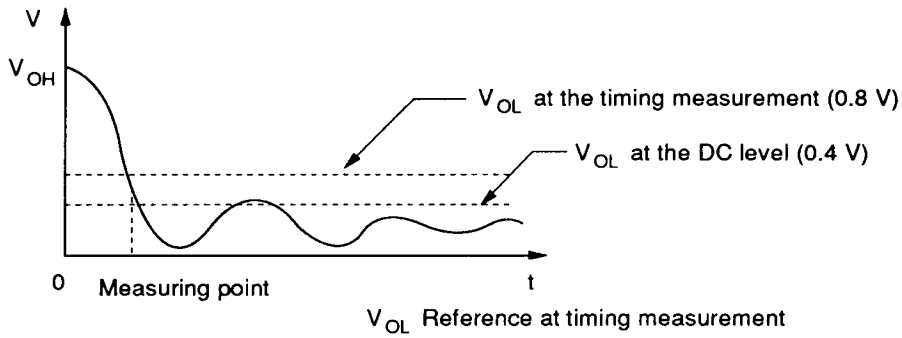
Table 15 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}Note	4.75	5.0	5.25	V
Input low level voltage	V_{IL}Note	–0.3		0.8	V
Input high level voltage	V_{IH}Note	2.0		V_{CC}	V
Operating temperature	T_{opr}	0	25	70	°C

Note: With respect to V_{SS} (system ground).

Timing measurement: The timing measurement point for the output low level is defined at 0.8 V throughout this specification.

The output low level at stable condition (DC characteristics) is defined at 0.4 V.



Electrical Characteristics

DC Electrical Characteristics

Table 16 DC Electrical Characteristics (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol		Min	Typ[Note]	Max	Unit	Condition
Input high level voltage	V_{IH}	φ (clock)	2.4	—	V_{CC}	V	
		Others	2.0	—	V_{CC}	V	
Input low level voltage	V_{IL}		–0.3	—	0.8	V	
Input leakage current	I_{IN}		—	—	2.5	µA	
Output high level voltage	V_{OH}		2.4	—	—	V	I_{OH} = –200 µA
Output low level voltage	V_{OL}		—	—	0.4	V	I_{OL} = 1.6 mA
Output leakage current	I_{LOH}		—	—	10	µA	
Pin capacitance	C_P		—	—	15	pF	V_{in} = 0 V F = 1 MHz T_a = 25°C
Current consumption	I_{CC}		—	26	50	mA	

Note: T_a = 25°C, V_{CC} = 5.0 V.