NEW PRODUCT

Rev. 15
Apr. 25, 1990

HM574256JP/ZP-35R/40/45

262,144-Word x 4-Bit High Speed Dynamic Random Access Memory

HITACHI

The Hitachi HM574256 is a super high speed dynamic RAM organized 262,144-word x 4-bit. HM574256 has realized higher density, higher performance and various functions by employing 1.3 µm Bi-CMOS technology and some new Bi-CMOS circuit design technologies. The HM574256 offers 2 bit static column mode as a high speed access mode.

Feature

* Single 5 V (±10%) for HM574256JP/ZP-40/45
  5 V (±5%) for HM574256JP/ZP-35R
* High speed
  - Access time 35ns/40ns/45ns(max)
* 512 refresh cycles ---- (4 ms)
* 2 variations of refresh
  - $\overline{CE}$ refresh
  - Automatic refresh
* 2 bits static column mode

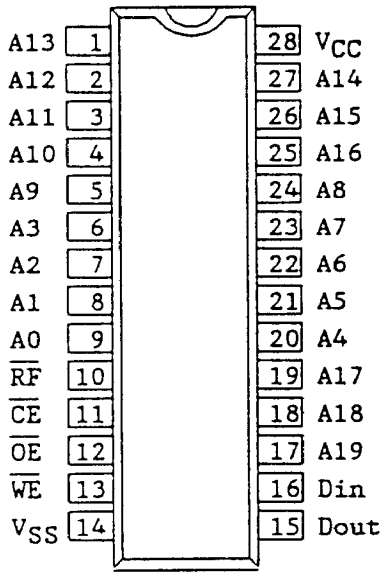
Ordering Informations

Part No.	Access	Package
HM574256JP-35R	35 ns	300 mil 28-pin plastic SOJ (CP-28DN)
HM574256JP-40	40 ns	
HM574256JP-45	45 ns	
HM574256ZP-35R*1	35 ns	400 mil 28-pin plastic ZIP
HM574256ZP-40*1	40 ns	
HM574256ZP-45*1	45 ns	

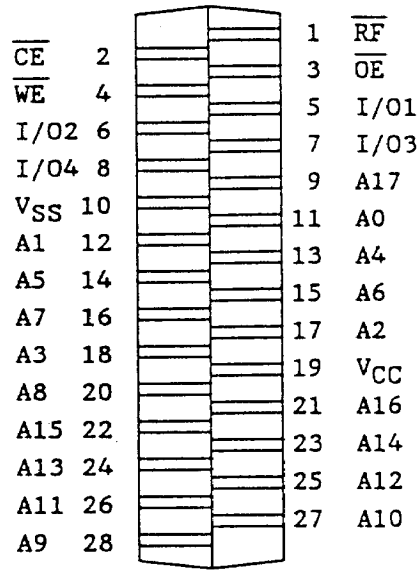
Note: 1. ZIP type products are preliminary.

Pin Arrangement

HM574256JP-35R/40/45
(Top View)



HM574256ZP-35R/40/45
(Bottom View)



Pin Description

Pin Name	Function
A0 - A8	Address input for $\overline{CE}$ refresh
A9 - A16	Address input
A17	Address input for static column mode
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Read / write enable
I/O1 - I/O4	Data in / data out
$\overline{RF}$	Refresh control
V_{CC}	Power (+5V)
V_{SS}	Ground

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_T	0.8	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage -35R	V_{CC}	4.75	5.0	5.25	V	1
Supply voltage -40/-45		4.50		5.50		
Input high voltage	V_{IH}	2.4	-	6.5	V	1, 3
Input low voltage	V_{IL}	-1.0	-	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}

2. The device will withstand undershoots to the -2 V level with a maximum pulse width of 20 ns at the -1.5 V level. (See Figure 1.)

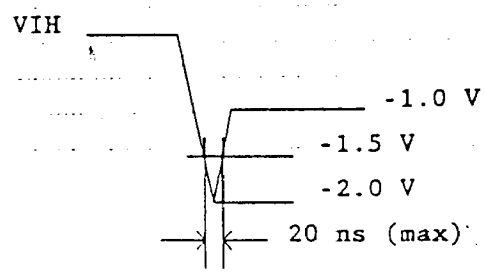


Figure 1 Undershoot of input voltage

3. The V_{IH} level of $\overline{OE}$ shall be lower than V_{CC}+0.5V.

DC Characteristics

Ta = 0 to +70 °C, V_{SS} = 0 V,
V_{CC} = 5 V ±10 % for HM574256JP-40/45,
V_{CC} = 5 V ± 5 % for HM574256JP-35R

Parameter	Symbol	HM574256 -35R Min	HM574256 -35R Max	HM574256 -40 Min	HM574256 -40 Max	HM574256 -45 Min	HM574256 -45 Max	Unit	Test Conditions	Note
Normal operating current	I_{CCA}		See figure 2					mA		1
Refresh current	I_{CCR}		See figure 2					mA		1
Standby current	I_{CCS}	-	5	-	5	-	5	mA		
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	µA	0 V < Vin < 7 V	2
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	µA	0 V < Vout < 7 V Dout = Disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -4 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 8 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. The Vin level of $\overline{OE}$ that is I_{LI} test condition of $\overline{OE}$ must be lower than Vcc+0.5V.

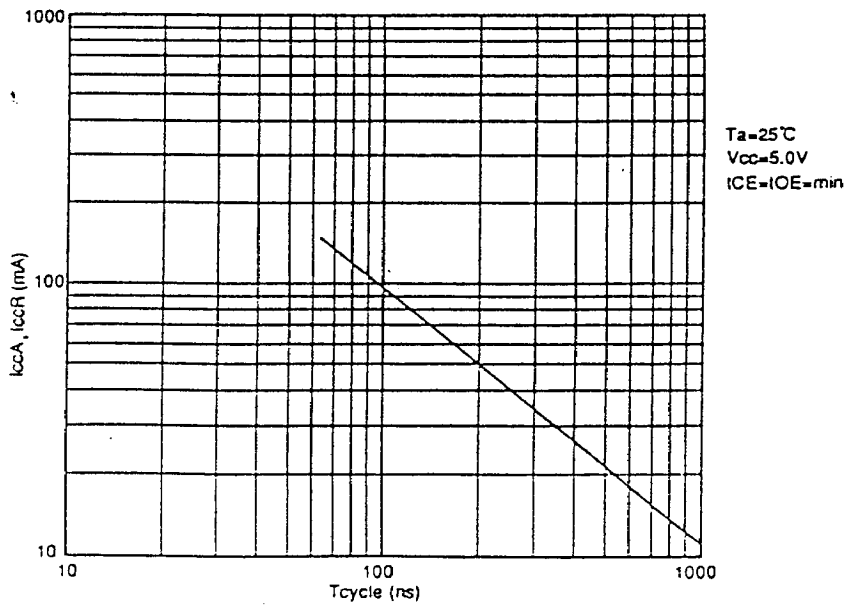


Figure 2 I_{CCA}, I_{CCR} vs Tcycle

Capacitance Ta = 25 °C,
V_{CC} = 5 V ±10 % for HM574256JP-40/45,
V_{CC} = 5 V ± 5 % for HM574256JP-35R

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data-in	Cin1	-	5	pF	1
	Clock ($\overline{CE}$, $\overline{OE}$)	Cin2	-	5	pF	1
	Clock ($\overline{WE}$, $\overline{RF}$)	Cin3	-	7	pF	1
Output capacitance (Data in / data out)		$C_{I/O}$	-	10	pF	1,2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$, $\overline{CE}$ = V_{IH} to disable Dout.

AC Characteristics [1] Ta = 0 °C to +70 °C, V_{SS} = 0 V,
V_{CC} = 5 V ±10 % for HM574256JP-40/45,
V_{CC} = 5 V ± 5 % for HM574256JP-35R

Test Conditions

Input pulse levels: V_{IH} = 3.0 V, V_{IL} = 0 V
Transition time: t_T = 3 ns
Input timing reference levels: High = 2.4 V, Low = 0.8 V (See Figure 3.)
Output timing reference levels: High = 2.4 V, Low = 0.4 V
Output load: See Figure 4.

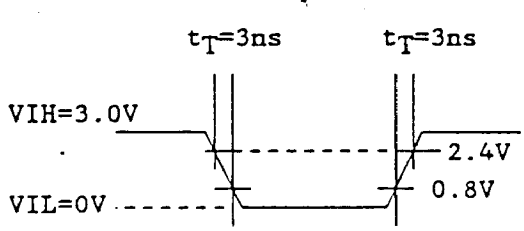


Figure 3 Input pulse

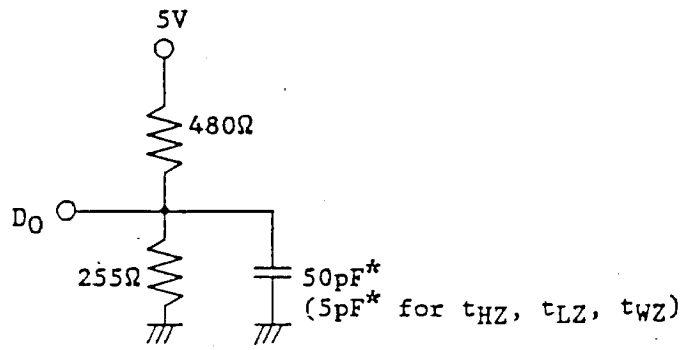


Figure 4 Output load

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM574256-35R Min	HM574256-35R Max	HM574256-40 Min	HM574256-40 Max	HM574256-45 Min	HM574256-45 Max	Unit	Note
Read / write cycle time	t_{CC}	75	---	85	---	90	---	ns	
CE pulse width	t_{CE}	35	5000	40	5000	45	5000	ns	
CE precharge time	t_{CP}	34	---	39	---	39	---	ns	
Address setup time	t_{AS}	0	---	0	---	0	---	ns	
Address hold time	t_{AH}	5	---	5	---	5	---	ns	
Transition time (rise and fall)	t_T	1	10	1	10	1	10	ns	
Refresh period	t_{REF}	---	4	---	4	---	4	ms	

Read Cycle

Parameter	Symbol	HM574256-35R Min	HM574256-35R Max	HM574256-40 Min	HM574256-40 Max	HM574256-45 Min	HM574256-45 Max	Unit	Note
Access time from $\overline{CE}$	t_{ACS}	---	35	---	40	---	45	ns	
Address access time	t_{AA}	---	25	---	30	---	30	ns	
Access time from $\overline{OE}$	t_{OAC}	---	20	---	25	---	25	ns	
Setup time on read	t_{RS}	0	---	0	---	0	---	ns	
Hold time on read	t_{RH}	5	---	5	---	5	---	ns	
$\overline{OE}$ setup time	t_{OES}	5	---	5	---	5	---	ns	
$\overline{OE}$ enable to output in low-Z	t_{LZ}	0	---	0	---	0	---	ns	
$\overline{OE}$ disable to output in high-Z	t_{HZ}	---	15	---	20	---	20	ns	
Output hold time from address	t_{AOH}	3	---	3	---	3	---	ns	
Output hold time from $\overline{CE}$	t_{COH}	0	---	0	---	0	---	ns	
$\overline{CE}$ to $\overline{OE}$ precharge time	t_{COP}	10	---	10	---	10	---	ns	

Write Cycle

Parameter	Symbol	HM574256-35R Min	HM574256-35R Max	HM574256-40 Min	HM574256-40 Max	HM574256-45 Min	HM574256-45 Max	Unit	Note
Data setup time	t_{DW}	20	---	25	---	30	---	ns	
Data hold time	t_{DH}	5	---	5	---	5	---	ns	
Setup time on early write	t_{ES}	5	---	5	---	5	---	ns	
$\overline{WE}$ pulse width	t_{WP}	25	---	30	---	35	---	ns	
Write hold time from $\overline{CE}$	t_{WH}	35	---	40	---	45	---	ns	
$\overline{WE}$ enable to output in high-Z	t_{WZ}	---	15	---	20	---	20	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	15	---	20	---	20	---	ns	
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	---	20	---	20	---	ns	
$\overline{CE}$ setup time from Din	t_{DZC}	0	---	0	---	0	---	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM574256-35R Min	HM574256-35R Max	HM574256-40 Min	HM574256-40 Max	HM574256-45 Min	HM574256-45 Max	Unit	Note
$\overline{WE}$ delay time from $\overline{CE}$	t_{CWD}	35	---	40	---	45	---	ns	

Refresh Cycle

Parameter	Symbol	HM574256-35R Min	HM574256-35R Max	HM574256-40 Min	HM574256-40 Max	HM574256-45 Min	HM574256-45 Max	Unit	Note
$\overline{RF}$ setup time	t_{FS}	5	---	5	---	5	---	ns	
$\overline{RF}$ hold time	t_{FH}	15	---	15	---	15	---	ns	
Mode selection setup time	t_{MS}	0	---	0	---	0	---	ns	
Mode selection hold time	t_{MH}	15	---	20	---	20	---	ns	
Setup time on $\overline{CE}$ refresh	t_{CRS}	15	---	20	---	20	---	ns	

Static Column Mode Cycle

Parameter	Symbol	HM574256-35R Min	HM574256-35R Max	HM574256-40 Min	HM574256-40 Max	HM574256-45 Min	HM574256-45 Max	Unit	Note
Static column address setup time	t_{ASZ}	20	---	25	---	25	---	ns	
Address setup time to $\overline{WE}$	t_{WS}	0	---	0	---	0	---	ns	
Address hold time from $\overline{WE}$	t_{WR}	0	---	0	---	0	---	ns	

Notes:

1. If $t_{OES} > t_{OES}(min)$ and $\overline{OE}$ is held at low level, Dout will be valid until the next negative transition of $\overline{CE}$.

2. Both t_{WH} and t_{WP} must be satisfied for a delayed write cycle.

3. If $t_{COP} < t_{COP}(min)$, Dout cannot be guaranteed to be in high impedance.

4. If the negative transition of $\overline{OE}$ occurs before that of $\overline{CE}$, t_{LZ} is controlled by $\overline{CE}$.

5. t_{WP} and t_{DW} are specified by the positive transition of $\overline{CE}$ or $\overline{WE}$ whichever occurs earlier.

6. When $\overline{WE}$ goes low, Dout becomes high impedance and is held in this condition to the next cycle. If the negative transition of $\overline{WE}$ occurs before that of $\overline{CE}$, Dout is controlled by $\overline{CE}$. t_{WZ} defines the time at which the output achieves the open circuit condition.

7. If $t_{ES} > t_{ES}(min)$, the cycle is early write and Dout is in high impedance.

8. In static column mode cycles, read operation cannot be performed after write operation.

9. Both t_{AH} and t_{WR} must be satisfied for a write cycle.

10. t_{HZ} defines the time at which the output achieves the open circuit condition.

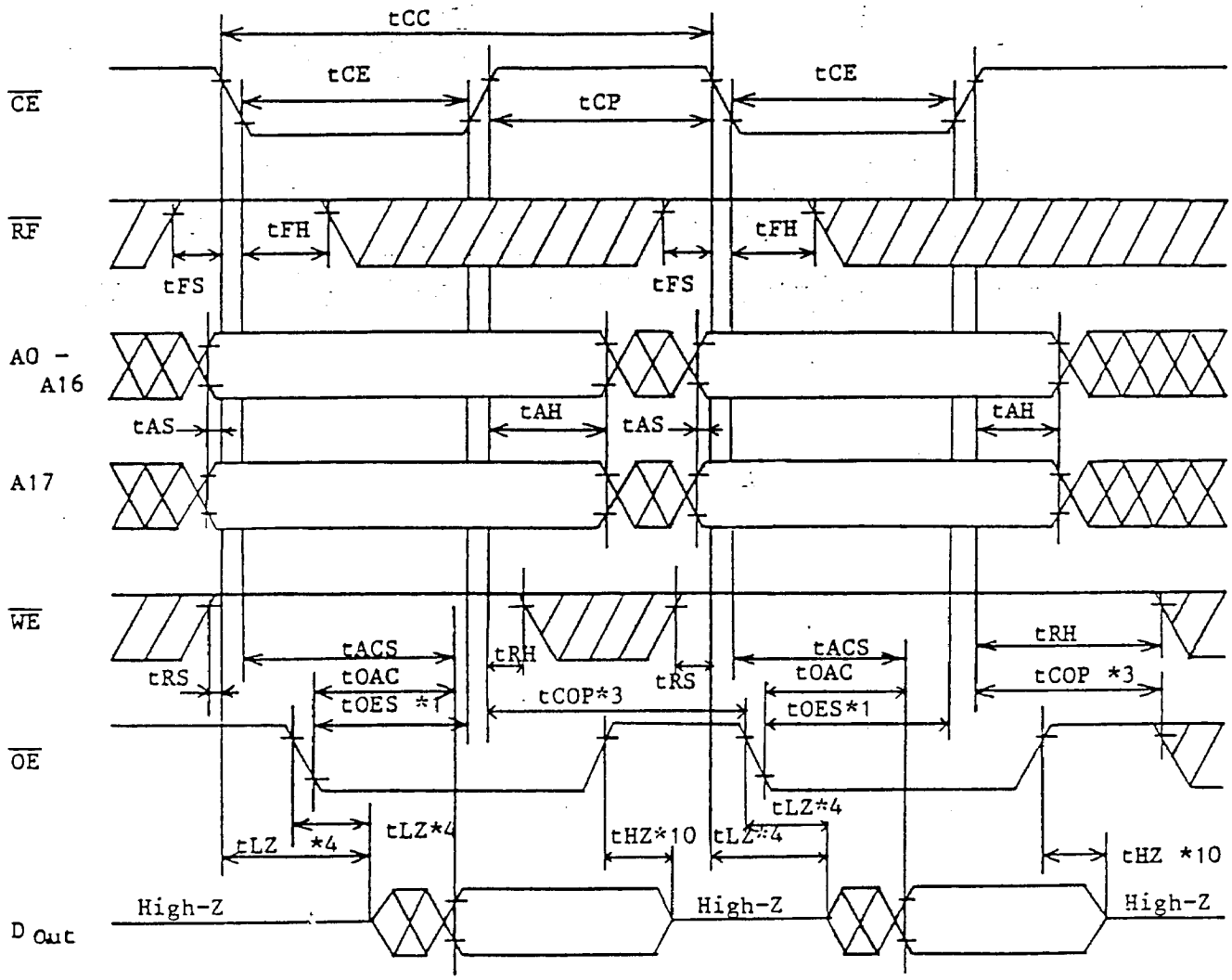
11. An initial pause of 100 µs is required after power-up, then execute at least eight $\overline{CE}$ refresh cycles.

12. During I/O pins are in the output state, Data-in shall not be applied to I/O pins. So, in all write cycles (early write, delayed write and read-modify-write), $\overline{OE}$ must go to high level to disable the output buffer prior to applying data to the device.

13. In static column mode cycle, there must not be any invalid address inputs for static column mode(A17) which are less than t_{AA}.

Timing Waveforms

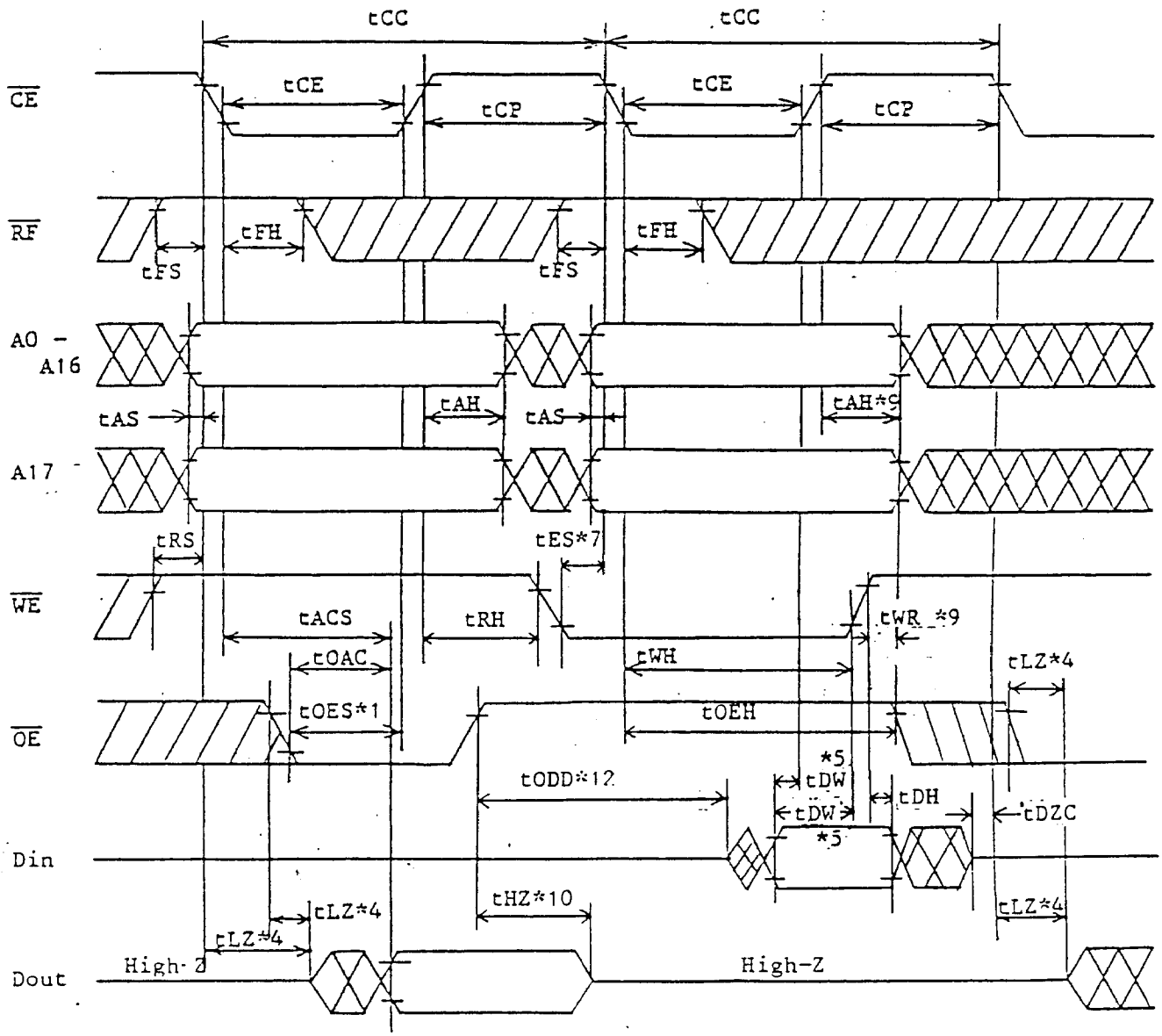
Read / Read Cycle



* D_{in}: Don't care

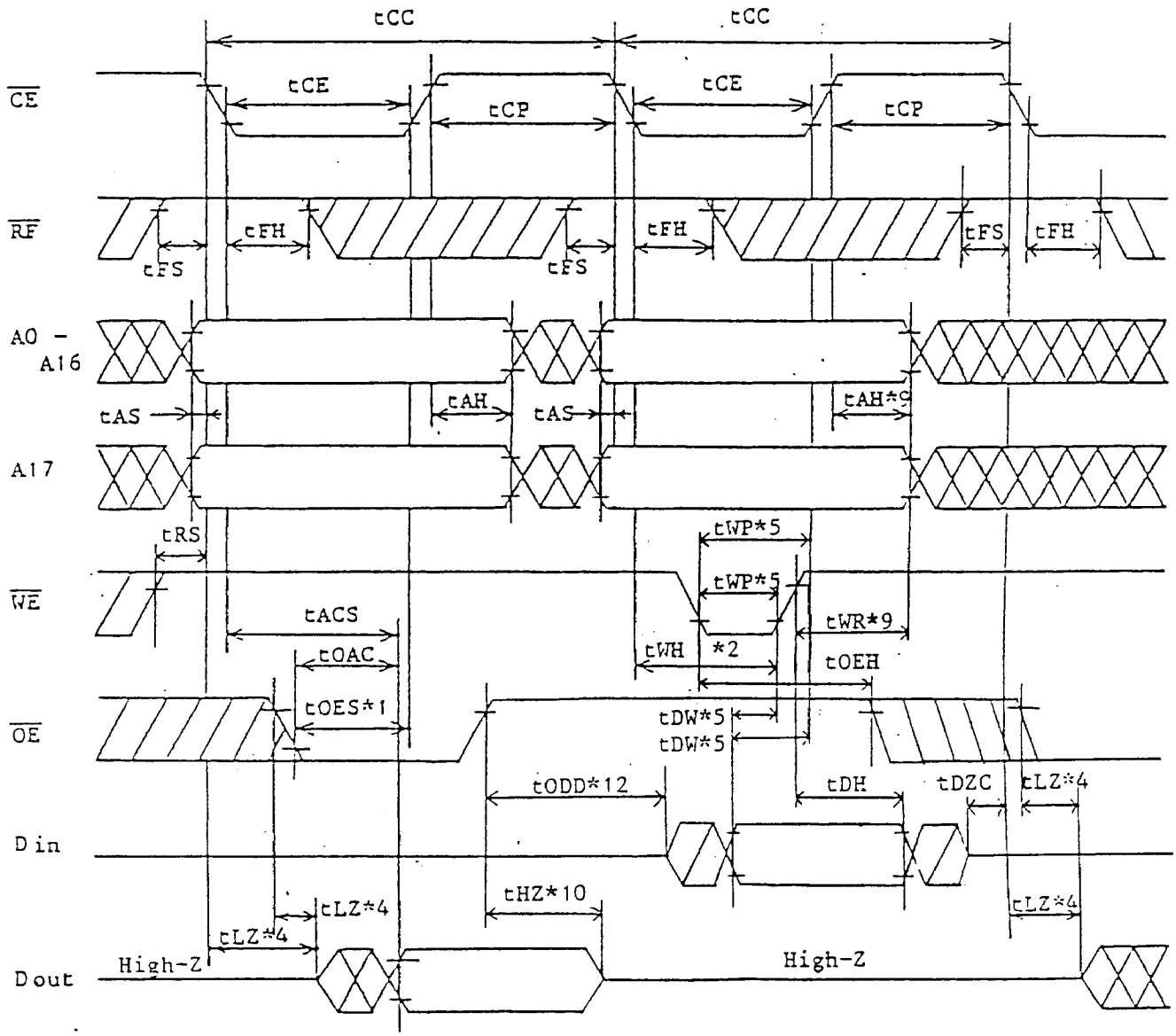
** ▨: Don't care

Read / Early Write Cycle



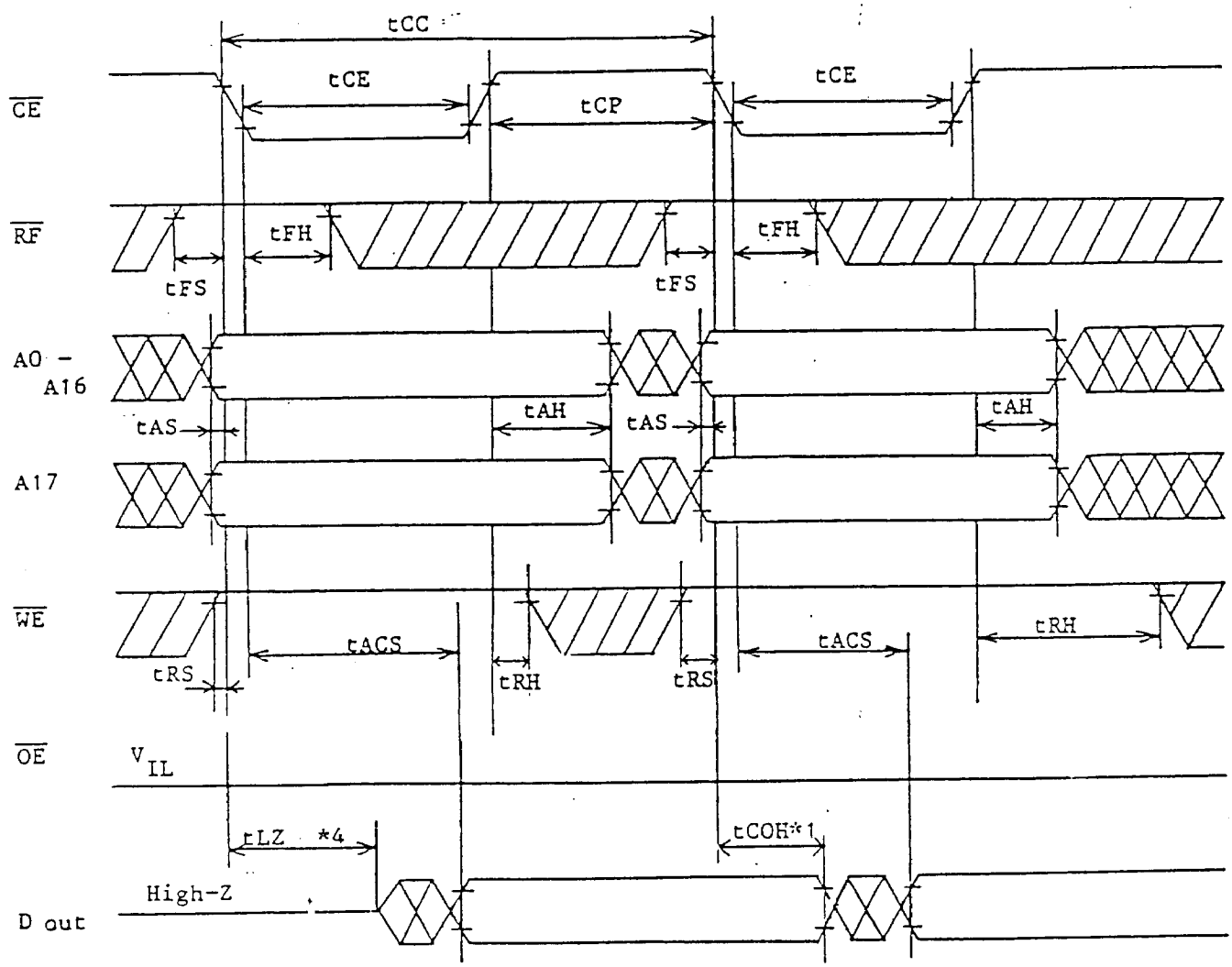
* //// : Don't care

Read / Delayed Write Cycle



* //// : Don't care

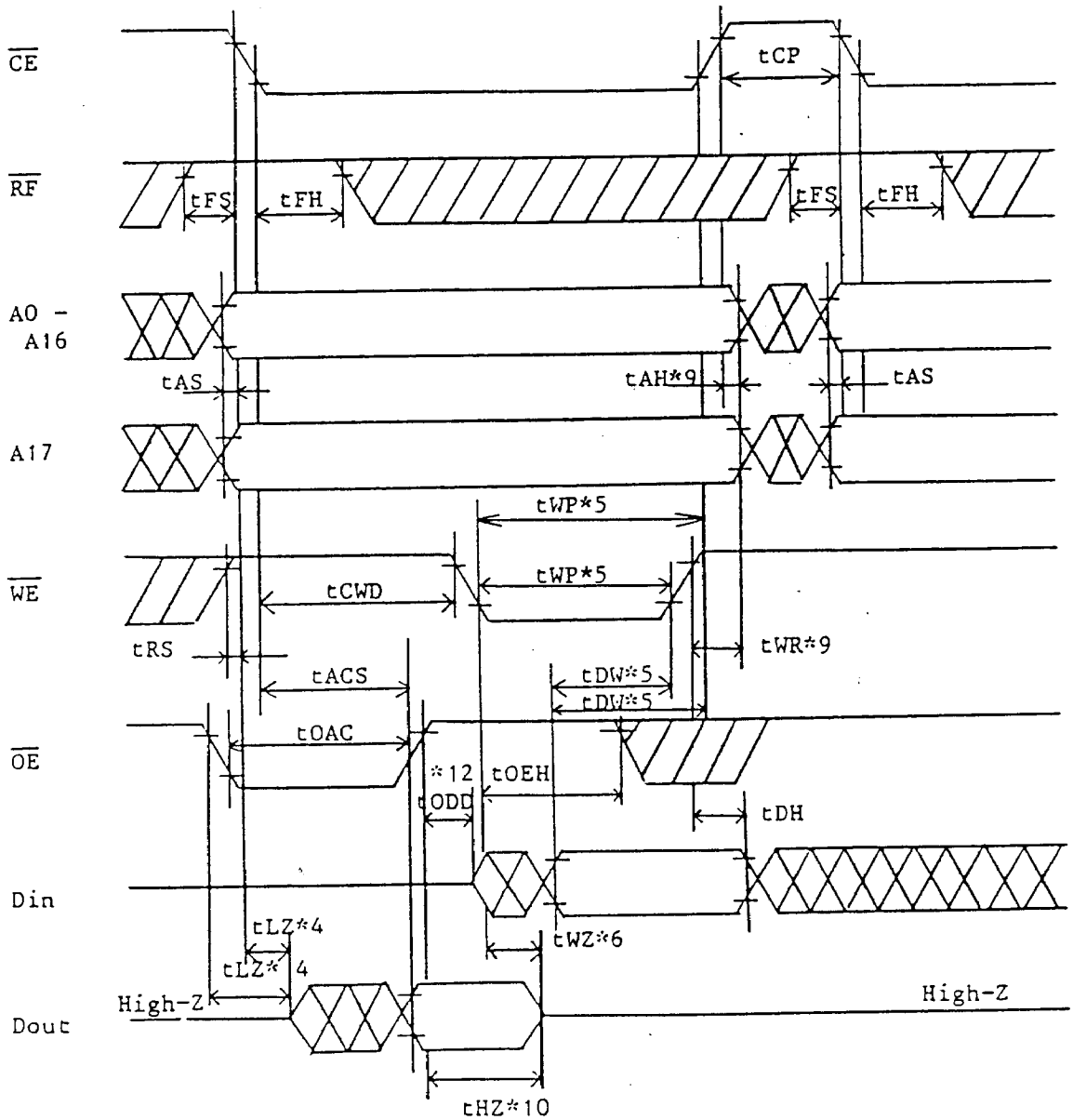
Read / Read Cycle ($\overline{OE}$ = V_{IL})



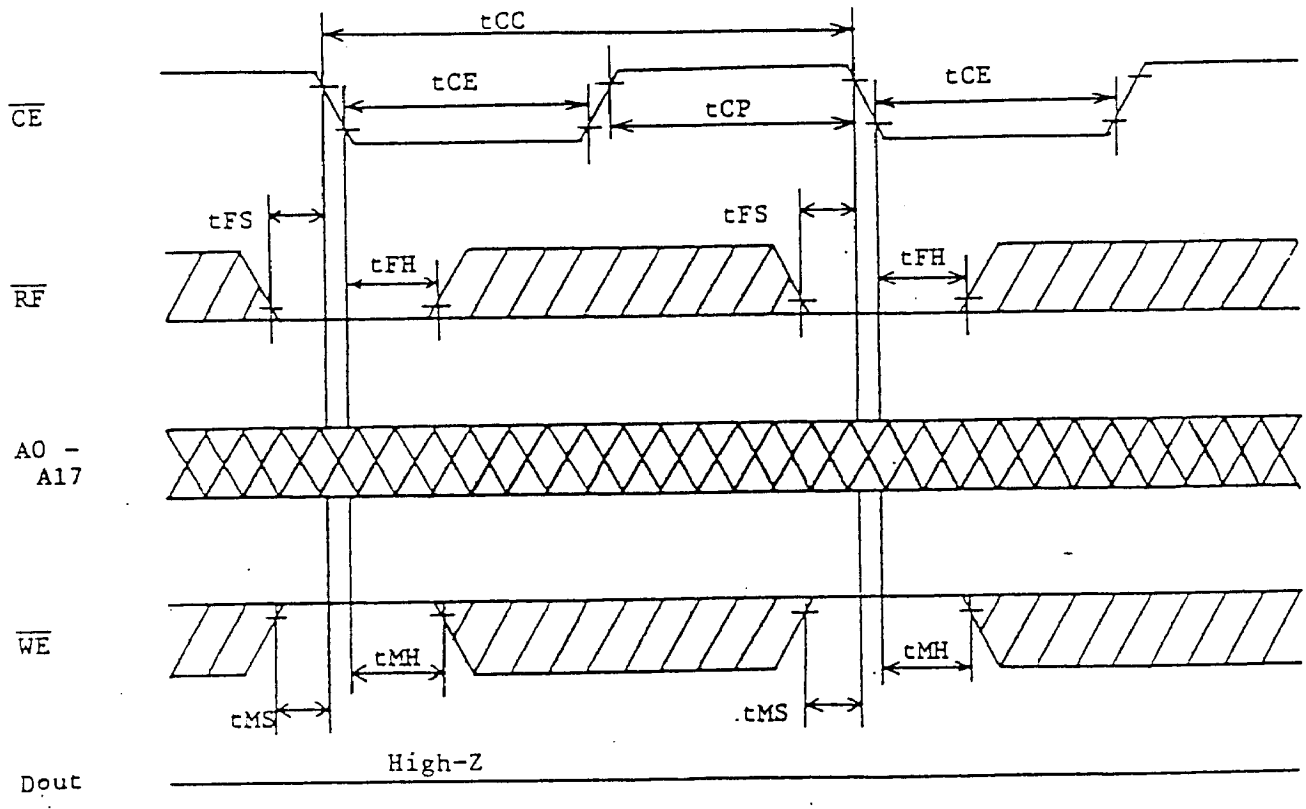
* Din: Don't care

** ▨: Don't care

Read-Modify-Write Cycle



Automatic Refresh Cycle

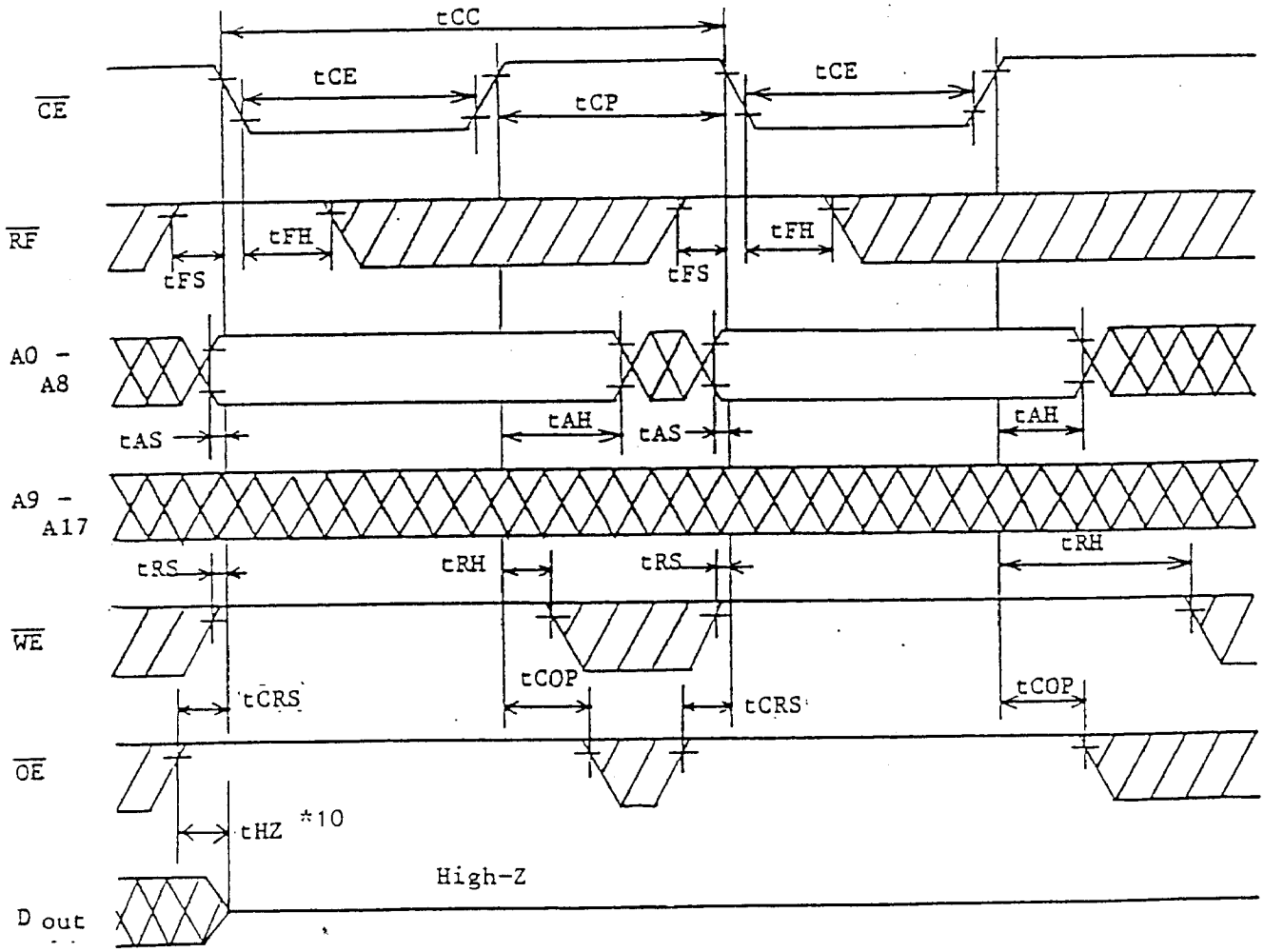


* A0 – A17 : Don't care

** $\overline{OE}$, Din : Don't care

*** ▨ : Don't care

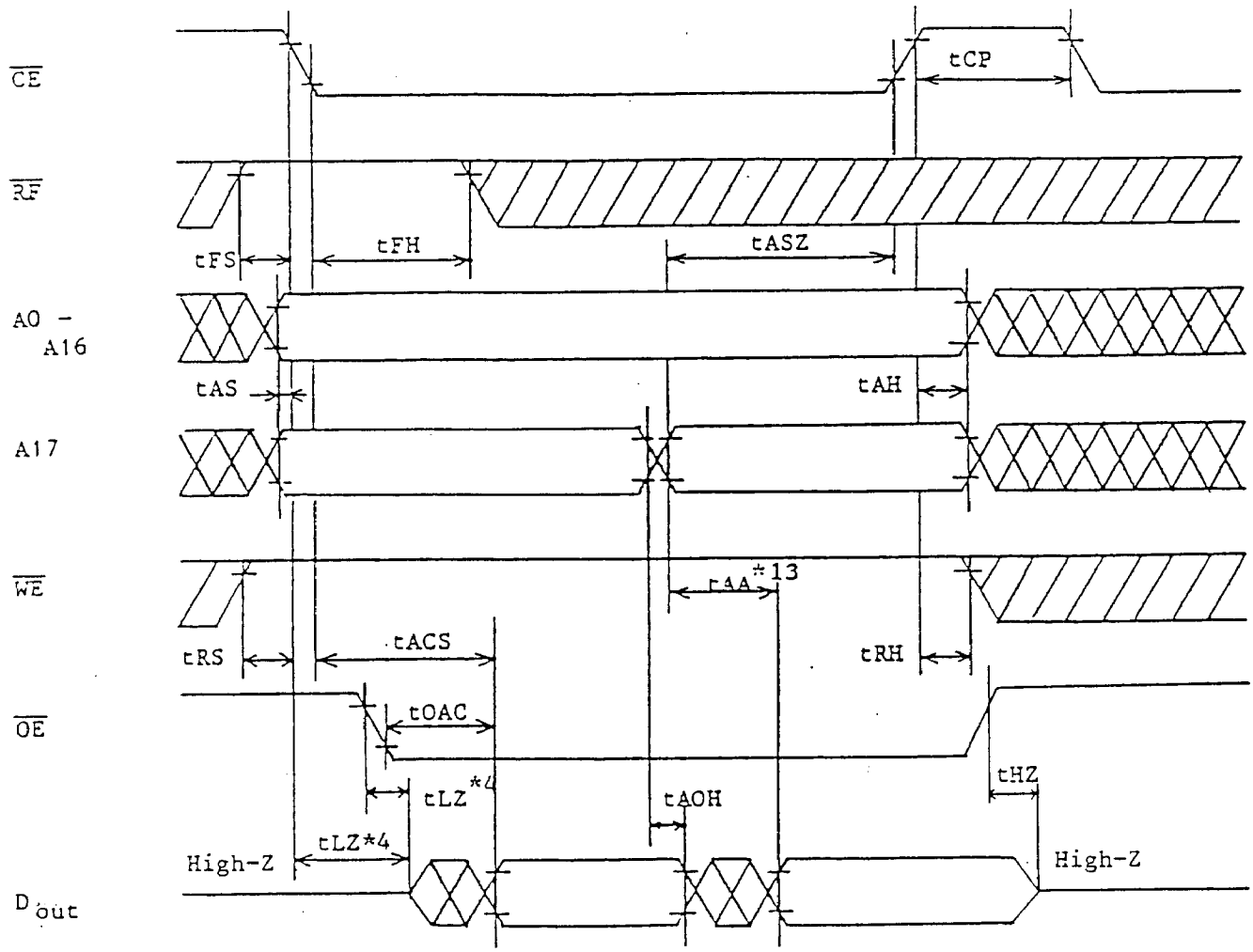
$\overline{CE}$ Refresh



* Din : Don't care

** ▨ : Don't care

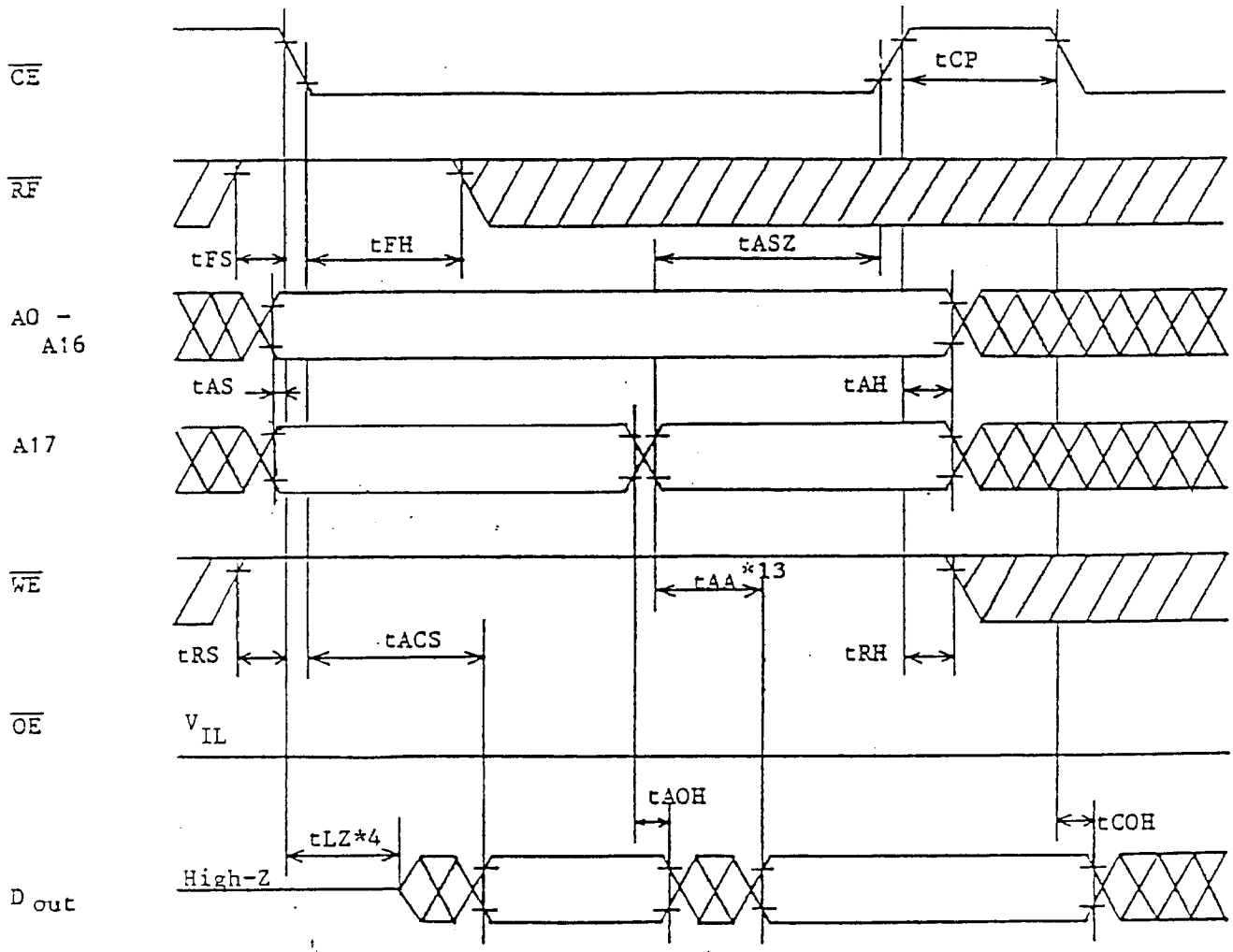
Static Column Mode Read Cycle



* Din: Don't care

** ▨ : Don't care

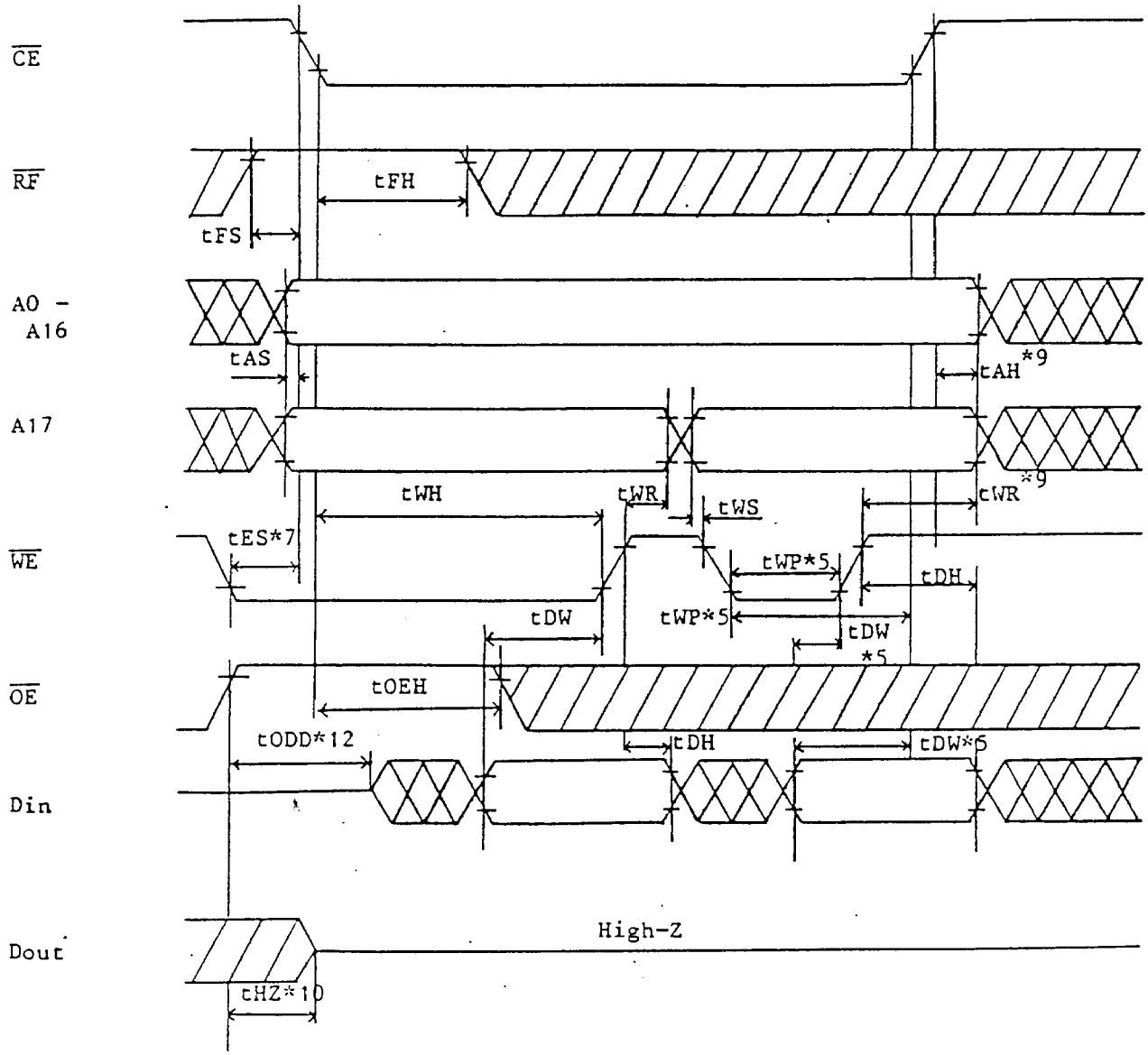
Static Column Mode Read Cycle ($\overline{OE}$ = V_{IL})



* Din: Don't care

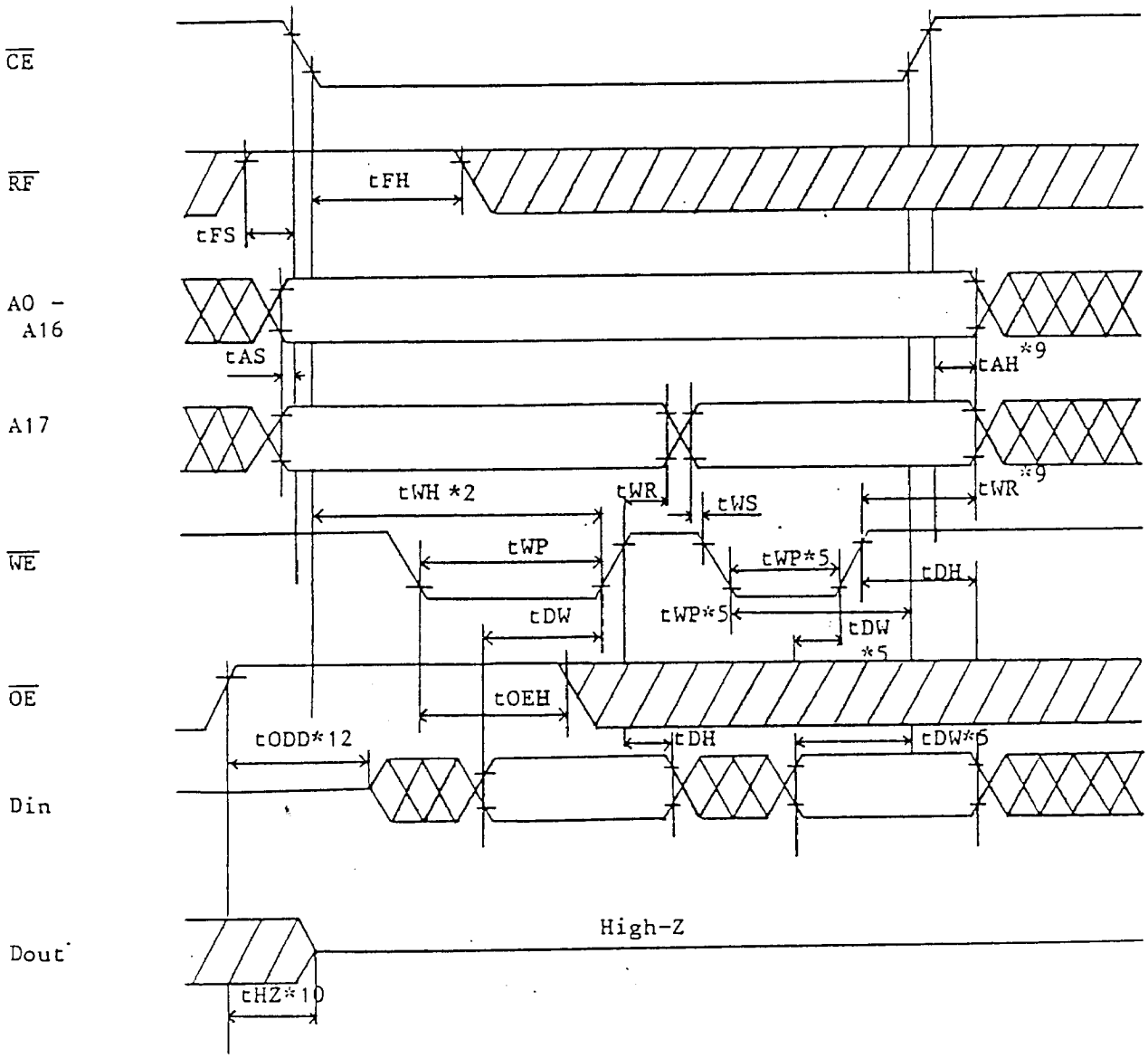
** ▨ : Don't care

Static Column Mode Write Cycle *8 (1st cycle = Early Write Cycle)



* ▨ : Don't care

Static Column Mode Write Cycle *8 (1st cycle = Delayed Write Cycle)



* ▨ : Don't care

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