# HN27V101ATT/ARR Series

**Preliminary** 

131072-Word × 8-Bit CMOS One Time Electrically Programmable ROM (with Low V<sub>CC</sub>)

The HN27V101ATT/ARR series are 131072-word  $\times$  8-bit one time electrically programmable ROM. Initially, all bits of the HN27V101ATT/ARR series are in the "1" state (output high).

Data is introduced by selectively programming "0" into the desired bit location. This device is packaged in a 32-pin plastic package, therefore, this device cannot be rewritten and erased.

The packages of the HN27V100ATT/ARR series are surface mount thin and small outline packages. They are suitable for hand-held equipment such as a memory card.

#### **Features**

- Low voltage and
  - wide range operation: 2.7 V to 5.5 V
- Fast high-reliability programming mode and fast high-reliability page programming mode
  - Programming voltage: +12.5 V DC
  - Fast high-reliability page programming:

14 sec typ

- High speed inputs and outputs TTL compatible during both read and program modes
- Low power dissipation: 50 mW/MHz typ (active)

5 μW typ (standby)

- Pin arrangement: 32-pin JEDEC standard except HN27V101ARR series
- Package
  - Surface mount thin and small outline package (TSOP) type II: HN27V101ATT series
  - TSOP type II reverse type: HN27V101ARR series
- Device identifier mode: manufacturer code and device code

#### **Ordering Information**

Type No.	Access time	Package	
HN27V101ATT-20	200 ns	32-pin plastic TSOP-(II) (TTP-32D)	
HN27V101ATT-25	250 ns		
HN27V101ARR-20	200 ns	32-pin plastic TSOP-(II) (TTP-32DR)	
HN27V101ARR-25	250 ns		

## **HN27V101ATT/ARR Series**

### Pin Arrangement

HN27V101ATT Series		HN27V101ARR Series	
V <sub>PP</sub> □1	32 \( \sum_{CC} \)	<u>V<sub>CC</sub></u> □ 32	1 V <sub>PP</sub>
A16 □2 ·	31 🗀 PGM	PGM □31	<sup>1</sup> 2 □ A16
A15 □3	30 🔲 NC	NC □30	3 🗆 A15
A12 □ 4	29 🗀 <b>A</b> 14	A14 □29	4 🗆 A12
A7 □ 5	28 🗀 A13	A13 <u>□</u> 28	5 🗆 A7
A6 □ 6	27 🗀 A8	A8 □27	6 🗆 A6
<b>A</b> 5 □ 7	26 🗀 A9	<b>A</b> 9	7 🗆 <b>A5</b>
A4 □ 8	25 🗀 A11	A11	8 🗀 A4
<b>A3</b> □ 9	24 🗆 OE	ŌE	9 🗆 A3
A2 ☐ 10	23 🗀 A10	A10	10 🗆 A2
A1 □ 11	22 🗆 CE	CE	11 🗆 A1
A0 ☐ 12	21 🗀 1/07	I/O7	12 🗆 A0
I/O0 □ 13	20 🔲 I/O6	I/O6	13 🗆 I/O0
I/O1 ☐ 14	19 🗀 I/O5	I/O5 ☐ 19	14 🗀 I/O1
I/O2 🗆 15	18 🗀 I/O4	l/O4	15 🗆 I/O2
V <sub>SS</sub> □16	17 🗀 I/O3	I/O3 🗀 17	16 □ V <sub>SS</sub>
(Top V	/iew)	(Top	View)