

FEATURES

- 8K x 8 CMOS Static RAM with 8-bit Tag Comparison Logic
- High Speed Address-to-MATCH — 12 ns maximum
- High Speed Flash Clear
- High Speed Read Access Time — 12 ns maximum
- Low Power Operation
Active: 320 mW typical at 35 ns
Standby: 500 μ W typical
- Data Retention at 2 V for Battery Backup Operation
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT7174, IDT71B74, MK48H74
- Package Styles Available:
 - 28-pin Plastic DIP
 - 28-pin CerDIP
 - 28-pin SOJ
 - 32-pin Ceramic LCC

DESCRIPTION

The L7C174 is a high-performance, low power CMOS static RAM optimized for use as the address tag comparator in high speed cache memory systems. One L7C174 can be used to map 8K cache lines into a 1 megabyte address space by comparing 20 address bits organized as 13-line address bits and 7-page address bits.

The storage circuitry is organized as 8192 words by 8 bits per word and includes an 8-bit data comparator with MATCH output. The 8-bit data is input/output on shared I/O pins and comparison is performed between 8-bit incoming data and accessed memory locations. Also provided is a high speed CLEAR control which clears all memory locations to zero when activated. This allows all address tag bits to be cleared when powering on or when flushing the cache.

This device is available in five speed grades with maximum address-to-MATCH times of 12 ns to 35 ns. Operation is from a single +5 V power supply with power consumption only being 320 mW (typical) at 35 ns. Dissipation drops to 0.5 mW (typical) when the memory is deselected (Enable is high).

The L7C174 consumes only 30 μ W (typical) at 3 V allowing effective battery backup operation. For minimal power consumption, data may be retained in inactive storage with a supply voltage as low as 2 V.

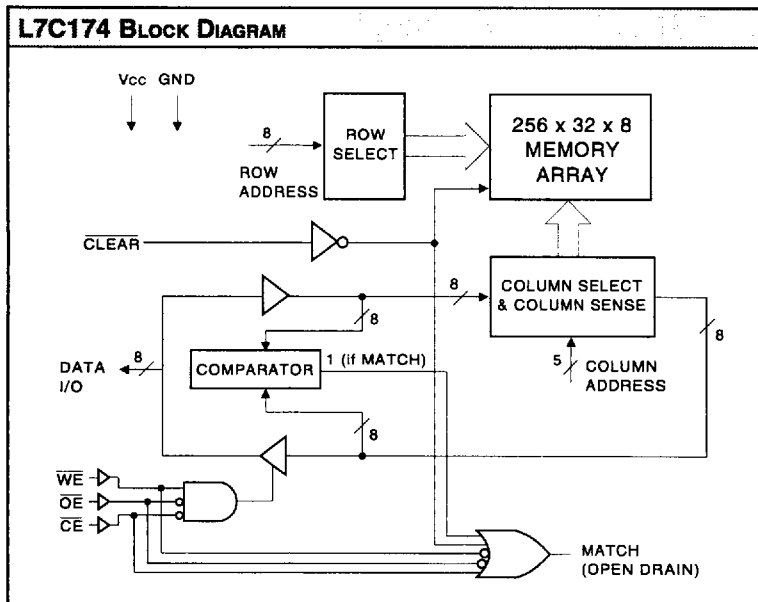
The L7C174 provides fully asynchronous (unlocked) operation with matching access and cycle times. An active low Chip Enable and Output Enable along with a three state I/O bus simplify the connection of several chips for increased storage capacity. Wide tag addresses are easily accommodated by paralleling devices and Wire-ORing the MATCH outputs. A low on the MATCH output indicates a data mismatch.

Memory locations are specified on address pins A0 through A12 with functions defined in the Truth Table.

During CLEAR, the state of the I/O pins remain completely defined by the WE, CE, and OE control inputs. Data In has the same polarity as Data Out.

Latchup and static discharge protection are provided on-chip. The L7C174 can withstand an injection current of up to 200 mA on any pin without damage.

L7C174 BLOCK DIAGRAM



TRUTH TABLE						
WE	CE	OE	CLEAR	MATCH	I/O	FUNCTION
X	X	X	L	H	—	Reset all bits to low
X	H	X	H	H	High-Z	Deselect chip
H	L	H	H	L	DIN	No MATCH
H	L	H	H	H	DIN	MATCH
H	L	L	H	H	DOUT	Read
L	L	X	H	H	DIN	Write

X = Don't Care; L = VIL; H = VIH

MAXIMUM RATINGS
Above which useful life may be impaired (Notes 1, 2)

Storage temperature	-65°C to +150°C
Operating ambient temperature	-55°C to +125°C
VCC supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-3.0 V to +7.0 V
Signal applied to high impedance output	-3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	-55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	-55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

ELECTRICAL CHARACTERISTICS Over Operating Conditions (Note 5)

Symbol	Parameter	Test Condition	L7C174			Unit
			Min	Typ	Max	
VOH	Output High Voltage (Note 11)	VCC = 4.5 V, IOH = -4.0 mA (all except MATCH pin)	2.4			V
VOL	Output Low Voltage (Note 11)	IOL = 8.0 mA (all except MATCH pin)			0.4	V
		IOL = 18.0 mA (MATCH pin)			0.4	V
VIH	Input High Voltage		2.2		VCC + 0.3	V
VIL	Input Low Voltage	(Note 3)	-3.0		0.8	V
IIX	Input Leakage Current	Ground ≤ VIN ≤ VCC	-10		+10	µA
IOZ	Output Leakage Current	Ground ≤ VOUT ≤ VCC, OE = VCC (except MATCH pin)	-10		+10	µA
ICC3	VCC Current, CMOS Standby	(Note 8)		100	500	µA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		10	250	µA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

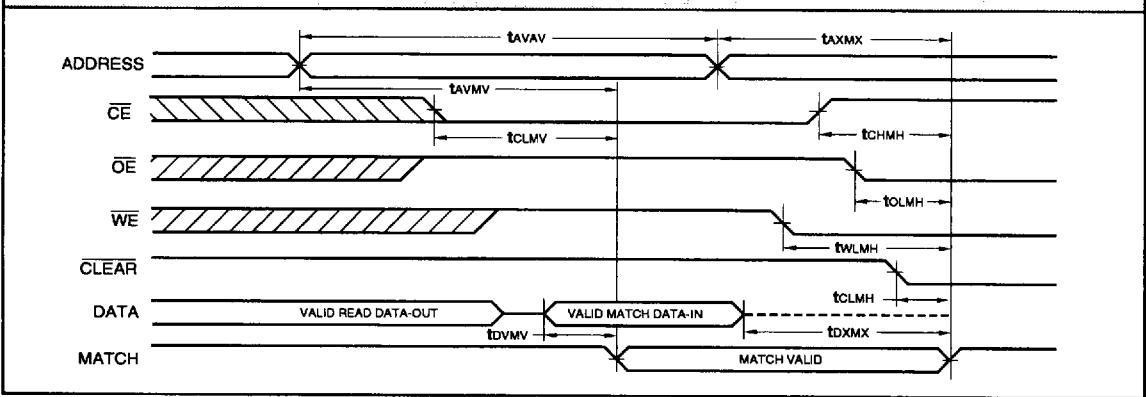
Symbol	Parameter	Test Condition	L7C174-					Unit
			35	25	20	15	12	
ICC1	VCC Current, Active	(Note 6)	110	150	185	240	275	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

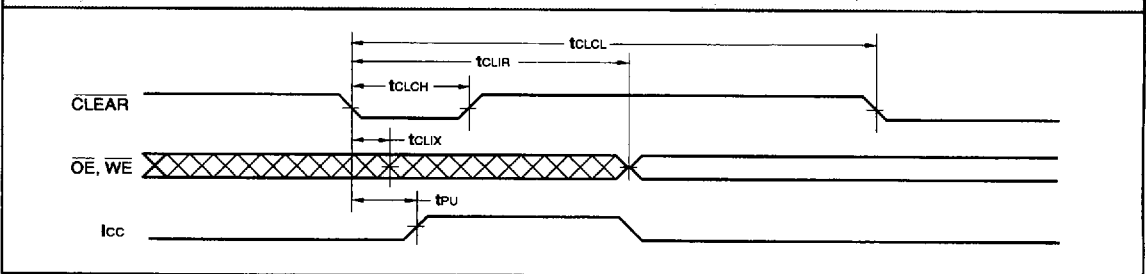
MATCH AND CLEAR CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

Symbol	Parameter	L7C174-									
		35		25		20		15		12	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	MATCH Cycle Time	35		25		20		15		12	
tAVMV	Address Valid to MATCH Valid		30		22		20		15		12
tAXMX	Address Change to MATCH Change	3		3		3		3		3	
tCLMV	Chip Enable Low to MATCH Valid		20		15		10		10		8
tCHMH	Chip Enable High to MATCH High	3		3		3		3		3	
tOLMH	Output Enable Low to MATCH High	3		3		3		3		3	
tWLMH	Write Enable Low to MATCH High	3		3		3		3		3	
tCLMH	CLEAR Low to MATCH High	0	25	0	20	0	15	0	12	0	10
tDVMV	Data Valid to MATCH Valid		20		15		15		13		10
tDXMX	Data Change to MATCH Change	0		0		0		0		0	
tCLCL	CLEAR Cycle Time	65		55		45		35		30	
tCLCH	CLEAR Pulse Width	20		15		15		12		12	
tCLIX	CLEAR Low to Inputs Don't Care	0		0		0		0		0	
tCLIR	CLEAR Low to Inputs Recognized		70		60		50		50		45

MATCH CYCLE *Note 19*

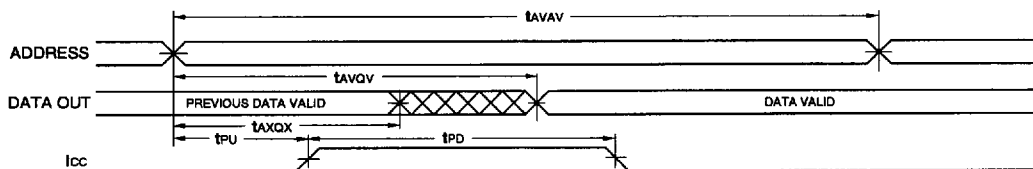
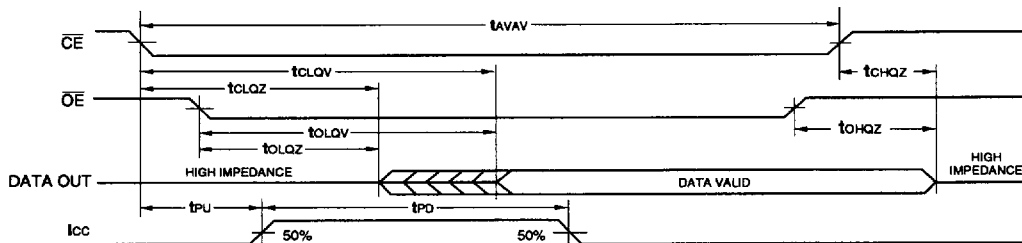
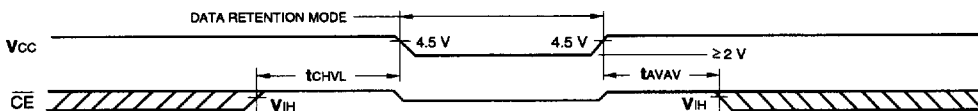


CLEAR CYCLE *Note 25*



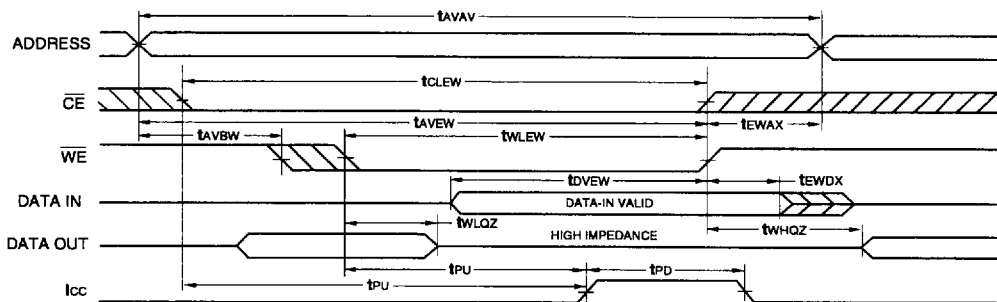
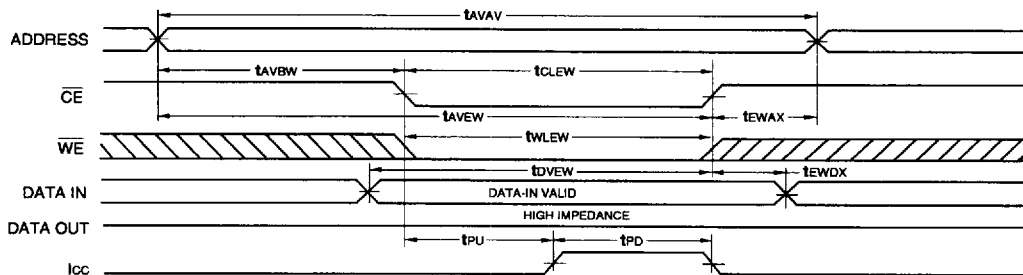
SWITCHING CHARACTERISTICS *Over Operating Range*
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

Symbol	Parameter	L7C174-									
		35		25		20		15		12	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t _{AVAV}	Read Cycle Time	35		25		20		15		12	
t _{AVQV}	Address Valid to Output Valid (Notes 13, 14)		35		25		20		15		12
t _{AXQX}	Address Change to Output Change	3		3		3		3		3	
t _{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		15		12		10		8		8
t _{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3		3	
t _{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		15		10		8		8		5
t _{OLQV}	Output Enable Low to Output Valid		15		12		10		8		6
t _{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0		0	
t _{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		12		10		8		5		5
t _{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0		0	
t _{PD}	Power Up to Power Down (Notes 10, 19)		35		25		20		20		20
t _{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0		0	

READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*

READ CYCLE — CE/OE CONTROLLED *Notes 13, 15*

DATA RETENTION *Note 9*


SWITCHING CHARACTERISTICS *Over Operating Range*
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

Symbol		Parameter		L7C174-									
				35		25		20		15		12	
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	25		20		20		15		12			
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10			
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0			
tAVEV	Address Valid to End of Write Cycle	25		15		15		12		10			
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0			
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10			
tdVEV	Data Valid to End of Write Cycle	15		10		10		7		6			
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0			
tWHQZ	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0		0			
tWLQZ	Write Enable Low to Output High Z (Notes 20, 21)		10		7		7		5		4		

WRITE CYCLE — WE CONTROLLED *Notes 16, 17, 18, 19*

WRITE CYCLE — CE CONTROLLED *Notes 16, 17, 18, 19*


NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at -0.6 V . A current in excess of 100 mA is required to reach -2.0 V . The device can withstand indefinite operation with inputs as low as -3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{\text{CE}}_1 \leq \text{VIL}$, $\text{CE}_2^* \geq \text{VH}$, $\overline{\text{WE}} \leq \text{VIL}$. Input pulse levels are 0 to 3.0 V .

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{\text{CE}}_1 \geq \text{VH}$, $\text{CE}_2^* \leq \text{VIL}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{\text{CE}}_1 = \text{VCC}$, $\text{CE}_2^* = \text{GND}$. Input levels are within 0.2 V of VCC or GND .

9. Data retention operation requires that VCC never drop below 2.0 V . $\overline{\text{CE}}_1$ must be $\geq \text{VCC} - 0.2\text{ V}$ or CE_2^* must be $\leq 0.2\text{ V}$. All other inputs must meet $\text{VIN} \geq \text{VCC} - 0.2\text{ V}$ or $\text{VIN} \leq 0.2\text{ V}$ to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{\text{CE}}_1$, CE_2^* , and $\overline{\text{WE}}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns , reference levels of 1.5 V , output loading for specified IOL and IOH plus 30 pF (Figs. 1a, 1c), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tAVEW is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{\text{WE}}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{\text{CE}}_1$ low, CE_2^* high).

15. All address lines are valid prior to or coincident with the $\overline{\text{CE}}_1$ and CE_2^* transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{\text{CE}}_1$ and CE_2^* active and $\overline{\text{WE}}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{\text{WE}}$ goes low before or concurrent with the latter of $\overline{\text{CE}}_1$ and CE_2^* going active, the output remains in a high impedance state.

18. If $\overline{\text{CE}}_1$ and CE_2^* goes inactive before or concurrent with $\overline{\text{WE}}$ going high, the output remains in a high impedance state.

19. Powerup from ICC_2 to ICC_1 occurs as a result of any of the following conditions:

- Rising edge of CE_2^* ($\overline{\text{CE}}_1$ active) or the falling edge of $\overline{\text{CE}}_1$ (CE_2^* active).
- Falling edge of $\overline{\text{WE}}$ ($\overline{\text{CE}}_1$, CE_2^* active).
- Transition on any address line ($\overline{\text{CE}}_1$, CE_2^* active).
- Transition on any data line ($\overline{\text{CE}}_1$, CE_2^* , and $\overline{\text{WE}}$ active).
- Falling edge of $\overline{\text{CLEAR}}$.

The device automatically powers down from ICC_1 to ICC_3 after tPD has elapsed from any of the prior conditions. The exception is $\overline{\text{CLEAR}}$ where the device remains powered up for the duration of the Clear cycle. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

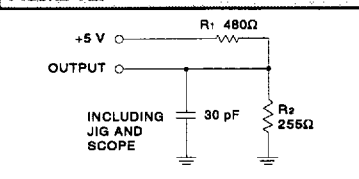
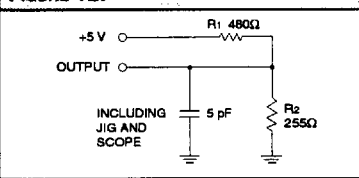
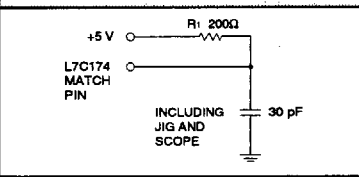
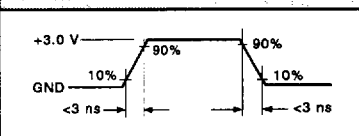
21. Transition is measured $\pm 200\text{ mV}$ from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

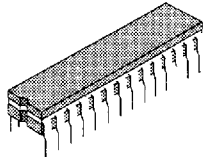
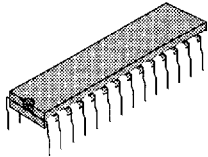
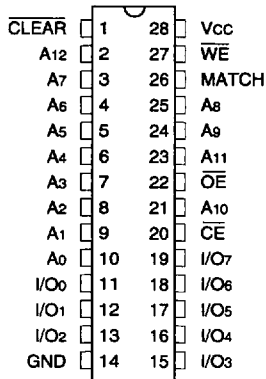
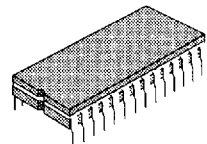
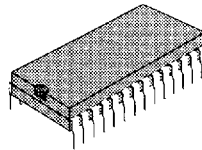
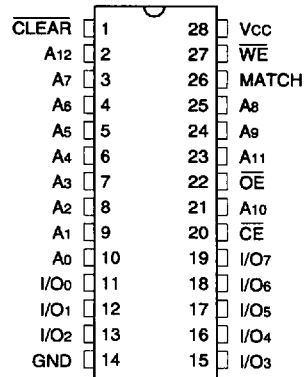
23. $\overline{\text{CE}}_1$, CE_2^* , or $\overline{\text{WE}}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A $0.01\text{ }\mu\text{F}$ high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

25. The Clear cycle is edge-triggered on the falling edge of $\overline{\text{CLEAR}}$. While the internal Clear cycle is in progress, all inputs, including multiple $\overline{\text{CLEAR}}$ pulses, are ignored. Inputs are recognized after tCLR has elapsed from the falling edge of $\overline{\text{CLEAR}}$. For proper operation, VCC must be within its specified normal operating voltage prior to assertion of $\overline{\text{CLEAR}}$.

FIGURE 1a.

FIGURE 1b.

FIGURE 1c.

FIGURE 2.


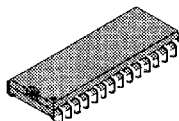
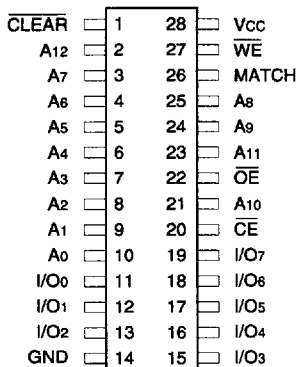
*If Applicable

ORDERING INFORMATION
28-pin — 0.3" wide

28-pin — 0.6" wide


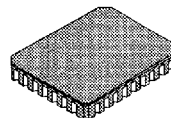
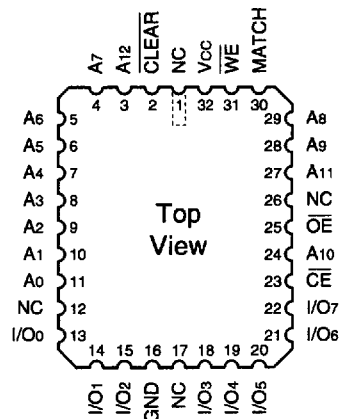
Speed	Plastic DIP (P10)	CerDIP (C5)	Plastic DIP (P9)	CerDIP (C6)
0°C to +70°C — COMMERCIAL SCREENING				
35 ns	L7C174PC35	L7C174CC35	L7C174NC35	L7C174IC35
25 ns	L7C174PC25	L7C174CC25	L7C174NC25	L7C174IC25
20 ns	L7C174PC20	L7C174CC20	L7C174NC20	L7C174IC20
15 ns	L7C174PC15	L7C174CC15	L7C174NC15	L7C174IC15
12 ns	L7C174PC12	L7C174CC12	L7C174NC12	L7C174IC12
-55°C to +125°C — COMMERCIAL SCREENING				
35 ns		L7C174CM35		L7C174IM35
25 ns		L7C174CM25		L7C174IM25
20 ns		L7C174CM20		L7C174IM20
15 ns		L7C174CM15		L7C174IM15
-55°C to +125°C — MIL-STD-883 COMPLIANT				
35 ns		L7C174CMB35		L7C174IMB35
25 ns		L7C174CMB25		L7C174IMB25
20 ns		L7C174CMB20		L7C174IMB20
15 ns		L7C174CMB15		L7C174IMB15

ORDERING INFORMATION

28-pin — 0.3" wide



32-pin — 0.450" x 0.550"



Speed	Plastic SOJ (W2)	Ceramic Leadless Chip Carrier (K7)
0°C to +70°C — COMMERCIAL SCREENING		
35 ns	L7C174WC35	L7C174KC35
25 ns	L7C174WC25	L7C174KC25
20 ns	L7C174WC20	L7C174KC20
15 ns	L7C174WC15	L7C174KC15
12 ns	L7C174WC12	L7C174KC12
-55°C to +125°C — COMMERCIAL SCREENING		
35 ns		L7C174KM35
25 ns		L7C174KM25
20 ns		L7C174KM20
15 ns		L7C174KM15
-55°C to +125°C — MIL-STD-883 COMPLIANT		
35 ns		L7C174KMB35
25 ns		L7C174KMB25
20 ns		L7C174KMB20
15 ns		L7C174KMB15