

T-46-23-08

P4C168/P4C168L, P4C169, P4C170 ULTRA HIGH SPEED 4K x 4 STATIC CMOS RAMS (SCRAMS)

2

FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
 - 12/15/20/25/30/35 ns (Commercial)
 - 20/25/30/35/45 ns (Military)
- Low Power Operation (Commercial/Military)
 - 550/660 mW Active
 - 193/220 mW Standby (TTL Input) P4C168
 - 83/110 mW Standby (CMOS Input) P4C168
 - 1.1/5.5 mW Standby (CMOS Input) P4C168L
- Single 5V±10% Power Supply
- Fully TTL Compatible, Common I/O Ports
- Three Options
 - P4C168/L Low Power Standby Mode
 - P4C169 Fast Chip Select Control
 - P4C170 Fast Chip Select, Output Enable Controls
- Data Retention with 2.0V Supply, .5 µA Typical Current
- Produced with PACE Technology™
- Standard Pinout (JEDEC Approved)
 - 20-Pin and 22-Pin (P4C170) 300 mil DIP
 - 20-Pin 300 mil SOIC (P4C168/L only)

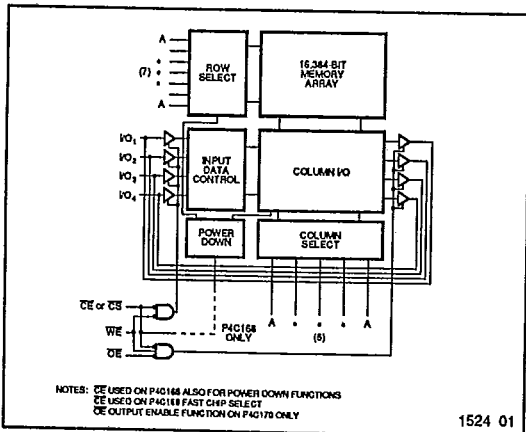
DESCRIPTION

The P4C168/L, P4C169 and P4C170 are a family of 16,384-bit ultra high speed static RAMs organized as 4K x 4. All three devices have common input/output ports. The P4C168/L enter the standby mode when the chip enable (\overline{CE}) control goes high; with CMOS input levels, power consumption is only 1.1 mW in this mode. Both the P4C169 and the P4C170 offer a fast chip select access time that is only 60% of the address access time. In addition, the P4C170 includes an output enable (\overline{OE}) control to eliminate data bus connection. The RAMs operate from a single 5V ± 10% tolerance power supply and retain data down to 2.0V.

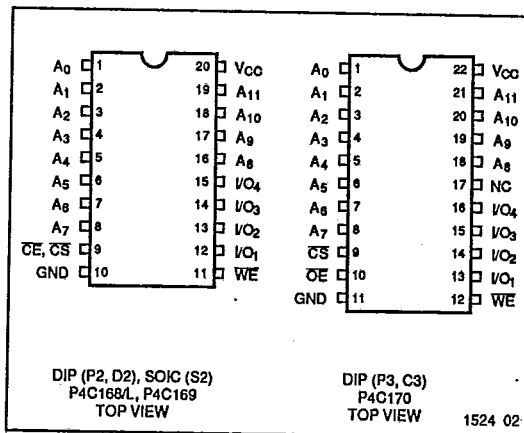
Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low 550 mW active, 193 mW standby. The P4C168/L, P4C169 and P4C170 are manufactured using PACE Technology™ and are members of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies.

The P4C168/L and P4C169 are available in 20-pin (P4C170 in 22-pin) 300 mil DIP packages providing excellent board level densities. The P4C168 is also available in 20-pin 300 mil SOIC packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V _{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to V _{CC} +0.5	V
T _A	Operating Temperature	-55 to +125	°C

1524 Tbl 01

Symbol	Parameter	Value	Unit
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	50	mA

1524 Tbl 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade ⁽²⁾	Ambient Temperature	GND	V _{CC}
Military	-55 to +125°C	0V	5.0V ± 10%

1524 Tbl 03

Grade ⁽²⁾	Ambient Temperature	GND	V _{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

1524 Tbl 04

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage⁽²⁾

Symbol	Parameter	Test Conditions	P4C168/169/170		P4C168L		Unit	
			Min	Max	Min	Max		
V _{IH}	Input High Voltage		2.2	V _{CC} +0.5	2.2	V _{CC} +0.5	V	
V _{IL}	Input Low Voltage		-0.5 ⁽³⁾	0.8	-0.5 ⁽³⁾	0.8	V	
V _{HC}	CMOS Input High Voltage		V _{CC} -0.2	V _{CC} +0.5	V _{CC} -0.2	V _{CC} +0.5	V	
V _{LC}	CMOS Input Low Voltage		-0.5 ⁽³⁾	0.2	-0.5 ⁽³⁾	0.2	V	
V _{CD}	Input Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-1.2		-1.2	V	
V _{OL}	Output Low Voltage (TTL Load)	I _{OL} = +10 mA, V _{CC} = Min. I _{OL} = +8 mA, V _{CC} = Min.		0.5 0.4		0.5 0.4	V	
V _{OLC}	Output Low Voltage (CMOS Load)	I _{OLC} = +100 µA, V _{CC} = Min.		0.2		0.2	V	
V _{OH}	Output High Voltage (TTL Load)	I _{OH} = -4 mA, V _{CC} = Min.	2.4		2.4		V	
V _{OHc}	Output High Voltage (CMOS Load)	I _{OHc} = -100 µA, V _{CC} = Min.	V _{CC} -0.2		V _{CC} -0.2		V	
I _{LI}	Input Leakage Current	V _{CC} = Max. V _{IN} = GND to V _{CC}	Mil. Com'l.	-10 -5	+10 +5	-5 -2	+5 +2	µA
I _{LO}	Output Leakage Current	V _{CC} = Max., CE = V _{IH} V _{OUT} = GND to V _{CC}	Mil. Com'l.	-10 -5	+10 +5	-5 -2	+5 +2	µA

1524 Tbl 05

CAPACITANCES⁽⁴⁾

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF

1524 Tbl 06

Symbol	Parameter	Conditions	Typ.	Unit
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	pF

1524 Tbl 07

Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IL} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20 ns.
- This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

T-46-23-08

Over recommended operating temperature and supply voltage⁽²⁾

Symbol	Parameter	Test Conditions	P4C168 P4C169 P4C170		P4C168L		Unit
			Min	Max	Min	Max	
I_{CC}	Dynamic Operating Current	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open	Mil. Com'l.	— 120 100	— — —	120 100	mA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}_1 \geq V_{IH}$ $V_{CC} = \text{Max.},$ $f = \text{Max.},$ Outputs Open	Mil. Com'l.	— 40 35	— — —	40 35	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}_1 \geq V_{HC}$ $V_{CC} = \text{Max.},$ $f = 0,$ Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	Mil. Com'l.	— 20 15	— — —	1 0.2	mA

n/a = Not Applicable

1524 Tbl 08

2

DATA RETENTION CHARACTERISTICS (P4C168L Only)

Symbol	Parameter	Test Condition	Min	Typ.* $V_{CC} =$		Max $V_{CC} =$		Unit
				2.0V	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	Mil. Com'l.		0.5 0.5	1.0 1.0	200 20	300 30	μA μA
t_{CDR}	Chip Deselect to Data Retention Time	$\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	0					ns
t_R^\dagger	Operation Recovery Time		t_{RC}^s					ns

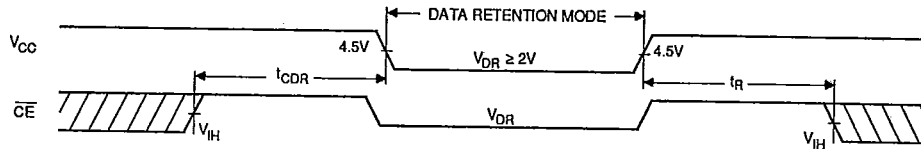
* $T_A = +25^\circ\text{C}$

1524 Tbl 09

^s t_{RC} = Read Cycle Time

[†]This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



1524 03



AC CHARACTERISTICS—READ CYCLE

T-46-23-08

(V_{CC} = 5V ± 10%, All Temperature Ranges)⁽²⁾

Sym	Parameter	-12*		-15*		-20		-25		-30		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{RC}	Read Cycle Time	12		15		20		25		30		35		45		ns
t _{AA}	Address Access Time		12		15		20		25		30		35		45	ns
t _{AC} [§]	Chip Enable Access Time		12		15		20		25		30		35		45	ns
t _{AC} [‡]	Chip Select Access Time		8		9		12		15		18		20		25	ns
t _{OH}	Output Hold from Address Change	2		3		3		3		3		3		3		ns
t _{LZ} [†]	Chip Enable to Output in Low Z	2		3		3		3		3		3		3		ns
t _{HZ} [†]	Chip Disable to Output in High Z		6		7		9		10		13		15		15	ns
t _{OE} [†]	Output Enable to Data Valid		8		10		12		15		15		15		15	ns
t _{OLZ} [†]	Output Enable to Output in Low Z	0		0		0		0		0		0		0		ns
t _{OHZ} [†]	Output Disable to Output in High Z		6		7		9		11		13		15		15	ns
t _{RCS}	Read Command Setup Time	0		0		0		0		0		0		0		ns
t _{RCH}	Read Command Hold Time	0		0		0		0		0		0		0		ns
t _{PU} [§]	Chip Enable to Power Up Time	0		0		0		0		0		0		0		ns
t _{PD} [§]	Chip Disable to Power Down Time		12		15		20		25		30		35		45	ns

1524 Tbl 10

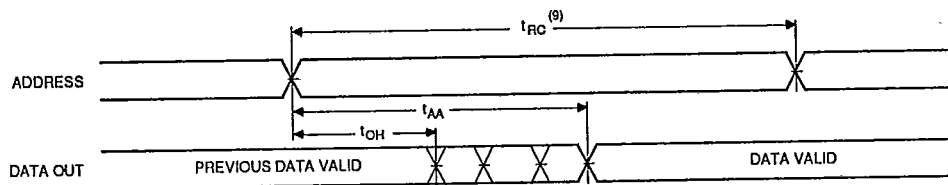
[§] P4C168 and P4C168L only

[†] P4C170 only

[‡] Chip Select/Deselect for P4C169 and P4C170

*V_{CC} = 5V ± 5% for -12, -15

TIMING WAVEFORM OF READ CYCLE NO. 1 (ADDRESS CONTROLLED)^(5,6)



1524 04

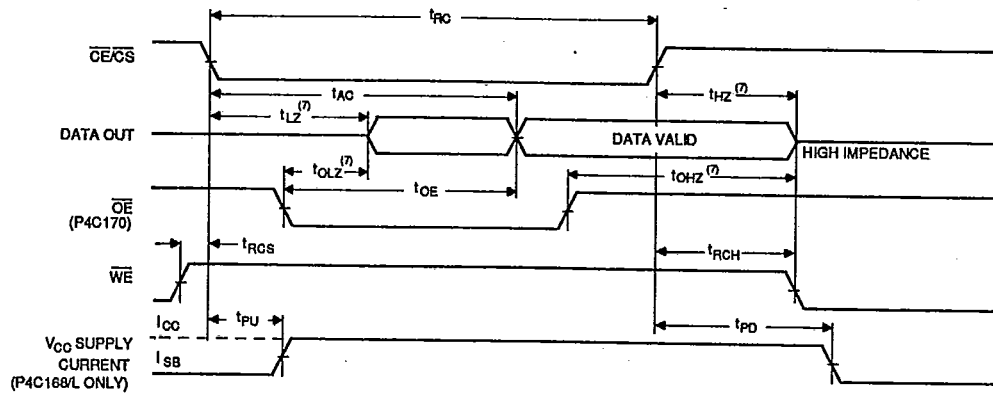
Notes:

5. WE is high for READ cycle.

6. CE/CS and OE are low for READ cycle.

TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{CE}/\overline{CS}$ CONTROLLED) ^(5,7)

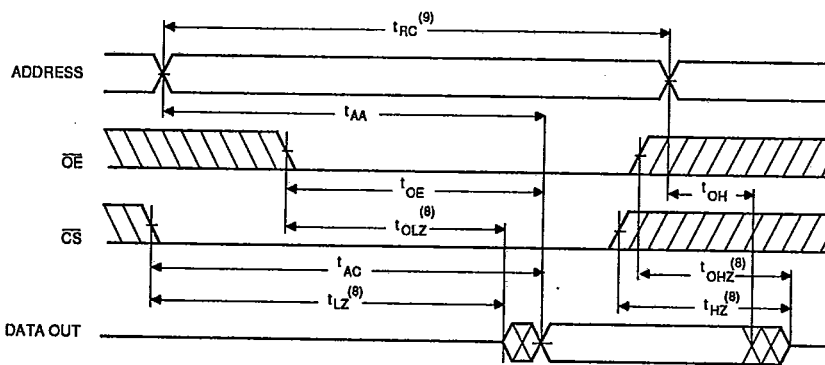
T-46-23-08



1524 05

2

TIMING WAVEFORM OF READ CYCLE NO. 3—P4C170 ONLY (\overline{OE} CONTROLLED) ⁽⁵⁾



1524 06

Notes:

- 7. ADDRESS must be valid prior to, or coincident with $\overline{CE}/\overline{CS}$ transition low. For Fast \overline{CS} , t_{AA} must still be met.
- 8. Transition is measured $\pm 200\text{mV}$ from steady state voltage prior to

- change, with loading as specified in Figure 1.
- 9. Read Cycle Time is measured from the last valid address to the first transitioning address.



T-46-23-08

AC ELECTRICAL CHARACTERISTICS—WRITE CYCLE

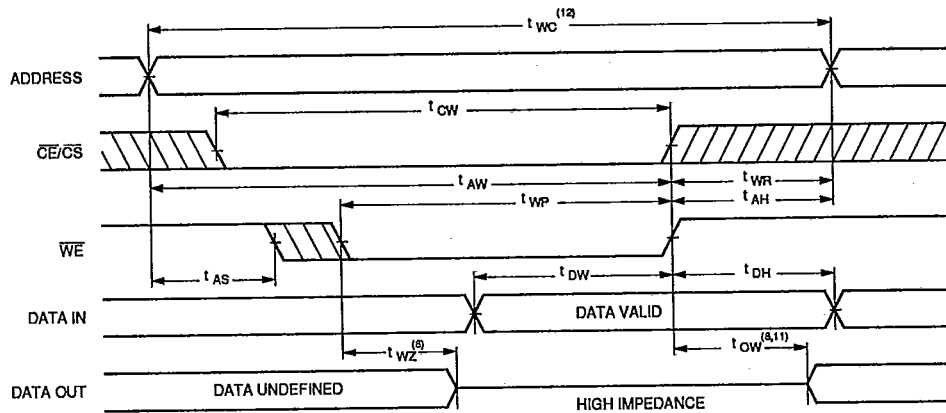
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Sym	Parameter	-12*		-15*		-20		-25		-30		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	12	15	15	18	20	20	25	30	30	30	40				ns
t_{CW}	Chip Enable Time to End of Write	12	15	15	18	20	20	25	30	30	30	35				ns
t_{AW}	Address Valid to End of Write	12	15	15	18	20	20	25	30	30	30	35				ns
t_{AS}	Address Set-up Time	0	0	0	0	0	0	0	0	0	0	0				ns
t_{WP}	Write Pulse Width	12	15	15	18	20	20	25	30	30	30	35				ns
t_{WR}	Write Recovery Time	0	0	0	0	0	0	0	0	0	0	0				ns
t_{AH}	Address Hold Time	0	0	0	0	0	0	0	0	0	0	0				ns
t_{DW}	Data Valid to End of Write	7	8	8	10	10	10	12	15	15	15	15				ns
t_{DH}	Data Hold Time	0	0	0	0	0	0	0	0	0	0	0				ns
t_{WZ}	Write Enable to Output in High Z	4	5	5	7	7	7	10	10	13	13	20				ns
t_{OW}	Output Active from End of Write	0	0	0	0	0	0	0	0	0	0	0				ns

* $V_{CC} = 5V \pm 5\%$ for -12, -15

1524 Tbl 11

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED)⁽¹⁰⁾



1524 07

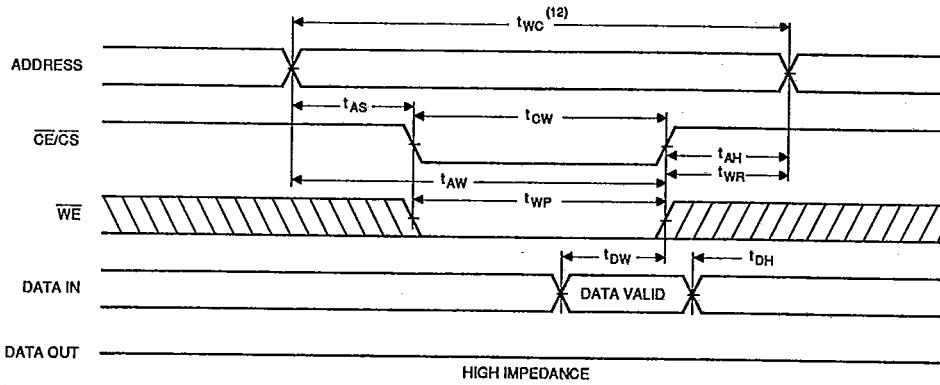
Notes:

- 10. $\overline{CE/CS}$ and \overline{WE} must be low for WRITE cycle.
- 11. If $\overline{CE/CS}$ goes high simultaneously with \overline{WE} high, the output remains in a high impedance state.

- 12. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CE/CS CONTROLLED) (10)

T-46-23-08



2

TRUTH TABLES

P4C168 (P4C169)

Mode	CE (CS)	WE	Output
Standby (Deselect)	H	X	High Z
Read	L	H	D _{OUT}
Write	L	L	High Z

1524 Tbl 12

AC TEST CONDITIONS

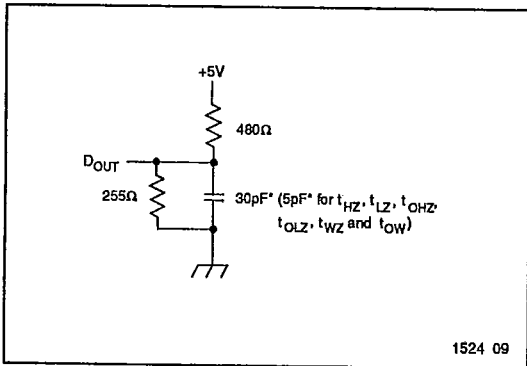
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

1524 Tbl 14

P4C170

Mode	CE	WE	OE	Output
Deselect	H	X	X	High Z
Read	L	H	L	D _{OUT}
Output Inhibit	L	H	H	High Z
Write	L	L	X	High Z

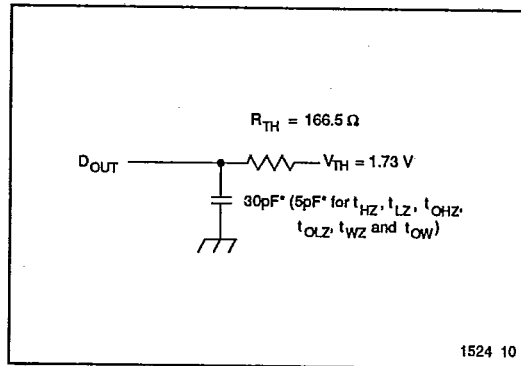
1524 Tbl 13



1524 09

Figure 1. Output Load

* including scope and test fixture.



1524 10

Figure 2. Thevenin Equivalent

Note:

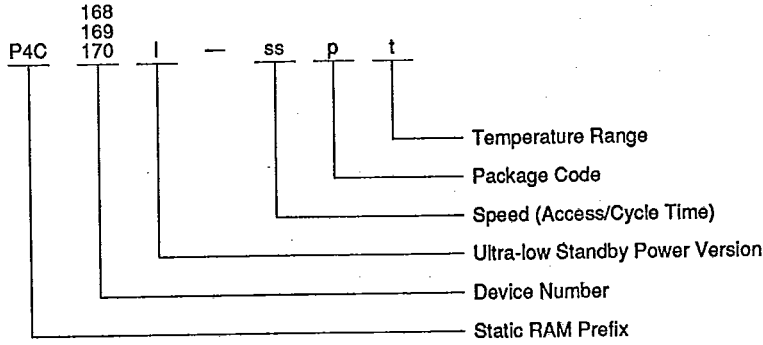
Due to the ultra-high speed of the P4C168/L, P4C169 AND P4C170 care must be taken when testing these devices; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between

V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).



T-46-23-08

ORDERING INFORMATION



- L = Ultra-low standby power designator L, if needed.
- ss = Speed (access/cycle time in ns), e.g., 15, 20
- p = Package code, i.e., P, S, D.
- t = Temperature range, i.e., C, M, MB.

1524 Tbl 11

PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
S	Plastic SOIC, 300 mil wide standard
D	CERDIP, 300 mil wide standard

1524 Tbl 15

TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C – +70°C.
M	Military Temperature Range, –55°C – +125°C.
MB	Mil. Temp. with MIL-STD-883C Class B compliance

1524 Tbl 16

SELECTION GUIDE

The P4C168/L, P4C169 and P4C170 are available in the following temperature, speed and package options.

Temperature Range	Package	Speed (ns)						
		12	15	20	25	30	35	45
Commercial	Plastic DIP	-12PC	-15PC	-20PC	-25PC	-30PC	-35PC	N/A
	Plastic SOIC†	-12SC	-15SC	-20SC	-25SC	-30SC	-35SC	N/A
	CERDIP	-12DC	-15DC	-20DC	-25DC	-30DC	-35DC	N/A
Military Temp.	CERDIP	N/A	N/A	-20DM	-25DM	-30DM	-35DM	-45DM
Military Processed*	CERDIP	N/A	N/A	-20DMB	-25DMB	-30DMB	-35DMB	-45DMB

1524 Tbl 17

† P4C168/L only
 * Military temperature range with MIL-STD-883 Revision C, Class B processing.
 N/A = Not available

Advance Information

TECHDOC 1524