P54/74PCT257A/B, P54/74PCT258A/B DATA SELECTOR/MULTIPLEXER

PRELIMINARY

T-67-21-51

FEATURES

- Quad 2-line to 1-line Data Selector Multiplexer
- Full CMOS Implementation
- Low Power Operation
- I_{OL} = 48 mA (Commercial) and 32 mA (Military)
- 3-State Outputs
- Fully TTL Compatible Input and Output levels
- Produced with PACE Technology™
- Compact Pinout—16-Pin 300 mil DIP, SOIC

DESCRIPTION

The P54/74PCT257A/B and P54/74PCT258A/B have four identical 2-input multiplexers with 3-state outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the select input is HIGH. Data appears at the output in true noninverted form for the P54/74PCT257A/B and in the inverted form for the P54/74PCT258A/B from the selected outputs.

The 'PCT257 and 'PCT258 are logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the select input.

Outputs are forced to a high-impedance "OFF" state when the Output Enable input ($\overline{OE}$) is HIGH.

All but one device must be in the High-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

The P54/74PCT257/258 is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded *internal gate delays.

Pace Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 enviroment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

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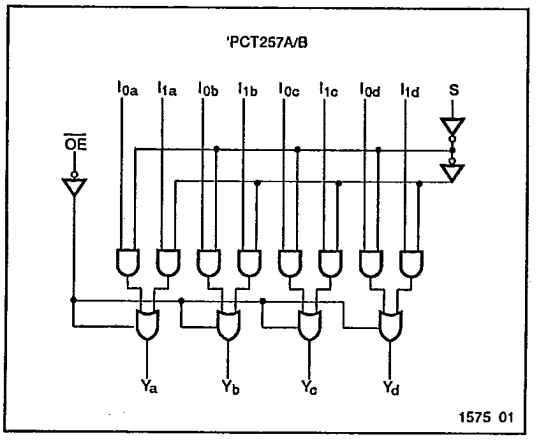
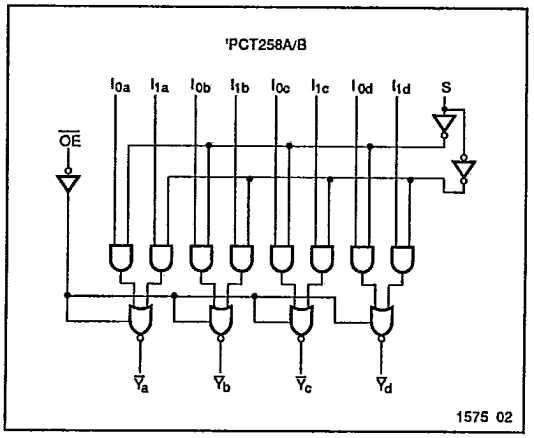
FUNCTIONAL BLOCK DIAGRAM





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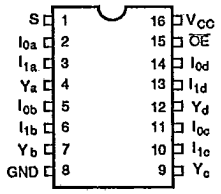
PIN CONFIGURATION

'PCT257A/B



DIP (P10, D10) SOIC (S10)

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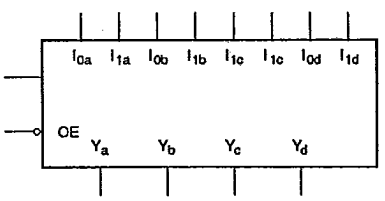
LOGIC DIAGRAM

'PCT257A/B



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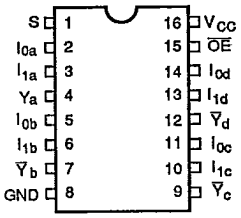
PIN CONFIGURATION

'PCT258A/B



DIP (P10, D10) SOIC (S10)

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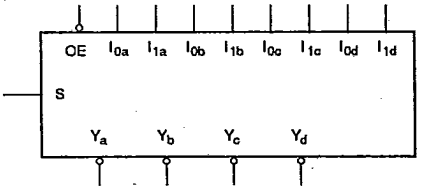
LOGIC DIAGRAM

'PCT258A/B



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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis			.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage				–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2			V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2			V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.7			V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V			0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)			0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)			0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)			0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied				10	µA	MAX	V_{OUT} = V_{CC}
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied				–10	µA	MAX	V_{OUT} = GND
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied[3]				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied[3]				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CCQC}	Quiescent Power Supply Current (CMOS inputs) Com'l	.003	0.3	mA	V_{CC} = MAX, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$, f = 0, Outputs Open
	Mil	.003	0.5	mA	
I_{CCQT}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$, Outputs Open
I_{CC}	Total Power Supply Current[5]		4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 5MHz, $\overline{OE}$ = GND and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
			6.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 5MHz, $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND
			7.8[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
			16.8[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQC} + I_{CCQT} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CCQC} = Quiescent Current with CMOS input levels
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLE

Inputs				Output	
$\overline{OE}$	S	I_0	I_1	Y	$\overline{Y}$
H	X	X	X	Z	Z
L	H	X	L	L	H
L	H	X	H	H	L
L	L	L	X	L	H
L	L	H	X	H	L

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H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance (OFF) state

DEFINITION OF FUNCTIONAL TERMS

Pins	Description
$I_{0n} - I_{1n}$	Data inputs
S	Common select input
$\overline{OE}$	Enable Input (Active-Low)
$Y_a - Y_d$	Data outputs

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AC CHARACTERISTICS

Sym.	Parameter	P54/74PCT257A P54/74PCT258A					P54/74PCT257B P54/74PCT258B					Units	Fig. No.
		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L			
		Typ.	Min.[1]	Max.	Min.[1]	Max.	Typ.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH}	Propagation Delay	4.5			3.0	7.0						ns	1
t_{PHL}	I_{na}, I_{nb} to Y_n 'PCT257	3.5			2.0	6.0						ns	3
t_{PLH}	Propagation Delay	7.5			5.0	10.5						ns	1
t_{PHL}	S to Y_n 'PCT257	5.5			4.0	8.0						ns	3
t_{PZH}	Output Enable time to	6.5			4.5	8.5						ns	1, 7,
t_{PZL}	High or Low 'PCT257	6.0			4.5	8.5						ns	8
t_{PHZ}	Output Disable time from	4.0			2.0	6.0						ns	1, 7,
t_{PLZ}	High or Low 'PCT257	3.5			2.0	6.0						ns	8
t_{PLH}	Propagation Delay	4.5			2.5	7.0						ns	1
t_{PHL}	I_n to $\overline{Y}_n$ 'PCT258	2.5			1.0	4.5						ns	2
t_{PLH}	Propagation Delay	6.5			3.5	9.0						ns	1
t_{PHL}	S_n to $\overline{Y}_n$ 'PCT258	6.0			2.5	9.0						ns	5
t_{PZH}	Output Enable time to	6.0			3.5	8.5						ns	1, 7,
t_{PZL}	High or Low 'PCT258	6.5			3.5	8.5						ns	8
t_{PHZ}	Output Disable time from	3.5			2.0	6.5						ns	1, 7,
t_{PLZ}	High or Low 'PCT258	3.5			2.0	6.0						ns	8

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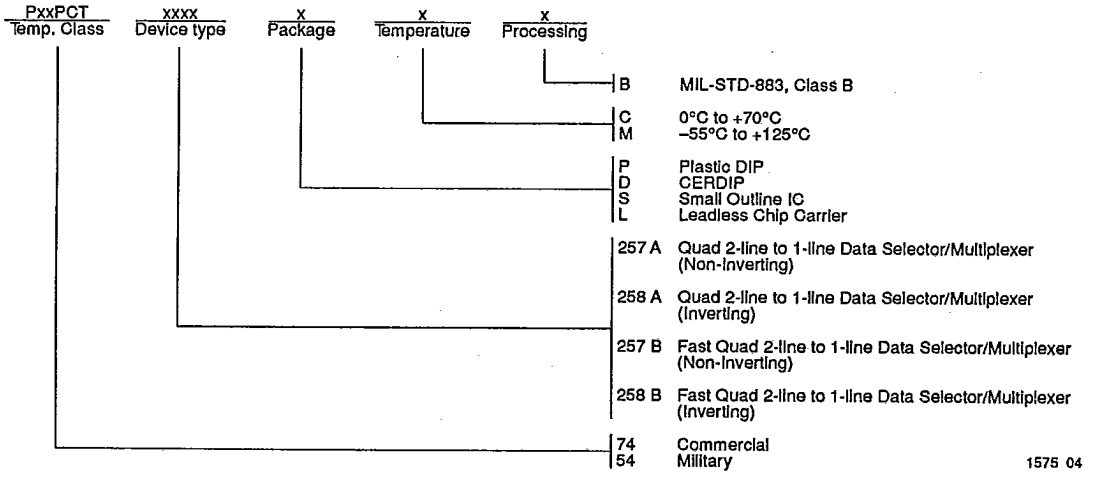
ORDERING INFORMATION



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