

Low-voltage single-chip 8-bit microcontroller

80CL32/80CL52

T-49-19-07

DESCRIPTION

The 80CL52 is manufactured in an advanced CMOS technology. The instruction set of the 80CL52 is based on that of the 8051. The 80CL52 is an 8-bit general purpose microcontroller especially suited for cordless telephone applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the 85CL781 (Piggy-back version) with 256 bytes of RAM is recommended. The 80CL52 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The 80CL52 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a single package
- 8K x 8 ROM, expandable externally to 64K bytes
- 256 bytes RAM, expandable externally to 64K bytes
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- External memory expandable up to 128K, external ROM
- up to 64K and/or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fourteen source, fourteen vector interrupt structure with two priority levels

- Full duplex serial UART
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight byte RAM register banks
  - stack depth limited only by available internal RAM (max. 256 bytes)
  - multiply, divide, subtract and compare instructions
- Power-down and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8 V to 6.0 V
- Frequency range of 32 kHz to 12 MHz
- Very low current consumption
- Operating temperature range: -40 to +85 °C

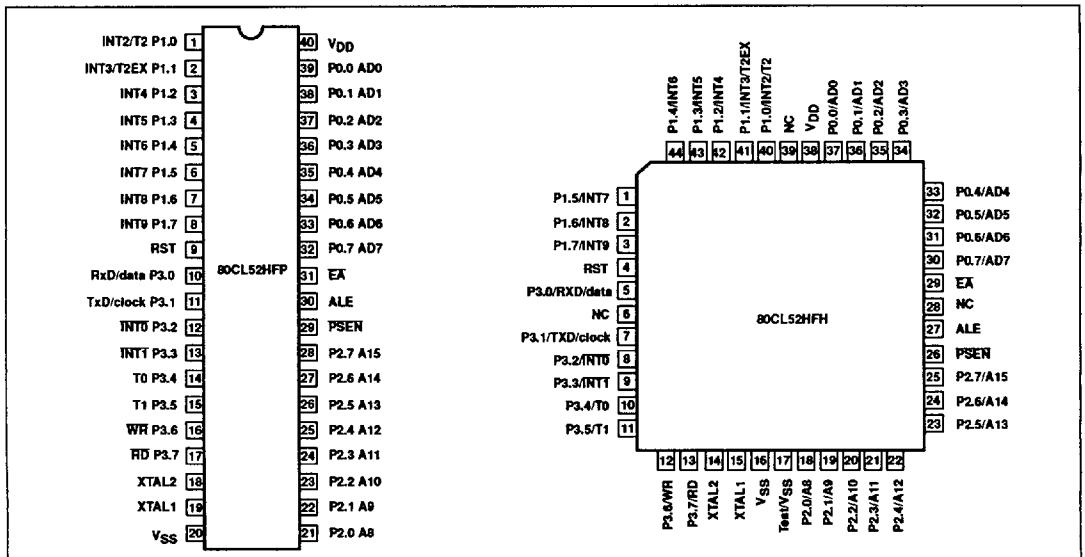
ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA <sup>3</sup> PART ORDER NUMBER		TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
ROMless	ROM	ROMless	ROM			
P80CL32HFP	P80CL52HFP	P80CL32HFP N	P80CL52HFP N	-40 to +85 40-Pin Plastic DIP <sup>1</sup>	32KHz to 12MHz	SOT129
P80CL32HFH	P80CL52HFH	P80CL32HFH B	P80CL52HFH B	-40 to +85 44-Pin Plastic QFP <sup>2</sup>	32KHz to 12MHz	SOT205

NOTES:

1. DIP = Dual In-line Package
2. QFP = Quad Flat Pack
3. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

PIN CONFIGURATIONS



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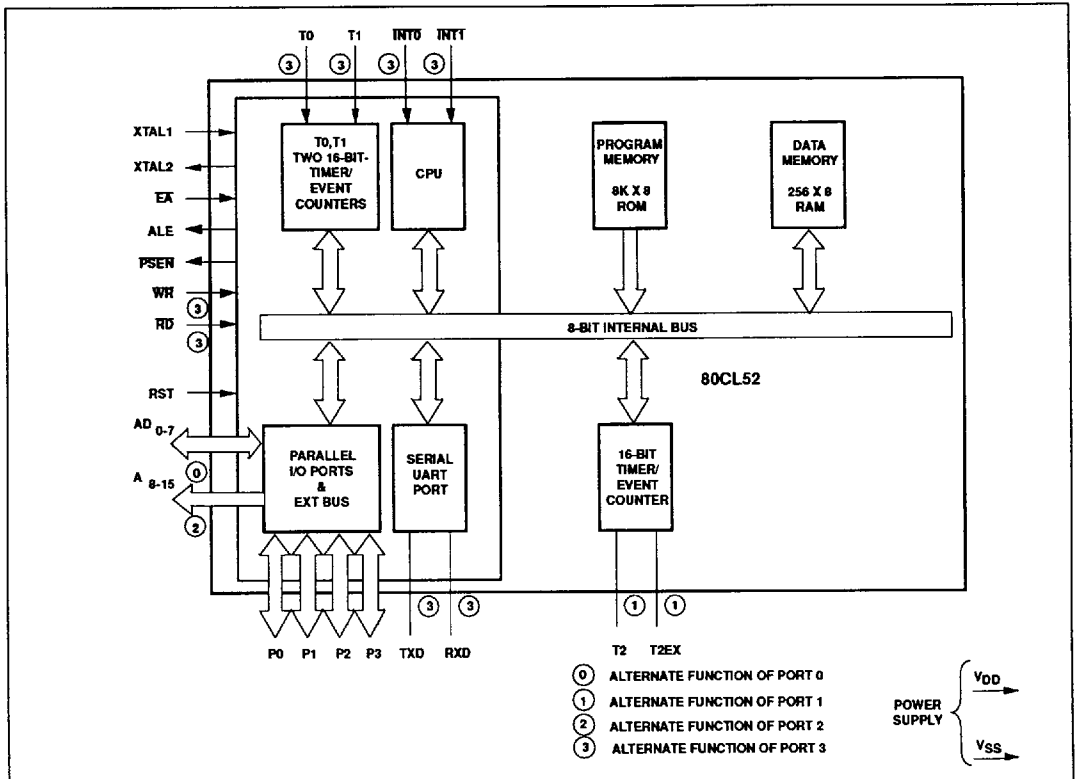
## PIN DESCRIPTIONS

PIN	DESIGNATION	FUNCTION
40 41 42 43 44 1 2 3	P1.0/INT2/T2 P1.1/INT3/T2EX P1.2/INT4 P1.3/INT5 P1.4/INT6 P1.5/INT7 P1.6/INT8 P1.7/INT9	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled HIGH by the internal pullups, and in that state can be used as inputs. The Port 1 output buffer can sink/source 4 LS TTL loads. As inputs, Port 1 pins that are externally pulled LOW will source current ( $I_{L}$ in the characteristics) due to the internal pullups. Port 1 also serves the alternative functions INT2 to INT9, and Timer T2 external input.
4	RST	<b>Reset:</b> A high level on this pin for two machine cycles while the oscillator is running resets the device.
5, 7-13	P3.0-P3.7	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled HIGH by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled LOW will source current ( $I_{L}$ in the characteristics) due to the internal pull-ups.
5	P3.0/RXD/data	<b>RXD/data:</b> serial port receiver data input (asynchronous) or data input/output (synchronous)
7	P3.1/TXD/clock	<b>TXD/clock:</b> serial port transmitter data output (asynchronous) or clock output (synchronous)
8	P3.2/INT0	<b>INT0:</b> External interrupt 0.
9	P3.3/INT1	<b>INT1:</b> External interrupt 1.
10	P3.4/T0	<b>T0:</b> Timer 0 external input.
11	P3.5/T1	<b>T1:</b> Timer 1 external input.
12	P3.6/WR	<b>WR:</b> External data memory write strobe.
13	P3.7/RD	<b>RD:</b> External data memory read strobe.
14	XTAL2	<b>Crystal output:</b> output of the inverting amplifier of the oscillator. Left open when external clock is used. <b>Crystal Input:</b> input to the inverting amplifier of the oscillator, also the input for an externally generated clock source.
15	XTAL1	<b>Crystal Input:</b> Input to the inverting amplifier of the oscillator; also the input for an externally generated clock source.
16	V <sub>SS</sub>	<b>Ground:</b> Circuit ground potential.
17	Test / V <sub>SS</sub>	<b>Test input:</b> must be connected to V <sub>SS</sub> or left open.
18-25	P2.0-P2.7	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled HIGH by the internal pullups, and in that state can be used as inputs. The Port 2 output buffer can sink/source 4 LS TTL loads. Port 2 emits the high-order address byte during accesses to external memory that use 16-bit addresses (MOVX @DPTR). In this application it uses the strong internal pullups when emitting 1s. During accesses to external memory that use 8-bit addresses (MOVX @Ri). Port 2 emits the contents of the P2 Special Function Register.
26	PSEN	<b>Program store enable output:</b> read strobe to external program memory. When executing code out of external program memory, PSEN is activated twice each machine cycle. However, during each access to external data memory two PSEN activations are skipped.
27	ALE	<b>Address Latch Enable:</b> output pulse for latching the low byte of the address during access to external memory. ALE is emitted at a constant rate of 1/6 of the oscillator frequency, and may be used for external timing or clocking purposes.
29	EA	<b>External Access:</b> When EA is held High the CPU executes out of internal program memory (unless the program counter exceeds 1FFFH). Holding EA LOW forces the CPU to execute out of external memory regardless of the value of the program counter.
30-37	P0.0-P0.7	<b>Port 0:</b> Port 0 is an 8-bit open drain bidirectional I/O port. As an open drain output port it can sink 8 LS TTL loads. Port 0 pins that have 1s written to them float, and in that state will function as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during access to external memory. In this application it uses strong internal pull-ups when emitting logic 1s. <b>Power supply</b>
38	V <sub>DD</sub>	<b>Power supply.</b>

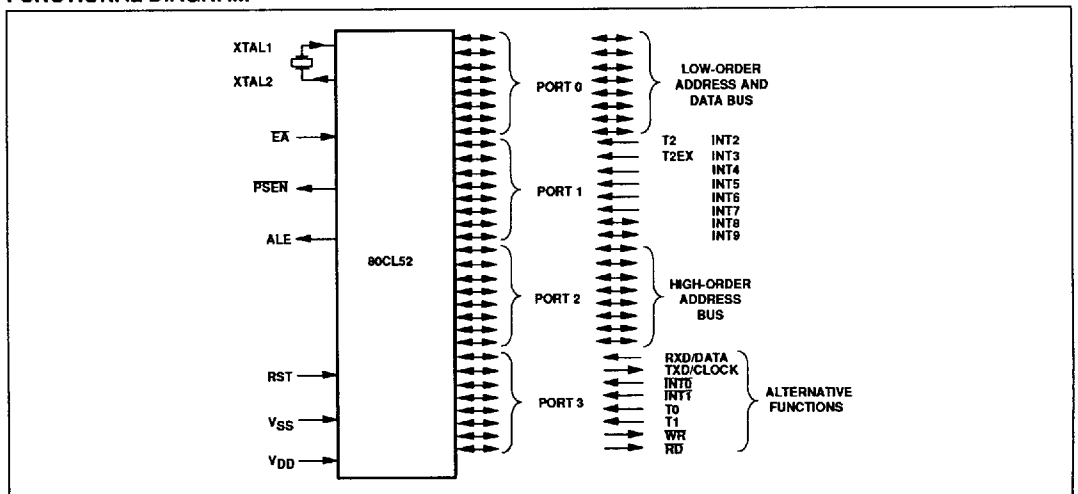
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BLOCK DIAGRAM



FUNCTIONAL DIAGRAM



## Low-voltage single-chip 8-bit microcontroller

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## 1.0 FUNCTIONAL DESCRIPTION

## General

The 80CL52 is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as instrumentation, industrial control, intelligent computer peripherals and consumer products.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

The 80CL52 contains a non-volatile 8K byte x 8 read-only program memory; a static 256 byte x 8 read/write data memory; 32 I/O lines; three 16-bit timer/event counters; a fourteen-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit.

The device has two software selectable modes of reduced activity for power reduction; IDLE and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial I/O and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

In addition, the device provides a standard UART serial interface.

## CPU timing

A machine cycle consists of a sequence of 6 states. Each state time lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1 ms if the oscillator frequency is 12 MHz.

**Note:** This datasheet covers only the special features of the 80CL52. For details on the 80CL52 core and the I<sup>2</sup>C-bus functions see the user manual:

## SINGLE-CHIP 8-BIT MICROCONTROLLER (USER MANUAL)

- The MAB8051/C51 microcontroller family.

## 1.1 Memory organization

The 80CL52 has a 8K Program Memory (ROM) plus 256 bytes of Data Memory (RAM) on board. The device has separate address spaces for Program and Data Memory (see Figure 1). Using Ports P0 and P2, the 80CL52 can address up to 64K bytes of external memory. The CPU generates both

read and write signals (RD and WR) for external Data Memory accesses, and the read strobe (PSEN) for external Program Memory.

## 1.1.1 Program Memory

The 80CL52 contains 8K bytes of internal ROM. After reset the CPU begins execution at location 0000H. The lower 8K bytes of Program Memory can be implemented in either on-chip ROM or external Memory. If the EA pin is strapped to V<sub>DD</sub>, then program memory fetches from addresses 000H through 1FFFH are directed to the internal ROM. Fetches from addresses 2000H through FFFFH are directed to external ROM. Program counter values greater than 1FFFH are automatically addressed to external memory regardless of the state of the EA pin.

**Please note that the first version of 80CL52 does not support automatic memory switching for addresses greater than 1FFFH. For customers using more than 8k byte memory it is recommended to work in external mode only. The automatic memory switching will be supported by a second version of 80CL52, becoming available in the 2nd half of 1993.**

## 1.1.2 Data Memory

The 80CL52 contains 256 bytes of internal RAM and 32 Special Function Registers (SFR). Figure 1 shows the internal Data Memory space divided into the Lower 128, the Upper 128, and the SFR space. Internal RAM locations 0-127 are directly and indirectly addressable. Internal RAM locations 128-255 are only indirectly addressable. The special function register locations 128-255 are only directly addressable.

## 1.1.3 Special Function Registers

The upper 128 bytes are the address locations of the SFRs. Figure 3 shows the Special Function Register (SFR) space. SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 bit addressable locations in the SFR address space (SFRs with addresses divisible by eight).

## 1.1.4 Addressing

The 80CL52 has five methods for addressing source operands:

- Register

- Direct
- Register-Indirect
- Immediate
- Base-Register-plus Index-Register-indirect

The first three methods can be used for addressing destination operands. Most instructions have a "destination/source" field that specifies data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four register banks through register, direct or indirect.
- Internal RAM (256 bytes) through direct or register indirect.
- Special Function Register through Direct.
- External data memory through Register-Indirect
- Program memory look-up tables through Base-Register-plus index-Register-indirect.

## 1.2 I/O Facilities

## 1.2.1 Ports

The 80CL52 has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit addressable ports. Port 0, 1, 2 and 3 perform the following alternate functions:

- Port 0: provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.
- Port 1:
  - (1) provides the inputs for the external interrupts INT2 / INT9.
  - (2) External counter/capture of Timer 2
- Port 2: provides the high-order address when expanding the device with external program
- Port 3: pins can be configured individually to provide:
  - (1) external interrupt request inputs
  - (2) counter input
  - (3) control signals to read and write to external memories
  - (4) UART input and output

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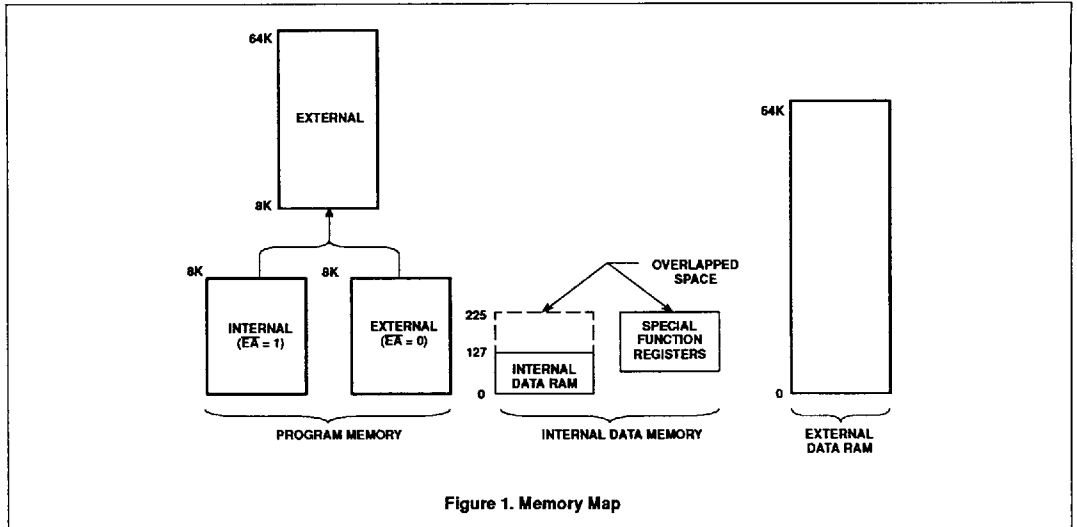


Figure 1. Memory Map

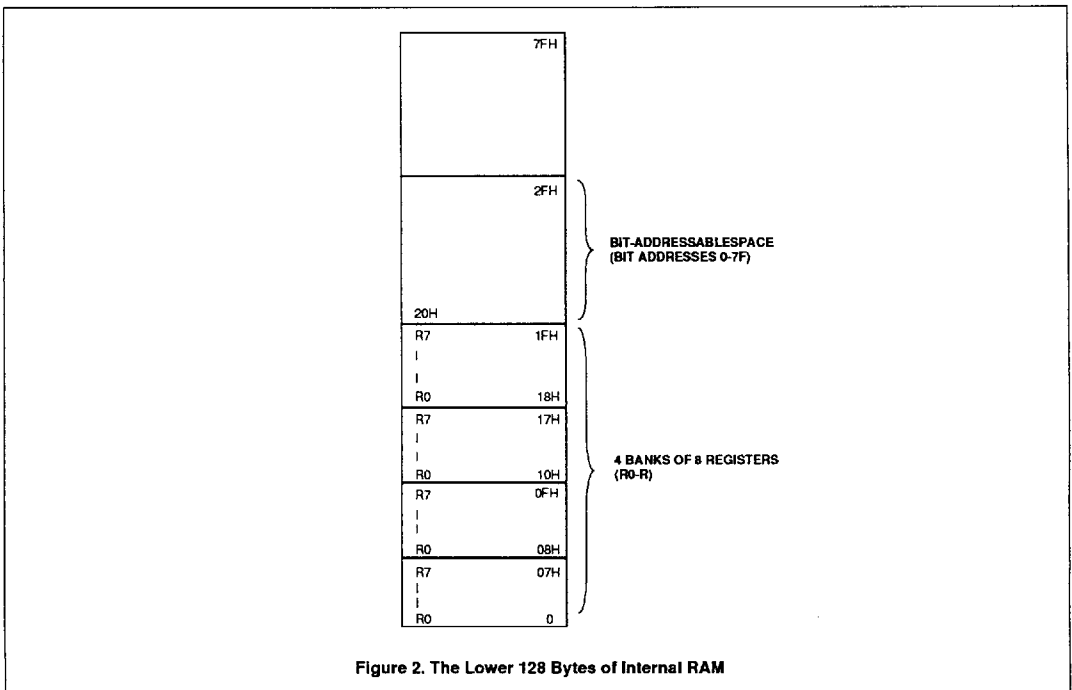


Figure 2. The Lower 128 Bytes of Internal RAM

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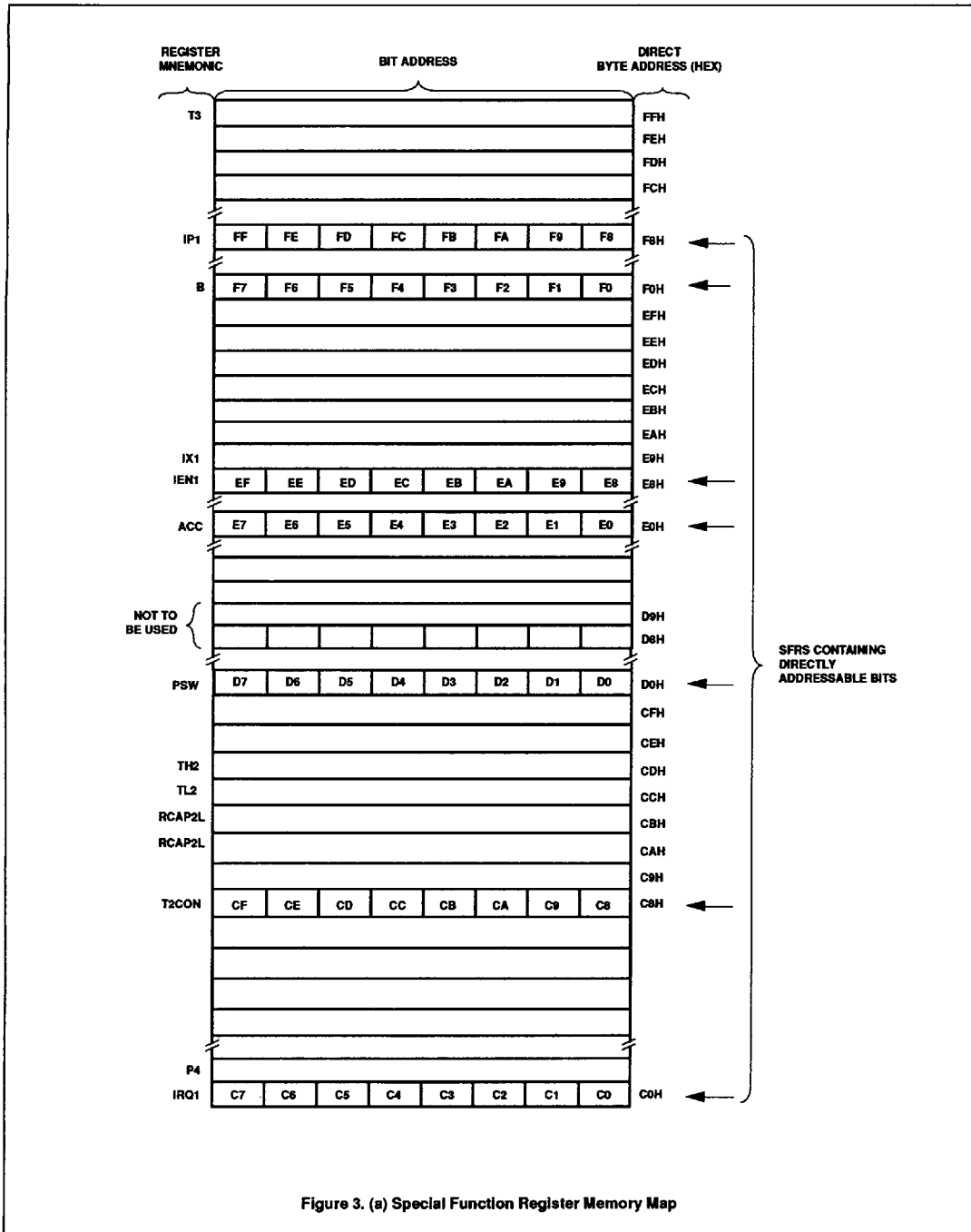


Figure 3. (a) Special Function Register Memory Map

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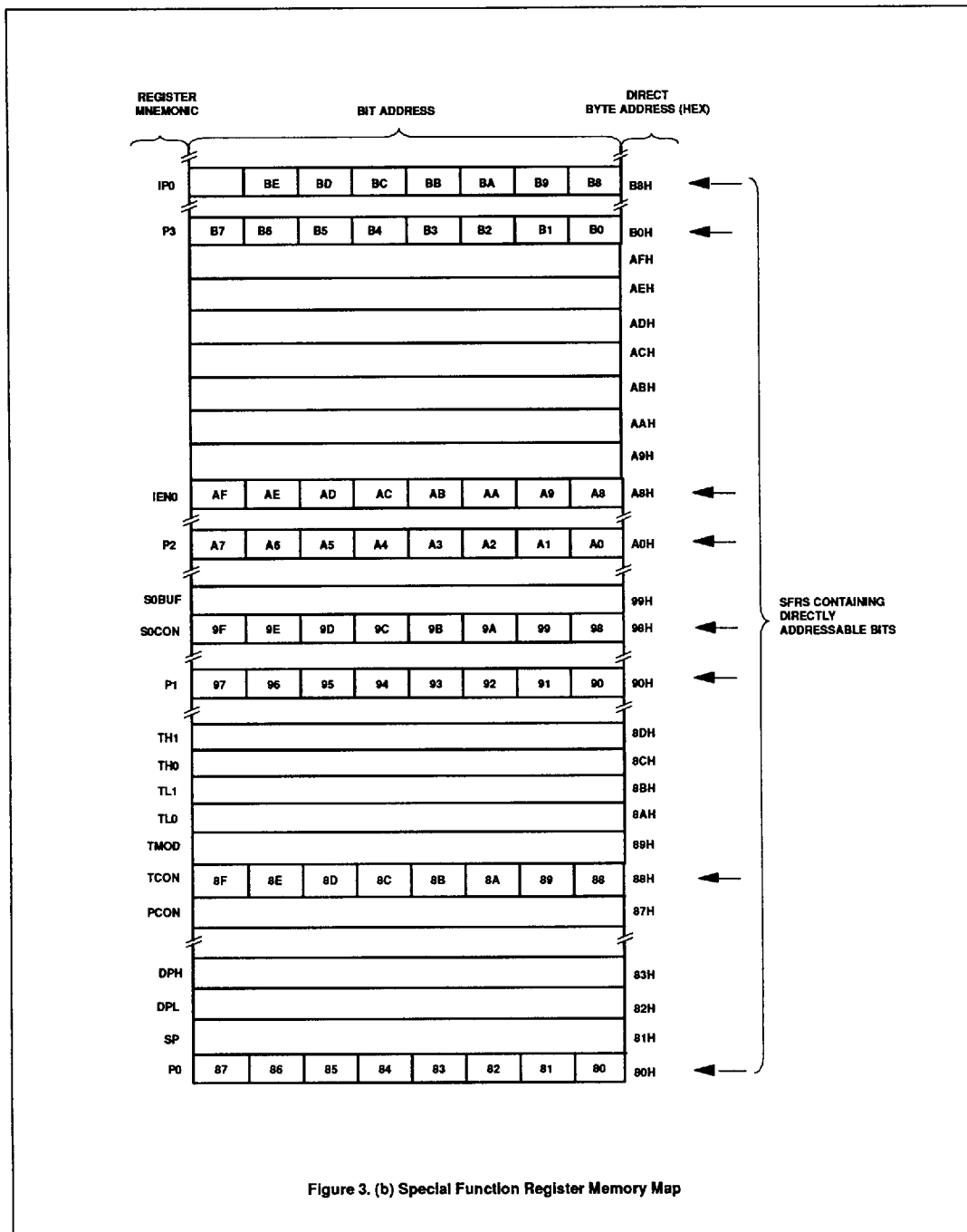


Figure 3. (b) Special Function Register Memory Map

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0To enable a Port 3 pin alternate function, the Port 3 bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and an input buffer. Ports 1,2,3 have internal pull-ups. Figure 4(a) shows that the strong transistor p1 is turned on for only 2 oscillator periods after a 0-to-1 transition in the port latch. When on, it turns on p3 (a weak pull-up) through the inverter. This inverter and p3 form a latch which hold the 1. In Port 0 the pull-up p1 is only on when emitting 1s for external memory access. Writing a 1 to a Port 0 bit latch leaves both output transistors switched off so the pin can be used as a high-impedance input.

### 1.2.2 Port Options

Thirty of the 32 parallel port pins may be individually configured with one of the following options (see Figure 4). Please note

that the options of port P1.6/P1.7 are fixed to 2S (open drain) on the first version of 80CL52. A second version of 80CL52 will become available in the 2nd half of 1993, where all options can be chosen for port P1.6/P1.7.

**Option 1: Standard Port;** quasi-bidirectional I/O with pull-up. The strong booster pull-up p1 is turned on for two oscillator periods after a 0-to-1 transition in the port latch (see Figure 4(a)).

**Option 2: Open drain;** quasi-bidirectional I/O with n-channel open drain output. Use as an output requires the connection of an external pull-up resistor (see Figure 4(c)). This option does not include the internal protection diode against  $V_{DD}$  for port P1.6 and P1.7.

**Option 3: Push-Pull;** output with drive capability in both polarities. Under this option, pins can only be used as outputs (see Figure 4(b)).

The definition of port options for port 0 is slightly different. Two cases have to be examined. First, accesses to external memory (EA=0 or access above the built-in memory boundary), second, I/O accesses.

#### External Memory Accesses

**Option 1:** True 0 and 1 are written as address to the external memory (strong pull-up is used).

**Option 2:** An external pull-up resistor is needed for external accesses.

**Option 3:** Not allowed for external memory accesses as the port can only be used as output.

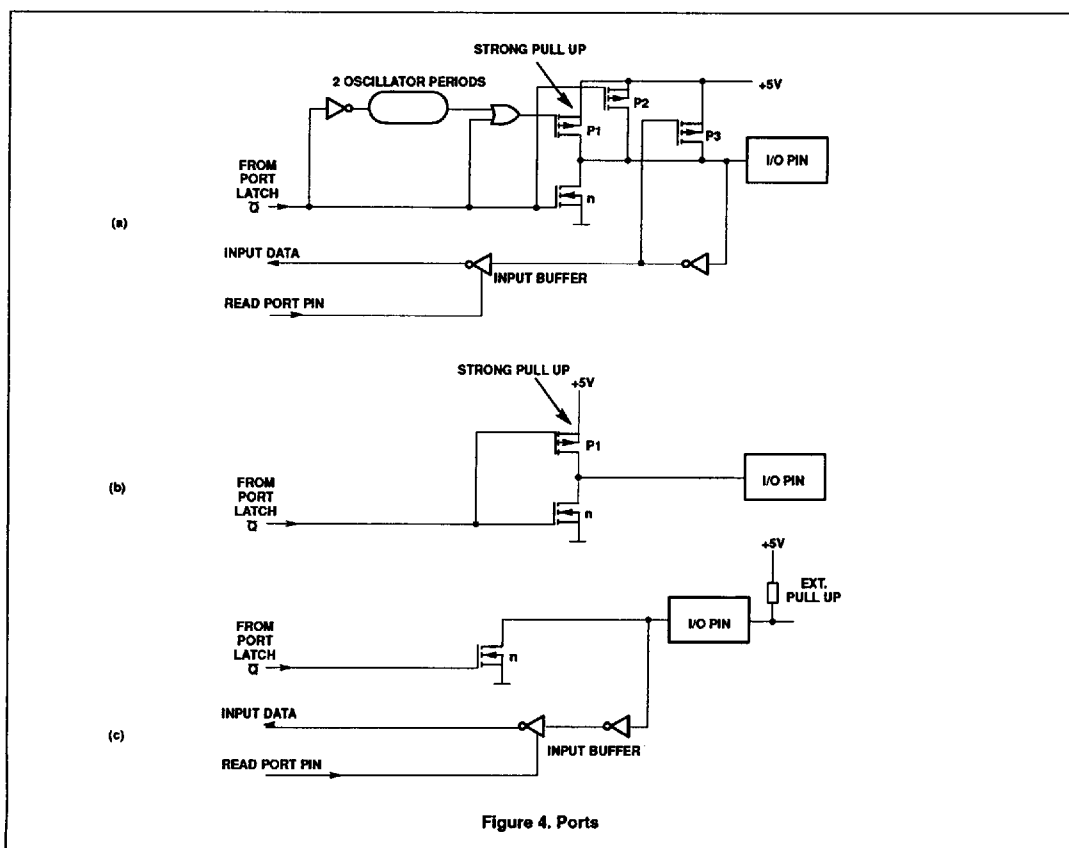


Figure 4. Ports

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**I/O Accesses:**

**Option 1:** When writing a 1 to the port-latch, the strong pull-up p1 will be on for 2 oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

**Option 2:** Open drain; quasi-bidirectional I/O with n-channel open drain output. Use as an output requires the connection of an external pull-up resistor (see Figure 4(c)).

**Option 3:** Push-Pull; output with drive capability in both polarities. Under this option, pins can only be used as outputs.

**Option S:** SET; after reset this pin will be initialized HIGH.

**Option R:** RESET; after reset this pin will be initialized LOW.

**1.3 Timer/event counter**

The 80CL52 contains three 16-bit Timer/Counter registers; Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupts requests

Timer 0 and Timer 1 can be independently programmed to operate as follows:

- Mode 0; 8-bit timer or counter with divide-by-32 prescaler
- Mode 1; 16-bit time-interval or event counter
- Mode 2; 8-bit time interval or event counter with automatic reload upon overflow
- Mode 3; Timer 0 establishes TLO and TH0 as two separate counters.

In the "Timer" function, the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the "Counter" function, the register is incremented in response to a 1-to-0 transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure a given level is sampled, it should be held for at least one full machine cycle.

**1.3.1 Timer 2**

Timer 2 is a 16-bit Timer/Counter. Like Timers 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/T2

in the Special Function Register T2CON (Figure 5). It has three operating modes: "capture", "auto-load" and "baud rate generator", which are selected by bits in T2CON as shown in Table 1.

**Table 1 Timer 2 Operating Modes**

RTCLK	CP/RLS	TR2	Mode
0	0	1	16-bit Auto-Reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(off)

In the Capture Mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2=1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. The Capture Mode is illustrated in Figure 6.

In the auto-reload mode there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2=0, then when Timer 2 rolls over it not only set TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2=1, the Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2.

The auto-reload mode is illustrated in Figure 7.

The baud rate generator mode is selected by RTCLK=1. It will be described in conjunction with the serial port.

Conversion already in progress is aborted when the Power-down mode is entered. The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the Idle mode.

**1.4 Idle and Power-down operation**

Idle mode operation permits the interrupt, serial ports, timer blocks continue functioning while the clock to the CPU is halted.

The following functions remain active during Idle mode. These functions may generate an interrupt or reset and thus end the Idle mode.

- Timer 0, Timer 1, Timer 2
- SIO
- External interrupt

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register.

**1.4.1 Power control register (PCON)**

These special modes are activated by software via the Special Function Register PCON. Its hardware address is 87H. [PCON is not bit addressable.]

	7	6	5	4	3	2	1	0
EA	-	ES1	ES0	ET1	EX1	ET0	EX0	

Bit	Symbol	Function
PCON.7	SMOD	Double Baud rate bit. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2, or 3.
PCON.6		(reserved)
PCON.5		(reserved)
PCON.4		(reserved)
PCON.3	GF1	General-purpose flag bit
PCON.2	GF0	General-purpose flag bit
PCON.1	PD	Power-down bit. Setting this bit activates Power-down mode.
PCON.0	IDL	Idle mode bit. Setting this bit activates the Idle mode

If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XX00000).

**1.4.2 Power-down mode**

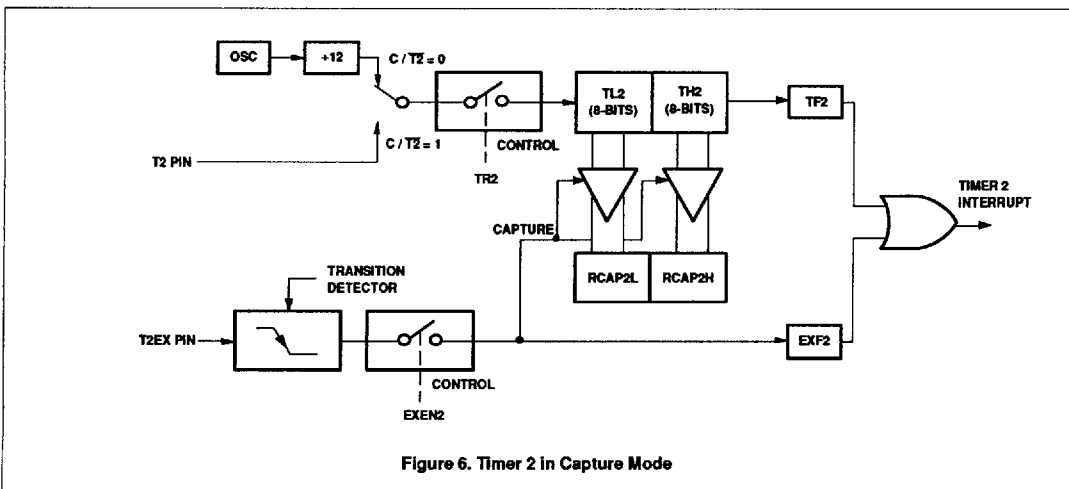
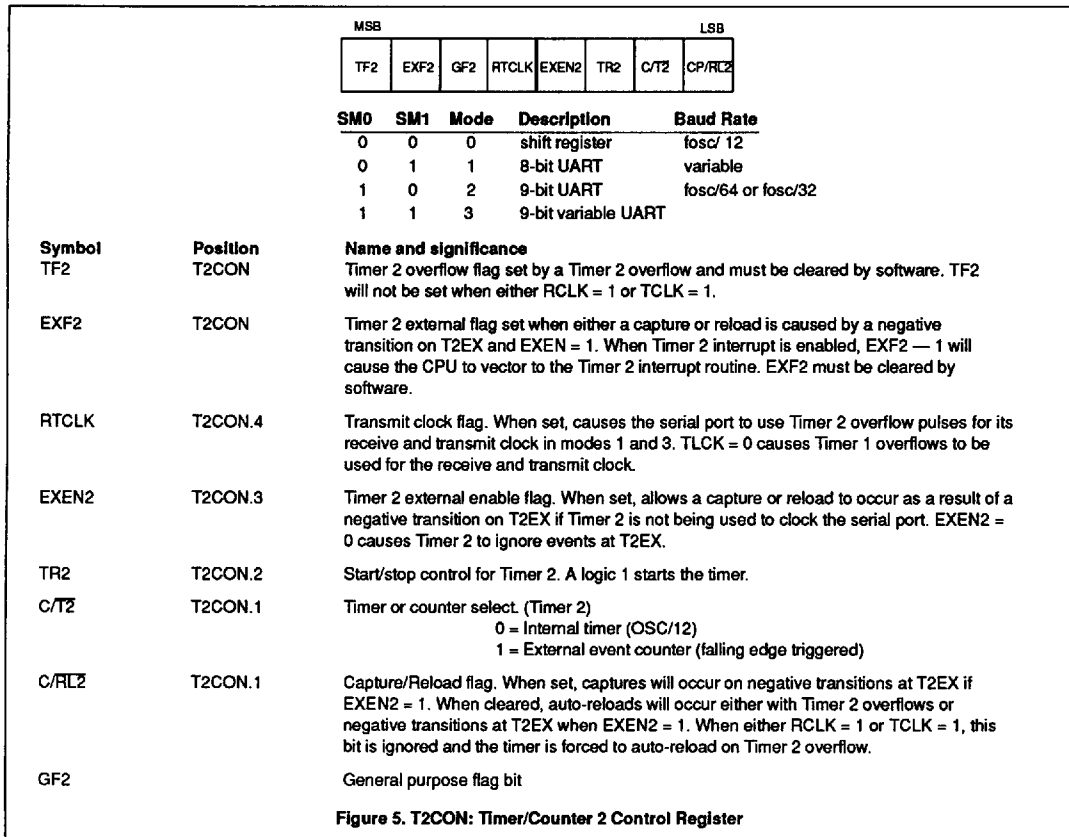
The instruction setting PCON.1 is the last executed prior to going into the Power-down mode. In Power-down mode the oscillator is stopped. The contents of the on-chip RAM and SFRs are preserved. The port pins output the values held by their respective SFRs. ALE and PSEN are held LOW.

**1.4.3 Wake-up mode**

Setting the PD flag in the PCON register forces the controller into the Power-down mode. Setting this flag enables the controller to be woken-up from the Power-down mode with either the external interrupts INT2 / INT9, or a reset operation.

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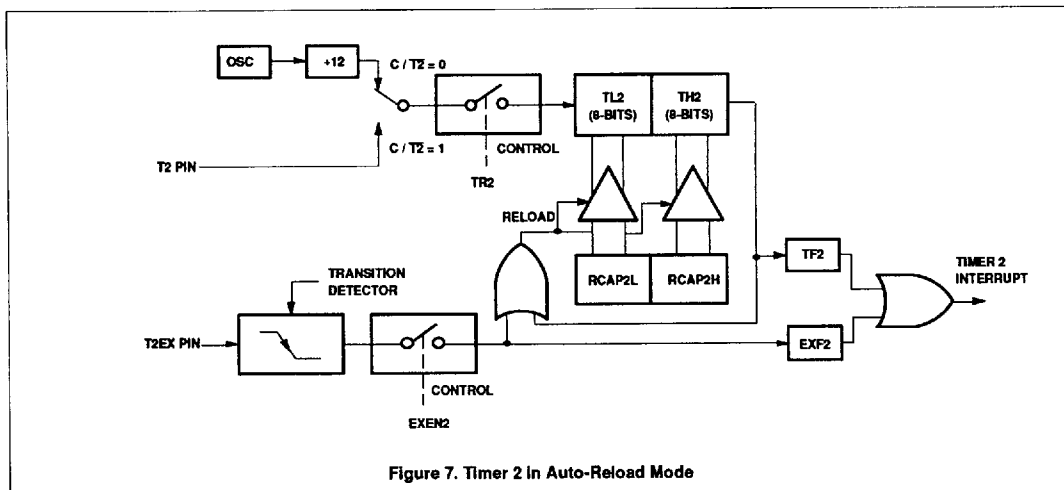


Figure 7. Timer 2 In Auto-Reload Mode

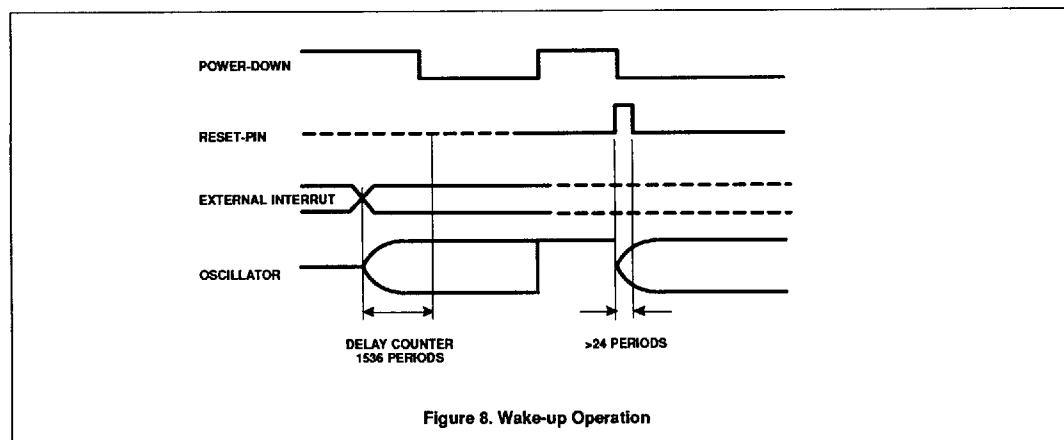


Figure 8. Wake-up Operation

The wake-up operation after power-down in this controller has two basic approaches:

**1.4.3.1 Wake-up using INT2 / INT9**

If INT2 to INT9 are enabled, the 80CL52 can be woken-up from power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

**1.4.3.2 Wake-up using RESET**

To wake-up the 80CL52 the RESET pin has to be kept HIGH for a minimum of 24 periods. The on-chip delay counter is inactive. The user has to ensure that the oscillator is stable

before any operation is attempted. Figure 8 illustrates the two possibilities for wake-up.

**1.4.4 Idle mode**

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 1.

There are two methods used to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following the return-from-interrupt instruction RETI, the next instruction to be executed will be the one which follows the instruction that wrote a logic 1 to PCON.0.

Flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during Idle mode. For example, the instruction that writes to

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PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.

The second method of terminating the Idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation.

Reset redefines all SFRs, but does not affect the on-chip RAM.

In the Power-down mode,  $V_{DD}$  may be reduced to minimize power consumption. However, the supply voltage must not be reduced until Power-down mode is active, and must be held active until the oscillator has restarted and stabilized.

The status of the external pins during Idle and Power-down mode is shown in Table 2. If the Power-down mode is activated whilst accessing external memory, port data held in the Special Function Register P2 is restored to Port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1 (see Figure 4(a)).

### 1.5 Standard serial interface SIO0: UART

This serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed at Special Function Register S0BUF. Writing to S0BUF loads the transmit register, and reading S0BUF loads the transmit register, and reading SOBIF accesses a physically separate receive register.

The serial port can operate in 4 modes:

**Mode 0:** Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud is fixed at 1/12 the oscillator frequency.

**Mode 1:** 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SC0N. The baud rate is variable.

**Mode 2:** 11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SC0N) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SC0N, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

**Mode 3:** 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

#### 1.5.1 Multiprocessor communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SC0N. A way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave

will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

#### 1.5.2 Serial port control register

The serial port control and status register is the Special Function Register S0CON, shown in Figure 9. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

#### Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = Oscillator Frequency / 12. The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is the value on reset), the baud rate is 1/64 the oscillator frequency. If SMOD = 1, the baud rate is 1/32 the oscillator frequency.

Mode 2 Baud Rate =  $(2^{SMOD} / 64) \times (\text{Oscillator Frequency})$

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

#### Using Timer 1 to generate baud rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

Modes 1,3 Baud Rate =  $(2^{SMOD} / 32) \times (\text{Timer 1 Overflow Rate})$

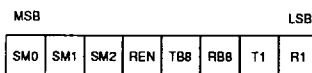
The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case the baud rate is given by the formula:

Table 2. Status of the External Pins During Idle and Power-down Mode

MODE	MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle (1)	internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle (1)	external	1	1	Floating	Port Data	Address	Port Data
Power-down	internal	0	0	Port Data	Port Data	Port Data	Port Data
Power-down	external	0	0	Floating	Port Data	Port Data	Port Data

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Where SM0, SM1 specify the serial port mode, as follows:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	shift register	fosc/ 12
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	fosc/64 or fosc/32
1	1	3	9-bit variable UART	

**- SM2**

Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2=1 then R1 will not be activated if a valid stopbit was not received. In Mode 0, SM2 should be 0.

**-REN**

Enables serial reception. Set by software to enable reception. Clear by software to disable reception.

**-TB8**

Is the 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.

**-RB8**

In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, if SM2=0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.

**-TI**

Is transmit interrupt flag. Set by hardware at the end of the 8th time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.

**-RI**

Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception except (see SM2). Must be cleared by software.

Figure 9. Serial Port control (SCON) Register

Mode 1, 3 Baud Rate =  $\{(2^{SMOD} / 32) \times$   
(Oscillator Frequency) /  $\{12 \times (256 - (TH1))\}$

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload. Table 2 lists various commonly used baud rates and how they can be obtained from Timer 1.

**Using Timer 2 to generate baud rates**

Timer 2 is selected as the baud rate generator by setting RTCLK in T2CON (Figure 10). Setting RTCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 10.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

Now, the baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as follows:

Modes 1,3 Baud Rate = (Timer 2 Overflow Rate) / 16

The Timer can be configured for either "timer" or "counter" operation. In the most typical applications, it is configured for "timer" operation (C/T2 = 0). "Timer" operation is a little different for Timer 2 when it's being used as a baud rate generator. Normally, as a timer is would increment every machine cycle (thus at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (thus at 1/2 the oscillator frequency). In that case the baud rate is given by the formula.

Modes 1,3 Baud Rate = (Oscillator Frequency) /  $\{32 \times (65536 - (RCAP2H, RCAP2L))\}$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 10. This Figure is valid only if RTCLK =

1 in T2CON. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Therefore, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt, if desired.

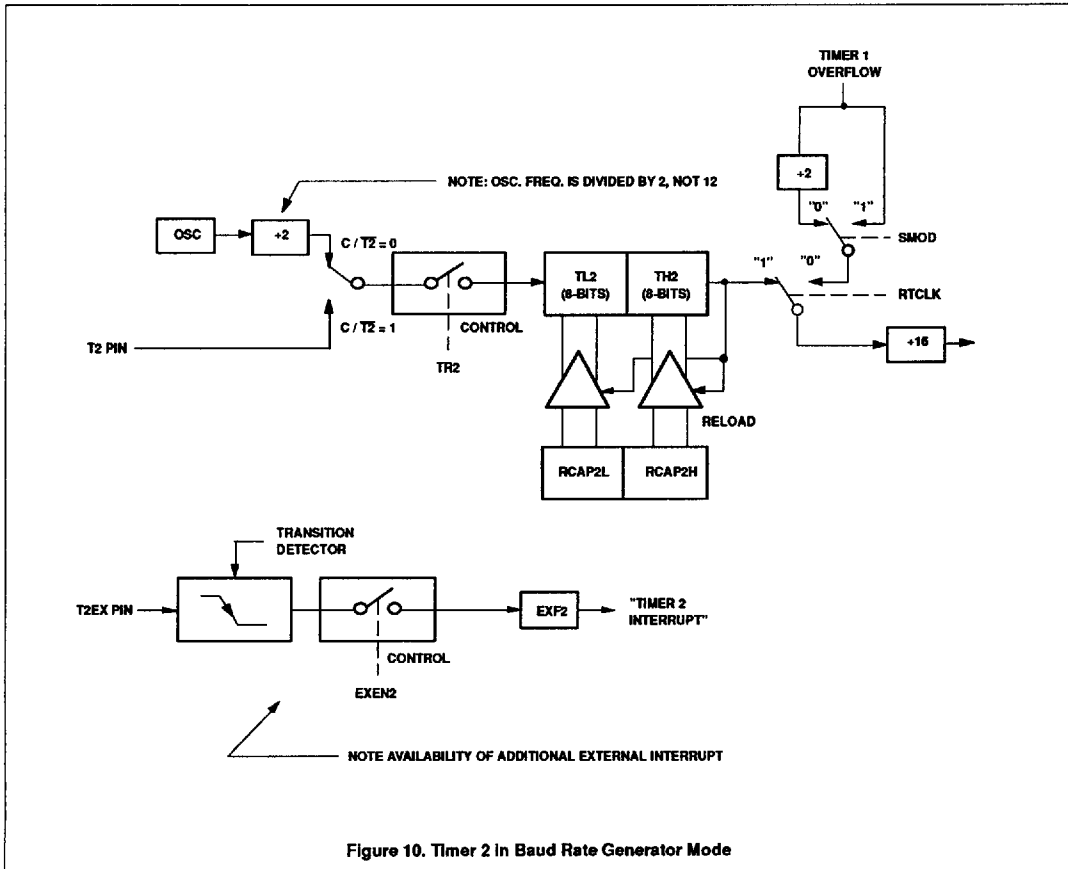
It should be noted that when Timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. Under these conditions the Timer is being incremented every state time, and the results of a read or write may not be accurate. The RCAP registers may be read, but shouldn't be written to, because a write might overlap a reload and cause write and/or reload errors. Turn the Timer off (clear TR2) before accessing the Timer 2 or RCAP register, in this case.

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Table 3. Timer 1 Generated Commonly Used Baud Rates

TIMER 1					
BAUD RATE	f <sub>osc</sub>	SMOD	C/T	MODE	RELOAD VALUE
Mode 0 Max: 1 MHz	12 MHz	x	x	x	x
Mode 2 Max: 375 K	12 MHz	1	x	x	x
Modes 1,3: 62.5 K	12 MHz	1	0	2	FFH
19.2 K	11.059 MHz	1	0	2	FDH
9.6 K	11.059 MHz	0	0	2	FDH
4.8 K	11.059 MHz	0	0	2	FAH
2.4 K	11.059 MHz	0	0	2	F4H
1.2 K	11.059 MHz	0	0	2	E8H
137.5 K	11.986 MHz	0	0	2	1DH
110	6 MHz	0	0	2	72H
110	12 MHz	0	0	1	FE6BH



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1.6 Interrupt system

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a multiple-source, two-priority-level, nested interrupt system is provided. The 80CL52 acknowledges interrupt requests from fourteen sources as follows:

- INTO through INT9
- Timer 0, Timer 1, and Timer 2
- UART

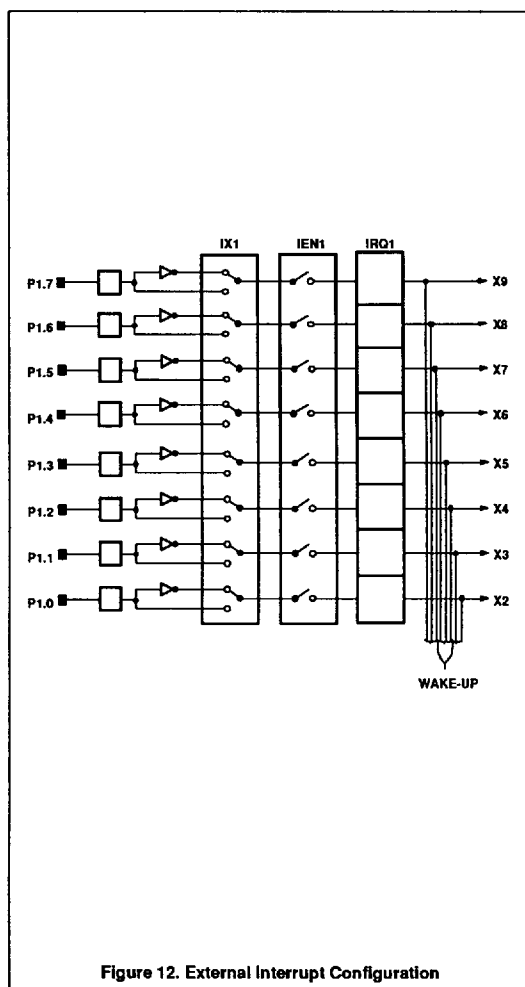
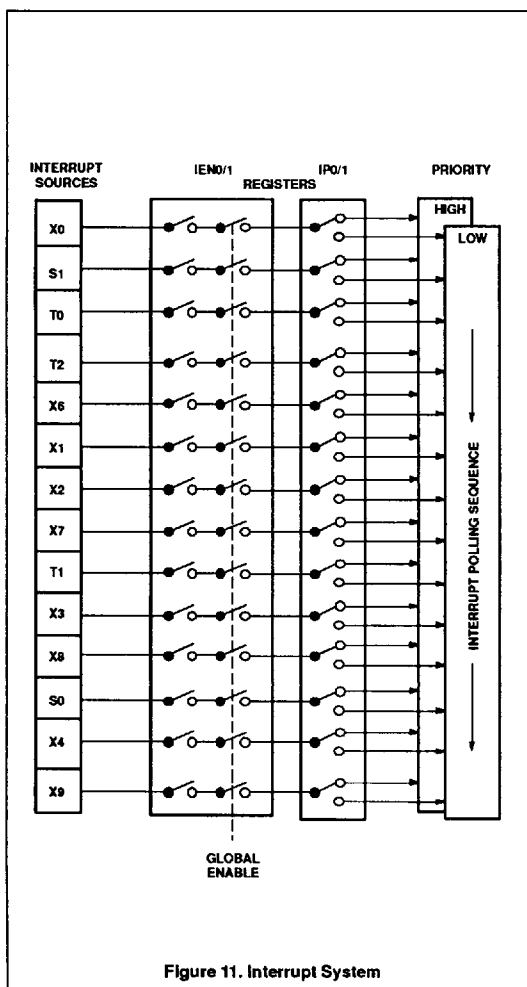
1.6.1 External Interrupts INT2 / INT9

Port 1 lines serve an alternative purpose as seven additional interrupts INT2 to INT9. When enabled, each of these lines may "wake-up" the device from Power-down mode. Using the IX1 register, each pin may be initialized to either active HIGH or LOW. IRQ1 is the interrupt request flag register. Each flag, if the interrupt is enabled, will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

Each interrupt vectors to a separate location in program memory for its service routine. Each

source can be individually enabled or disabled by corresponding bits in the Interrupt Enable Registers (IE, IE0). The priority level is selected via the Interrupt Priority register (IPO, IP1). All enabled sources can be globally disabled or enabled.

The port 1 interrupts are level sensitive. A port 1 interrupt will be recognized when a level (HIGH or LOW depending on Interrupt Polarity Register IX1) on P1x is held active for at least one machine cycle. The Interrupt Request is not served until the next machine cycle.



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Interrupt enable register IEN0, IEN1  
IEN0 (A8H)

EA	ET2	ES1	ES0	ET1	EX1	ET0	EX0
----	-----	-----	-----	-----	-----	-----	-----

Bit	Symbol	Function
IEN0.7	EA	General enable/disable control
		0 = no interrupt is enabled 1 = any individually enabled interrupt will be accepted
IEN0.6	-	Enable T2 interrupt
IEN0.5	ES1	Must be set to 0 by the user
IEN0.4	ES0	Enable UART SIO interrupt
IEN0.3	ET1	Enable timer T1 interrupt
IEN0.2	EX1	Enable external interrupt 1
IEN0.1	ET0	Enable Timer T0 interrupt
IEN0.0	EX0	Enable external interrupt 0

IEN1 (E8H)

EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2
-----	-----	-----	-----	-----	-----	-----	-----

Bit	Symbol	Function
IEN1.7	EX9	Enable external interrupt 9
IEN1.6	EX8	Enable external interrupt 8
IEN1.5	EX7	Enable external interrupt 7
IEN1.4	EX6	Enable external interrupt 6
IEN1.3	EX5	Enable external interrupt 5
IEN1.2	EX4	Enable external interrupt 4
IEN1.1	EX3	Enable external interrupt 3
IEN1.0	EX2	Enable external interrupt 2

where 0 = interrupt disabled  
1 = interrupt enabled

Interrupt priority register IP0, IP1  
IP0 (B8H)

-	PT2	PS1	PS0	PT1	PX1	PT0	PX0
---	-----	-----	-----	-----	-----	-----	-----

bit	Bit	Function	Sym
IP0.7	-	Unused	
IP0.6	PT2	Timer 2 interrupt priority level	
IP0.5	PS1	Unused	
IP0.4	PS0	UART SIO interrupt priority level	
IP0.3	PT1	Timer 1 interrupt priority level	
IP0.2	PX1	External interrupt 1 priority level	
IP0.1	PT0	Timer 0 interrupt priority level	
IP0.0	PX0	External interrupt 0 priority level	

Interrupt priority is as follows:  
0 = low priority  
1 = high priority

IP1 (B8H)

PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2
-----	-----	-----	-----	-----	-----	-----	-----

Bit	Symbol	Function
IP1.7	PX9	External interrupt 9 priority level
IP1.6	PX8	External interrupt 8 priority level
IP1.5	PX7	External interrupt 7 priority level
IP1.4	PX6	External interrupt 6 priority level
IP1.3	PX5	External interrupt 5 priority level
IP1.2	PX4	External interrupt 4 priority level
IP1.1	PX3	External interrupt 3 priority level
IP1.0	PX2	External interrupt 2 priority level

Interrupt polarity register IX1  
IX1 (E9H)

IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2
-----	-----	-----	-----	-----	-----	-----	-----

Bit	Symbol	Function
IX1.7	IL9	External interrupt 9 polarity level
IX1.6	IL8	External interrupt 8 polarity level
IX1.5	IL7	External interrupt 7 polarity level
IX1.4	IL6	External interrupt 6 polarity level
IX1.3	IL5	External interrupt 5 polarity level
IX1.2	IL4	External interrupt 4 polarity level
IX1.1	IL3	External interrupt 3 polarity level
IX1.0	IL2	External interrupt 2 polarity level

Interrupt request flag register IRQ1  
IRQ1 (C0H)

IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2
-----	-----	-----	-----	-----	-----	-----	-----

Bit	Symbol	Function
IRQ1.7	IQ9	External interrupt 9 request flag
IRQ1.6	IQ8	External interrupt 8 request flag
IRQ1.5	IQ7	External interrupt 7 request flag
IRQ1.4	IQ6	External interrupt 6 request flag
IRQ1.3	IQ5	External interrupt 5 request flag
IRQ1.2	IQ4	External interrupt 4 request flag
IRQ1.1	IQ3	External interrupt 3 request flag
IRQ1.0	IQ2	External interrupt 2 request flag

Writing either a "1" or "0" to an IX1 register bit sets the polarity level of the corresponding external interrupt to active HIGH or LOW respectively.

1.6.2 Interrupt Vectors

Vector	Source
(highest)	
X0	0003H External/0
X5	0053H External 5
T0	000BH Timer 0
T2	0003H Timer 2
X6	005BH External 6
X1	0013H External 1
X2	003BH External 2
X7	0063H External 7
T1	001BH Timer 1
X3	0043H External 3
X8	006BH External 8
S0	002BH UART
X4	004BH External 4
X9	0073H External 9
(lowest)	

Interrupt priority

Each interrupt priority source can be set to either high or low priority. If both priorities are requested simultaneously, the controller will branch to the high priority vector.

A low priority interrupt can only be interrupted by a high priority interrupt. A high priority interrupt routine cannot be interrupted.

1.6.3 Related registers

The following registers are used in conjunction with the interrupt system:

Register	Function	SFR Address
IX1	Interrupt polarity register	E9H
IRQ1	Interrupt request flag register	C0H
IEN0	Interrupt enable register	A8H
IEN1	Interrupt enable register (INT2-INT9)	E8H
IP0	Interrupt priority register	B8H
IP1	Interrupt priority register (INT2-INT9)	F8H

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**1.7 Oscillator registers**

The on-chip oscillator circuitry of the 80CL52 is a single-stage inverting amplifier biased by an internal feedback resistor (Figure 13). For operation as a standard quartz oscillator, no external components are needed (except at 32 kHz). When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Figure 14 and oscillator options).

In the Power-down mode the oscillator is stopped and XTAL1 is pulled HIGH. The oscillator inverter is switched off to ensure no current will flow regardless of the voltage at

XTAL1. To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Fig. 14(f). There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is buffered by a flip-flop.

The following options are provided for optimum on-chip oscillator performance. Please state option when ordering.

**1.7.1 Oscillator options (see Figure 14)**

32kHz: Figure 14(c). An option for 32 kHz clock applications with external

trimmer for frequency adjustment. A 4.7 M $\Omega$  bias resistor is needed for use in parallel with the crystal.

- Osc 2: Figure 14(e): An option for low-power, low-frequency operations using LC components or quartz.
- Osc 3: An option for medium frequency range applications.
- Osc 4: An option for high frequency range applications.
- RC: Figure 14(g). An option for an RC oscillator.

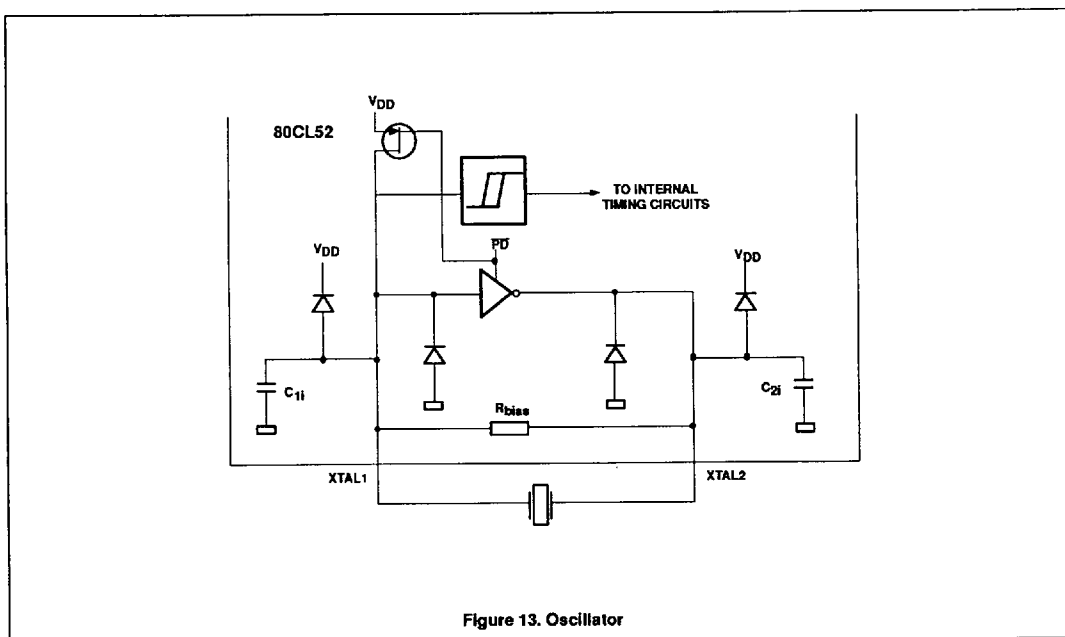


Figure 13. Oscillator

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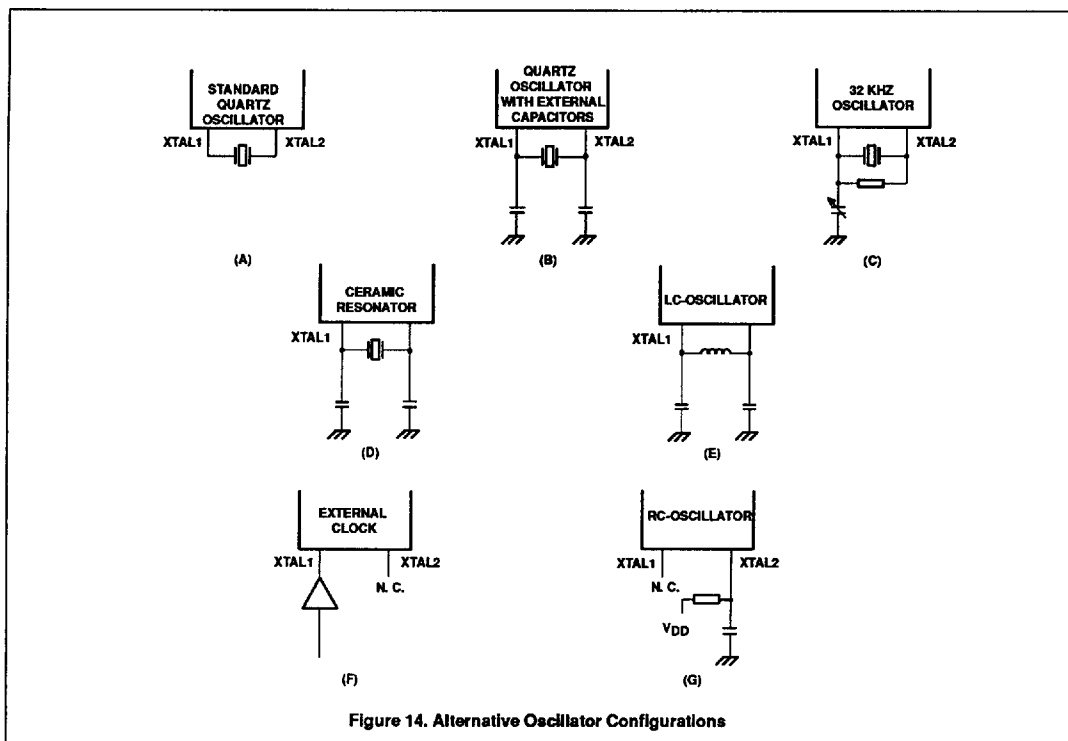


Figure 14. Alternative Oscillator Configurations

OSCILLATOR TYPE SELECTION GUIDE

RESONATOR	f(MHz)	OPTION	C1 EXT. (pF)		C2 EXT. (pF)		MAX. RESONATOR SERIES RESISTANCE 15 kΩ (1)
			MIN.	MAX.	MIN.	MAX.	
Quartz	0.032	32 kHz	5	15	0	0	600 Ω
Quartz	1.0	OSC. 2	0	30	0	30	100 Ω
Quartz	3.58	OSC. 2	0	15	0	15	75 Ω
Quartz	4.0	OSC. 2	0	20	0	20	60 Ω
Quartz	6.0	OSC. 3	0	10	0	10	60 Ω
Quartz	10.0	OSC. 4	0	15	0	15	40 Ω
Quartz	12.0	OSC. 4	0	10	0	10	10 Ω
PXE	0.455	OSC. 2	40	50	40	50	100 Ω
PXE	1.0	OSC. 2	15	50	15	50	10 Ω
PXE	3.58	OSC. 2	0	40	0	40	10 Ω
PXE	4.0	OSC. 2	0	40	0	40	10 Ω
PXE	6.0	OSC. 2	0	20	0	20	5 Ω
PXE	10.0	OSC. 3	0	15	0	15	6 Ω
PXE	12.0	OSC. 4	10	40	10	40	6 Ω
LC		OSC. 2	20	90	20	90	10 μH = 1 Ω 100 μH = 5 Ω 1 mH = 75 Ω

NOTE:

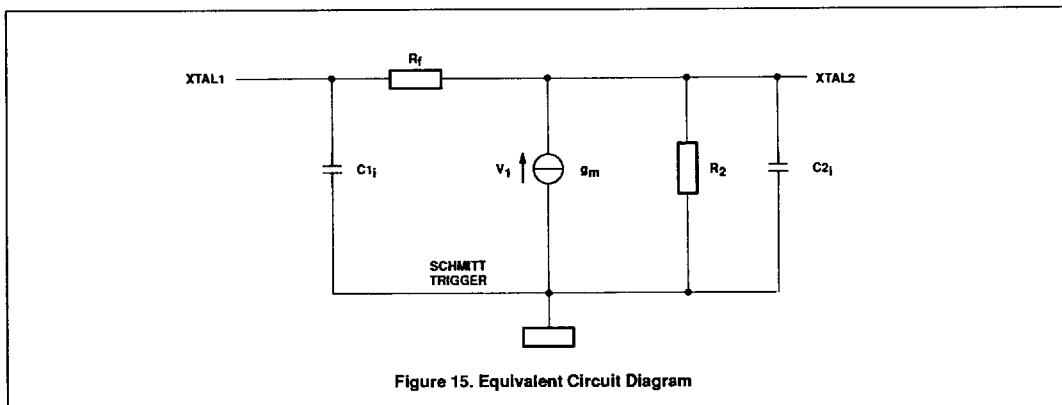
1. 32 kHz quartz crystals with a series resistance higher than 15 kΩ will reduce the guaranteed supply voltage range to 2.5 -3.5V. The equivalent circuit data of the internal oscillator compares with that of matched crystals.

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OSCILLATOR EQUIVALENT CIRCUIT PARAMETERS (see Figure 15)

PARAMETER	OPTION	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Transconductance	32 kHz	$g_m$	$T = +25\text{ }^\circ\text{C}; V_{DD} = 4.5\text{V}$	-	15	-	$\mu\text{s}$
	Osc.2	$g_m$	$T = +25\text{ }^\circ\text{C}; V_{DD} = 4.5\text{V}$	200	600	1000	$\mu\text{s}$
	Osc.3	$g_m$	$T = +25\text{ }^\circ\text{C}; V_{DD} = 4.5\text{V}$	400	1500	4000	$\mu\text{s}$
	Osc.4	$g_m$	$T = +25\text{ }^\circ\text{C}; V_{DD} = 4.5\text{V}$	1000	4000	10000	$\mu\text{s}$
Input Capacitance	32 kHz	$C_{1i}$		-	3.0	-	pF
	Osc. 2	$C_{1i}$		-	8.0	-	pF
	Osc. 3	$C_{1i}$		-	8.0	-	pF
	Osc. 4	$C_{1i}$		-	8.0	-	pF
Output Capacitance	32 kHz	$C_{2i}$		-	23	-	pF
	Osc. 2	$C_{2i}$		-	8.0	-	pF
	Osc. 3	$C_{2i}$		-	8.0	-	pF
	Osc. 4	$C_{2i}$		-	8.0	-	pF
Output Capacitance	32 kHz	$R_2$		-	3800	-	k $\Omega$
	Osc. 2	$R_2$		-	65	-	k $\Omega$
	Osc. 3	$R_2$		-	18	-	k $\Omega$
	Osc. 4	$R_2$		-	5.0	-	k $\Omega$



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**1.7.3 RC Oscillator** (see Figure 16)

The externally adjustable RC-oscillator has a frequency range from 100 kHz to 500 kHz.

**1.8 Reset circuitry**

To initialize the 80CL52, a reset is performed by either of two methods:

- via the RST pin
- via a power-on-reset

It leaves the internal registers as follows:

REGISTER	CONTENT
ACC	0000 0000
B	0000 0000
DPL	0000 0000
DPH	0000 0000
IE0	0000 0000
IE1	0000 0000
IP0	XX00 0000
IP1	0000 0000
IX1	0000 0000
IRQ1	0000 0000
PCH	0000 0000
PCL	0000 0000
PCON	0XXX 0000
P0-P3	1111 1111
S0BUF	XXXX XXXX
S0CON	0000 0000
SP	0000 0111
TCON	0000 0000
TH0, TH1, TH2	0000 0000
TL0, TL1, TL2	0000 0000
TMOD	0000 0000
PSW	0000 0000
RCAP2L	0000 0000
RCAP2H	0000 0000

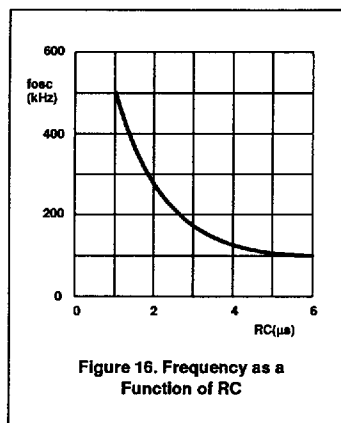


Figure 16. Frequency as a Function of RC

The reset state of the port pins is mask-programmable and can therefore be defined by the user. The standard reset value for port P0-P3 is 1111 1111.

The reset input to the 80CL52 is RST pin 15. A Schmitt trigger qualifies the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle.

A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods), while the oscillator is running. The CPU responds by generating an internal reset. Port pins adopt their reset state immediately after RST goes HIGH. During reset ALE and PSEN are held HIGH.

The external reset is asynchronous to the internal clock. The RST pin is sampled during State 5, Phase 2 of every machine cycle. After a HIGH is detected at the RST pin, an internal reset is repeated every cycle until RST goes LOW.

The internal RAM is not affected by reset. When  $V_{DD}$  is turned on the RAM contents are indeterminate.

**1.8.1 Power-on reset**

The 80CL52 contains on-chip circuitry which switch the port pins to the customer defined logic level as soon as  $V_{DD}$  exceeds 1.3 V. As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods.

A hysteresis of approximately 50mV at a typical power-on switching level of 1.3 V will ensure correct operation.

An automatic reset can be obtained at power-on by connecting the RST pin to  $V_{DD}$  via a 10 mF capacitor. At power-on, the voltage on the RST pin is equal to  $V_{DD}$  minus the capacitor voltage, and decreases from  $V_{DD}$  as the capacitor discharges through the internal resistor  $R_{RST}$  to ground. The larger the capacitor, the more slowly  $V_{RST}$  decreases.  $V_{RST}$  must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles.

**1.9 INSTRUCTION SET**

The 80CL52 uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Assigned opcodes add new high-power operation and permit new addressing modes. The instruction set consists of 49 single-byte, 46 two-byte and 16 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 ms and 45 in 2 μs. Multiply and divide instructions execute in 4 μs.

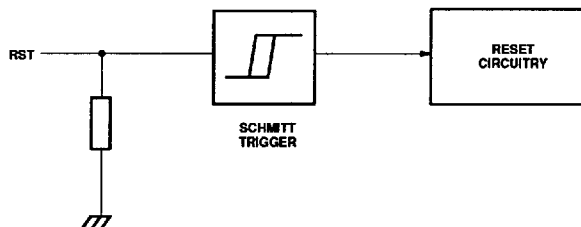


Figure 17. Reset Configuration at RST Pin

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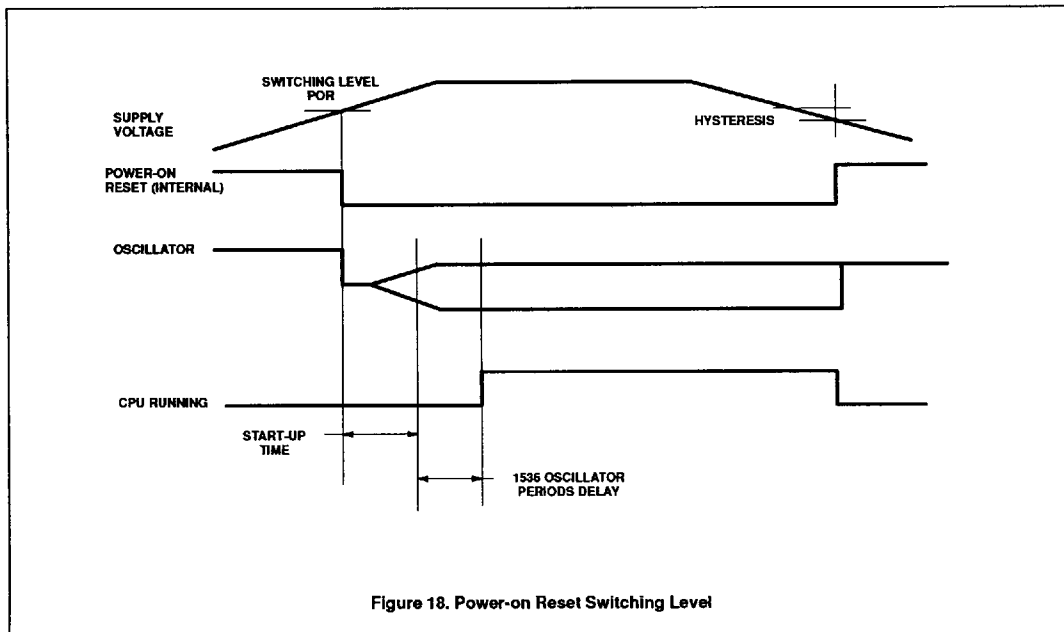


Figure 18. Power-on Reset Switching Level

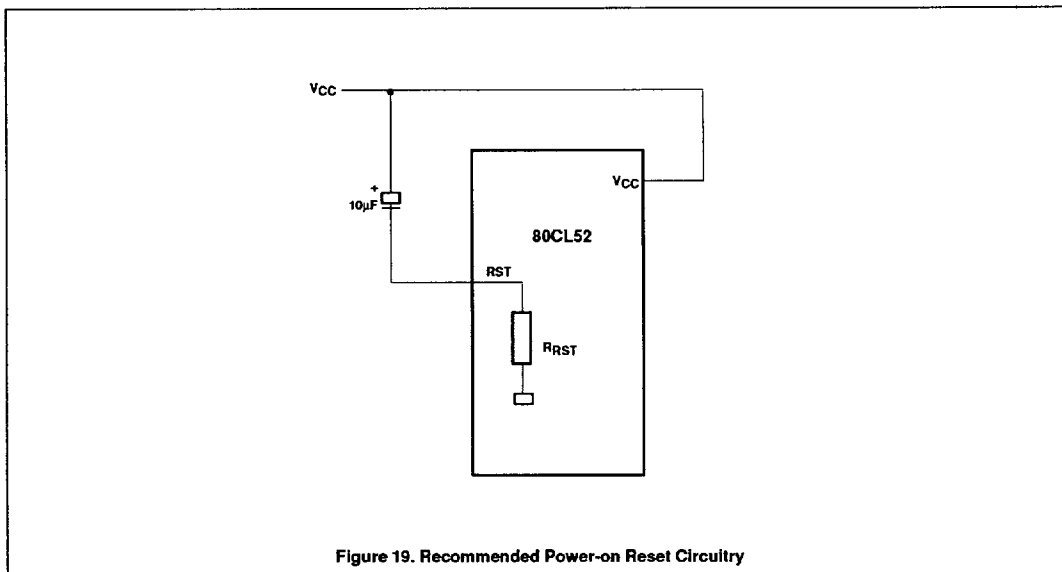


Figure 19. Recommended Power-on Reset Circuitry

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## INSTRUCTION SET

MNEMONC	DESCRIPTION	BYTES /CYCLES	OPCODE (HEX.)
<b>Arithmetic Operations</b>			
ADD A,Rr	Add register to A	1 1	25*
ADD A,direct	Add direct byte to A	2 1	25
ADD A,@R	Add indirect RAM to A	1 1	26, 27
ADD A,#data	Add immediate data to A	1 1	24
ADDC A,Rr	Add register to A with carry flag	1 1	3*
ADDC A,direct	Add direct byte to A with carry flag	2 1	35
ADDC A,@R	Add indirect RAM to A with carry flag	1 1	36, 37
ADDC A,#data	Add immediate data to A with carry flag	2 1	34
SUBB A,Rr	Subtract register from A with borrow	1 1	9*
SUBB A,direct	Subtract direct byte from A with borrow	2 1	95
SUBB A,@Ri	Subtract indirect RAM from A with borrow	1 1	96, 97
SUBB A,#data	Subtract immediate data from A with borrow	2 1	94
INC A	Increment A	1 1	04
INC Rr	Increment register	1 1	0*
INC direct	Increment direct byte	2 1	05
INC @R	Increment indirect RAM	1 1	06, 07
DEC A	Decrement A	1 1	14
DEC Rr	Decrement register	1 1	1*
DEC direct	Decrement direct byte	2 1	15
DEC @R	Decrement indirect RAM	1 1	16, 17
INC DPTR	Increment data pointer	1 2	A3
MUL AB	Multiply A & B	1 4	A4
DIV AB	Divide A by B	1 4	84
DA A	Decimal adjust A	1 1	D4
<b>Logic Operations</b>			
ANL A,Rr	AND register to A	1 1	5*
ANL A,direct	AND direct byte to A	2 1	55
ANL A,@R	AND indirect RAM to A	1 1	56, 57
ANL A,#data	AND immediate data to A	2 1	54
ANI direct,A	AND A to direct byte	2 1	52
ANL direct,#data	AND immediate data to direct byte	3 2	53
ORL A,Rr	OR register to A	1 1	4*
ORL A,direct	OR direct byte to A	2 1	45
ORL A,@Ri	OR indirect RAM to A	1 1	46, 47
ORL A,#data	OR immediate data to A	2 1	44
ORL direct,A	OR A to direct byte	2 1	42
ORL direct,#data	OR immediate data to direct byte	3 2	43
XRL A,Rr	Exclusive-OR register to A	1 1	6*
XRL A,direct	Exclusive-OR direct byte to A	2 1	65
XRL A,@Ri	Exclusive-OR indirect RAM to A	1 1	66, 67
XRL A,#data	Exclusive-OR immediate data to A	2 1	64
XRL direct,A	Exclusive-OR to direct byte	2 1	62
XRL direct,#data	Exclusive-OR immediate data to direct byte	3 2	63
CLR A	Clear A	1 1	E4

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## INSTRUCTION SET (Continued)

MNEMONC		DESCRIPTION	BYTES /CYCLES		OPCODE (HEX.)
<b>Logic Operations (Continued)</b>					
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4
<b>Data transfer</b>					
MOV*	A,Rr	Move register to A	1	1	E*
MOV	A,direct	Move direct byte to A	2	1	E5
MOV	A,@R	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A-DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A-PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E3, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	MOV A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7
<b>Bit-Operations</b>					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND direct bit to carry flag	2	2	B0

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## INSTRUCTION SET (Continued)

MNEMONIC	DESCRIPTION	BYTES /CYCLES	OPCODE (HEX.)
<b>Bit-Operations (Continued)</b>			
ORL C bit	OR direct bit to carry flag	2 2	72
ORL C /bit	OR complement of direct bit to carry flag	2 2	A0
MOV C,bit	Move direct bit to carry flag	2 1	A2
MOV bit,C	Move carry flag to direct bit	2 2	92
<b>Program and Machine Control</b>			
ACALL addr11	Absolute subroutine call	2 2	**1addr
LCALL addr16	Long subroutine call	3 2	12
RET	Return from subroutine	1 2	22
RETI addr11	Return from interrupt	1 2	32
AJMP addr16	Absolute jump	2 2	**1addr
LJMP rel	Long jump	3 2	02
SJMP rel	Short jump (relative address)	2 2	80
JMP @A+DPTR	Jump indirect relative to the DPTR	1 2	73
JZ rel	Jump if A is zero	2 2	60
JNZ rel	Jump if A is not zero	2 2	70
JC rel	Jump if carry flag is set	2 2	40
JNC rel	Jump if no carry flag	2 2	50
JB bit,rel	Jump if direct bit is set	3 2	20
JNB bit,rel	Jump if direct bit is not set	3 2	30
JBC bit,rel	Jump if direct bit is set and clear bit	3 2	10
CJNE A,direct ,rel	Compare direct to A and jump if not equal	3 2	B5
CJNE A,#data,rel	Compare immediate to A and jump if not equal	3 2	B4
CJNE Rr,#data,rel	Compare immediate to reg. and jump if not equal	3 2	B*
CJNE @Ri,#data,rel	Compare immediate to ind. and jump if not equal	3 2	B6, B7
DJNZ Rr,rel	Decrement register and jump if not zero	2 2	D*
DJNZ direct,rel	Decrement direct and jump if not zero	3 2	D5
NOP	No operation	1 1	00

## NOTES:

Data addressing modes:

- Rr = Working register R0 - R7
- direct = 128 internal RAM locations and any special function register (SFR)
- @Ri = Indirect internal RAM location addressed by register R0 or R1.
- #data = 8-bit constant included in instruction
- #data = 16-bit constant included in instruction
- bit = Direct constant included in instruction
- addr16 = 16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64K-byte program memory address space.
- addr11 = 11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.
- rel = Signed (two's complement) 8-bit offset byte. Used by SMJP and all conditional jumps. Range is -128 to +128 bytes relative to first byte of the following instruction.

Hexadecimal opcode cross-reference

- \* :8, 9, A, B, C, D, E, F.
- \*\* :11, 31, 51, 71, 91, B1, D1, F1.
- \*\*\* :01, 21, 41, 61, 81, A1, C1, E1.

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## 2.0 RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage (pin 40)	$V_{DD}$	-0.5	+6.5	V
All input voltages	$V_I$	-0.5	$V_{DD}+0.5$	V
DC current into any input or output	$I_I, I_O$	-	5	mA
Total power dissipation	$P_{tot}$	-	300	mW
Storage temperature range	$T_{stg}$	-65	+150	°C
Operating ambient temperature range	$T_{amb}$	-40	+85	°C
Operating junction temperature	$T_j$	-	125	°C

## 3.0 DC CHARACTERISTICS

 $V_{DD} = 1.8V$ ;  $V_{SS} = 0V$ ;  $T_{amb} = -40$  to  $+85^\circ C$ ; all voltages with respect to  $V_{SS}$ ; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
$V_{DD}$	Supply voltage		1.8		6.0	V
	RAM retention voltage in power-down mode		1.0	—	6.0	V
$I_{DD}$	Supply current: Operating (note 1)	$V_{DD} = 5V$ ; $f_{clk} = 12$ MHz	—	—	tbody	mA
		$V_{DD} = 3V$ ; $f_{clk} = 3.58$ MHz	—	—	tbody	mA
	Idle mode (note 2)	$V_{DD} = 5V$ ; $f_{clk} = 12$ MHz	—	—	tbody	mA
		$V_{DD} = 3V$ ; $f_{clk} = 3.58$ MHz	—	—	tbody	mA
$I_{PD}$	Power-down (note 3)	$V_{DD} = 1.8V$ ; $T_{amb} = 25^\circ C$	—	—	10	mA
$V_{IL}$	Input voltage LOW (note 6)	$V_{SS} < V_I < V_{DD}$	$V_{SS}$	—	$0.3V_{DD}$	V
$V_{IH}$	Input voltage HIGH (note 6)		$0.7V_{DD}$	—	$V_{DD}$	V
$\pm I_{LI}$	Input leakage current (port 0, EA)				10	$\mu A$
$I_{OL}$	Output sink current LOW	$V_{DD} = 5V$ ; $V_{OL} = 0.4V$	1.6	—	—	mA
		$V_{DD} = 2.5V$ ; $V_{OL} = 0.4V$	0.7	0.7	—	mA
$-I_{OH}$	Output source current HIGH, push-pull options only	$V_{DD} = 5V$ ; $V_{OH} = V_{DD}-0.4V$	1.6	1.6	—	mA
		$V_{DD} = 3V$ ; $V_{OH} = V_{DD}-0.4V$	0.7	0.7	—	mA
$-I_{IL}$	Input current logic 0	$V_{DD} = 5V$ ; $V_{IN} = 0.4V$	—	—	100	$\mu A$
		$V_{DD} = 3V$ ; $V_{IN} = 0.4V$	—	—	50	$\mu A$
$-I_{TL}$	Input current logic 0, 1-to-0 transition	$V_{DD} = 5V$ ; $V_{IN} = V_{DD}/2$	—	—	1.0	mA
		$V_{DD} = 3V$ ; $V_{IN} = V_{DD}/2$	—	—	500	$\mu A$
$R_{RST}$	RST pull-down resistor		10	—	200	k $\Omega$

## NOTES TO DC CHARACTERISTICS:

- The operating supply current is measured with all output pins disconnected; XTAL 1 driven with  $t_r = t_f = 10$  ns;  $V_{IL} = V_{SS}$ ;  $V_{IH} = V_{DD}$ ; XTAL2 not connected; EA = RST + PORT 0 =  $V_{DD}$ .
- The idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with  $t_r = t_f = 10$  ns;  $V_{IL} = V_{SS}$ ;  $V_{IH} = V_{DD}$ ; XTAL2 is not connected; EA = PORT 0 =  $V_{DD}$ .
- The power-down current is measured with all output pins disconnected; XTAL 1 not connected; EA = Port 0 =  $V_{DD}$ ; RST =  $V_{SS}$ .
- Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3 pins when these pins make a 1-to-0 transition during bus operations. In the most adverse conditions (capacitive loading > 100 pF) the noise pulse on the ALE line may exceed 0.8 V. In this event it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger strobe input.
- Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and PSEN to momentarily fall below the 0.9% of  $V_{DD}$  specification when the address bits are stabilizing.

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**4.0 AC CHARACTERISTICS**

$V_{DD} = 5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$  for Port 0; ALE and PSEN,  $C_L = 40\text{ pF}$  for all other outputs unless otherwise specified.

**PROGRAM MEMORY** (See Figure 20)

PARAMETER	SYMBOL	12 MHz		VARIABLE CLOCK		
		MIN.	MAX	MIN.	MAX	UNIT
ALE pulse duration	$t_{LL}$	127	-	$2t_{CK}-40$	-	ns
Address set-up time to ALE	$t_{AL}$	43	-	$t_{CK}-40$	-	ns
Address hold time to ALE	$t_{LA}$	48	-	$t_{CK}-35$	-	ns
Time from ALE to control pulse PSEN	$t_{LC}$	58	-	$t_{CK}-25$	-	ns
Time from ALE to valid instruction input	$t_{LIV}$	-	233	-	$4t_{CK}-100$	ns
Control pulse duration PSEN	$t_{CC}$	215	-	$3t_{CK}-35$	-	ns
Time from PSEN to valid instruction input	$t_{CIV}$	-	215	-	$3t_{CK}-125$	ns
Input instruction hold time after PSEN	$t_{CI}$	0	-	0	-	ns
Input instruction float delay after PSEN	$t_{CIF}$	-	63	-	$t_{CK}-20$	ns
Address valid after PSEN	$t_{AC}$	75	-	$t_{CK}-8$	-	
Address to valid instruction input	$t_{AIV}$	-	302	-	$5t_{CK}-115$	
Address float time to PSEN	$t_{AFC}$	12	-	0	-	ns

**EXTERNAL DATA MEMORY** (See Figures 21 and 22)

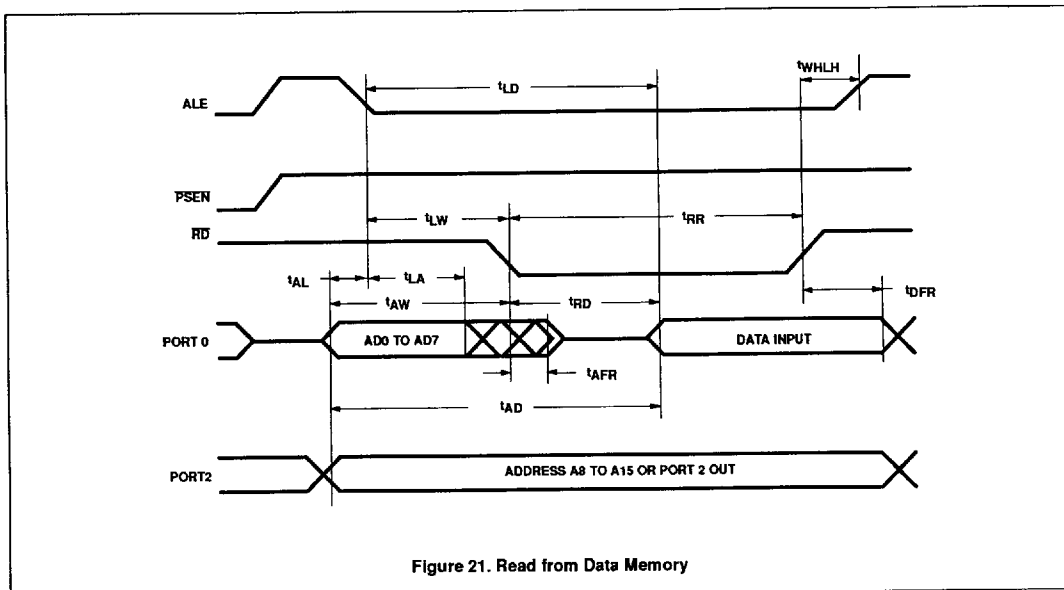
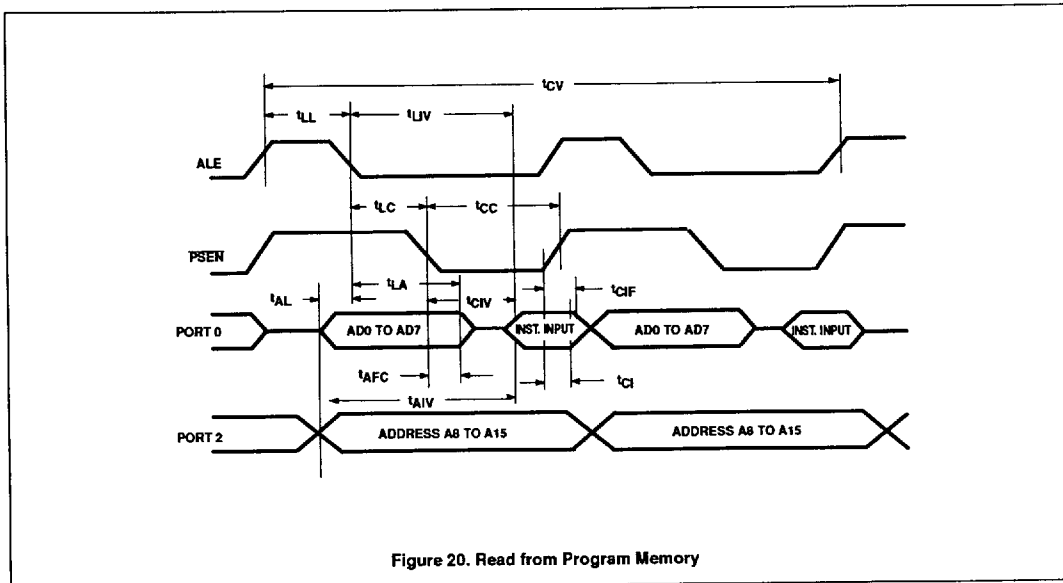
PARAMETER	SYMBOL	12 MHz		VARIABLE CLOCK		
		MIN.	MAX	MIN.	MAX.	UNIT
RD pulse duration	$t_{RR}$	400	-	$6t_{CK}-100$	-	ns
WR pulse duration	$t_{WW}$	400	-	$6t_{CK}-100$	-	ns
Address hold time after ALE	$t_{LA}$	48	-	$t_{CK}-35$	-	ns
RD to valid data input	$t_{RD}$	-	150	-	$5t_{CK}-165$	ns
Data float delay after RD	$t_{DFR}$	-	97	-	$2t_{CK}-70$	ns
Time from ALE to valid data input	$t_{LD}$	-	517	-	$8t_{CK}-150$	ns
Address to valid data input	$t_{AD}$	-	585	-	$9t_{CK}-165$	ns
Time from ALE to RD and WR	$t_{LW}$	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to RD and WR	$t_{AW}$	203	-	$4t_{CK}-130$	-	ns
Time from RD or WR HIGH to ALE HIGH	$t_{WHLH}$	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to WR transition	$t_{DWX}$	23	-	$t_{CK}-60$	-	ns
Data set-up time before WR	$t_{DW}$	433	-	$7t_{CK}-150$	-	ns
Data hold time after WR	$t_{WD}$	33	-	$t_{CK}-50$	-	ns
Address float delay after RD	$t_{WAFR}$	-	12	-	12	ns

**NOTE TO THE AC CHARACTERISTICS:**

- Interfacing the 80CL52 to devices with float times up to 75 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

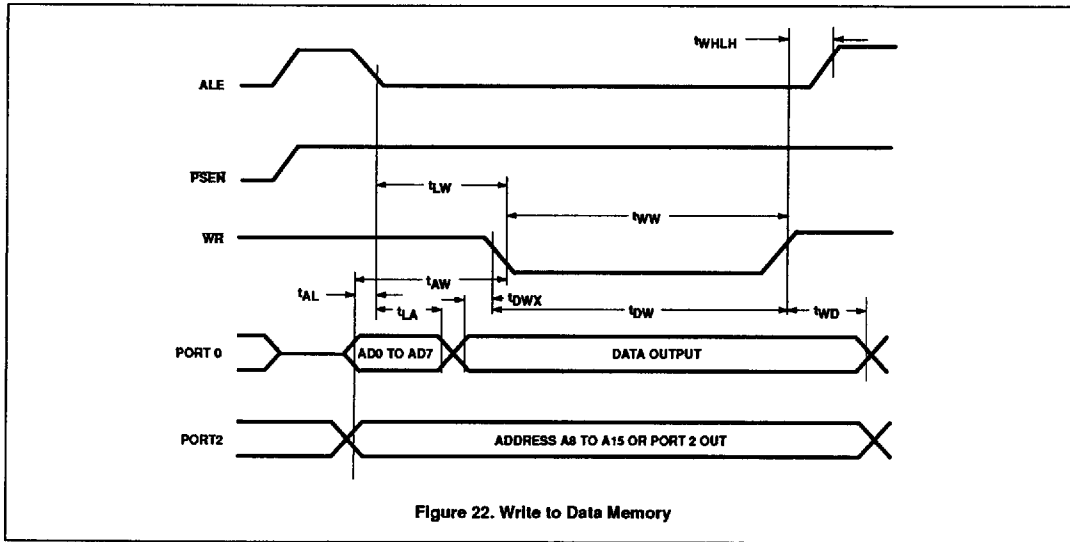
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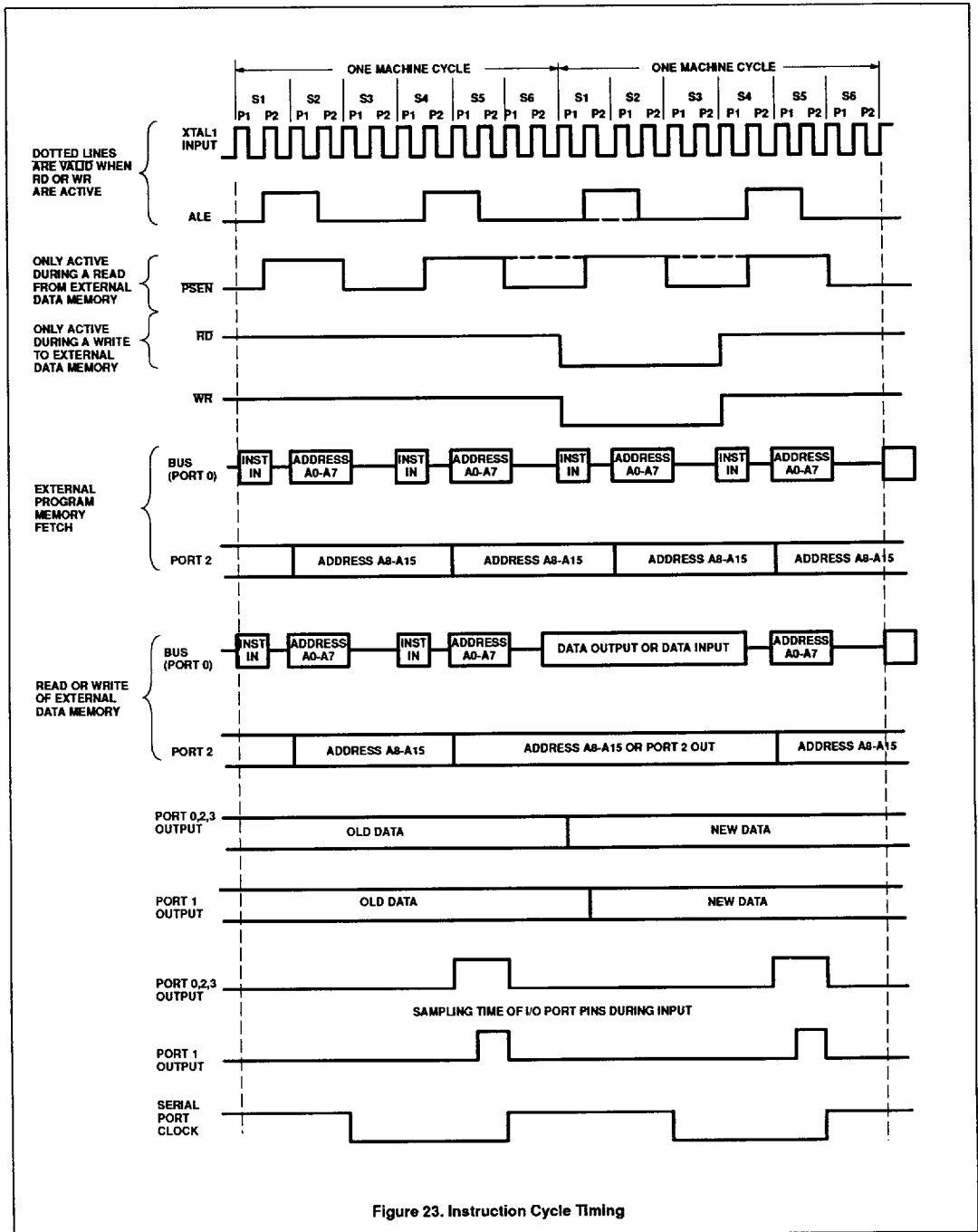


Figure 23. Instruction Cycle Timing

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5.0 CHARACTERISTICS CURVES

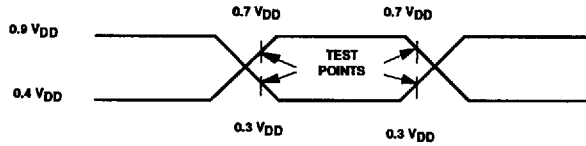


Figure 24. AC Testing Input Waveform

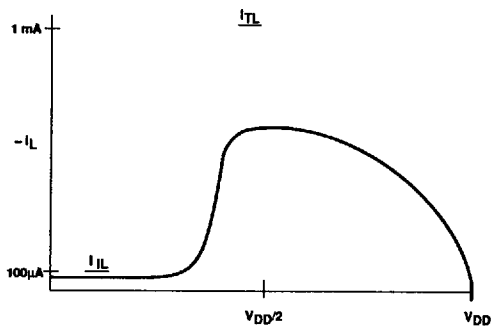


Figure 25. Input Current

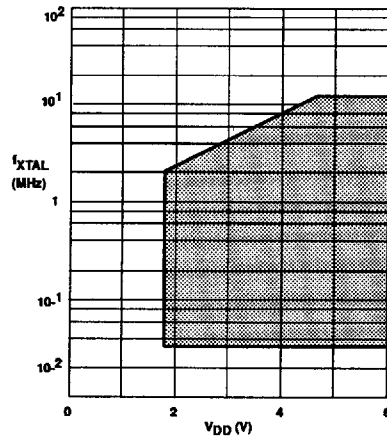


Figure 26. Frequency Operating Range

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