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1M x 32 FLASH MODULE

PUMA 68F32006/A-90/12/15

Issue 4.2 : December 1999

Description

The PUMA 68F32006 is a high density 32Mbit CMOS 5V Only FLASH memory organised as 1M x 32 in a JEDEC 68 pin surface mount PLCC, with read access times of 90, 120, and 150ns.

The output width is user configurable as 8 , 16 or 32 bits using four Chip Selects (CE1~4) for optimum application flexibility.

The module incorporates Embedded Algorithms for Program and Erase with Sector architecture (64K sector) and supports full chip erase.

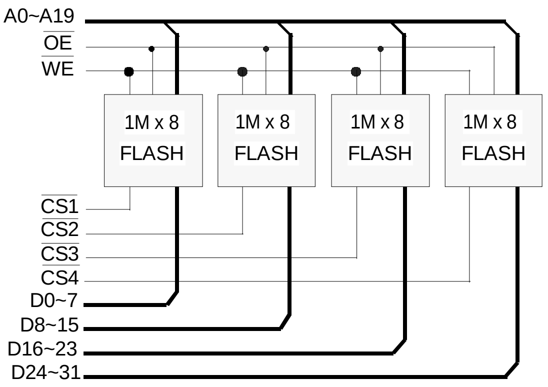
The device also features hardware sector protection, which disables both program and erase operations in any of the 64 sectors on the module.

A version 'A' with four independant write enables (WE1-4) is available.

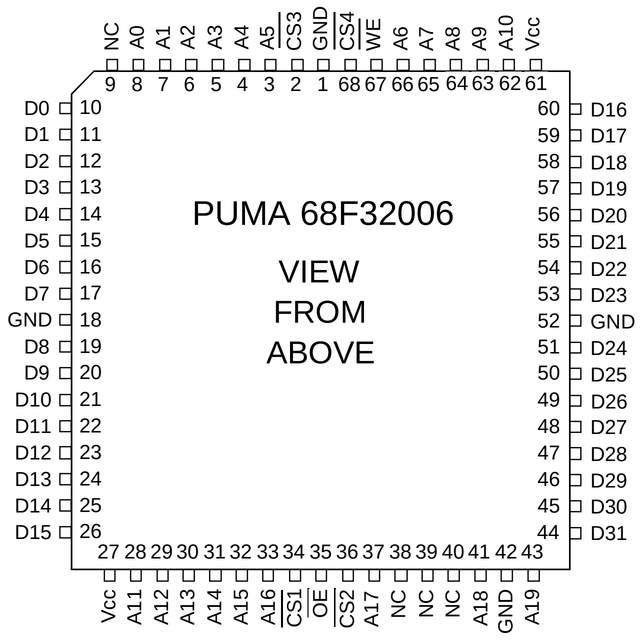
Features

- Fast Access Times of 90/120/150 ns.
- Output Configurable as 32 / 16 / 8 bit wide.
- Commercial, Industrial, or Military (Restricted) grade.
- Automatic Write/Erase by Embedded Algorithm - end of Write/Erase indicated by DATA Polling and Toggle Bit.
- Flexible Sector Erase Architecture - 64K byte sector size, with hardware protection of sector groups.
- Single Byte Program of 7µs (Typ.)
- Erase/Write Cycle Endurance 100,000 (Min.) - E variant.

Block Diagram (see page 24 for 'A' version)



Pin Definition (see page 24 for 'A' version)



Pin Functions

A0-A19	**Address Input**	**D0-D31**	**Data Inputs/Outputs**
CE1-4	**Chip Enables**	**WE**	**Write Enable (WE1-4 for 'A' version)**
OE	**Output Enable**	**Vcc**	**Power (+5V)**
GND	**Ground**		

Absolute Maximum Ratings (1)

	max	*unit*
Voltage on any pin w.r.t. Gnd	-2.0 to +7	V
Supply Voltage (2)	-2.0 to +7	V
Voltage on A9 w.r.t. Gnd (3)	-2.0 to +13.5	V
Storage Temperature	-65 to +125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operationof the device at those or any other conditions above those indicated in the operational sections of this specification is not implied.

(2) Minimum DC voltage on any input or I/O pin is -0.5V. Maximum DC voltage on output and I/O pins is Vcc+0.5V During transitions voltage may overshoot by +/-2V for upto 20ns

(3) Minimum DC input voltage on A9 is -0.5V during voltage transitions, A9 may overshoot Vss to -2V for periods of up to 20ns, maximum DC input voltage in A9 is 12.5V which may overshoot to 14.0V for periods up to 20ns

Recommended Operating Conditions

Parameter		*min*	*typ*	*max*	*unit*
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5	-	V_{CC}+0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (-I suffix)
	T_{AM}	-55	-	115	°C (-M suffix)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
I/P Leakage CurrentAddress, $\overline{OE}$, $\overline{WE}$		I_{LI1}	V_{CC}=V_{CC} max, V_{IN}=0V or V_{CC}	-	-	±4	µA
A9 Input Leakage Current		I_{LI2}	V_{CC}=V_{CC} max, A9=12V	-	-	200	µA
Other Pins		I_{LI3}	V_{CC}=V_{CC} max, V_{IN}=0V or V_{CC}	-	-	±1	µA
Output Leakage Current		I_{LO}	V_{CC}=V_{CC} max, V_{OUT}=0V or V_{CC}	-	-	±4	µA
V_{CC} Operating Current	32 bit	I_{CCO32}	$\overline{CE}$=V_{IL}(1), $\overline{OE}$=V_{IH}, I_{OUT}=0mA, *f*=6MHz	-	-	120	mA
	16 bit	I_{CCO16}	As above	-	-	62	mA
	8 bit	I_{CCO8}	As above	-	-	33	mA
V_{CC} Program/Erase Current	32 bit	I_{CCP32}	Programming in Progress	-	-	240	mA
	16 bit	I_{CCP16}	As above	-	-	122	mA
	8 bit	I_{CCP8}	As above	-	-	63	mA
Standby Supply Current		I_{SB1}	V_{CC}=V_{CC} max, $\overline{CE}$=V_{IH}(1) $\overline{OE}$ = V_{IH}	-	-	4	mA
Autoselect / Sector Protect Voltage		V_{ID}	V_{CC} = 5.0V	11.5	-	12.5	V
Output Low Voltage		V_{OL}	I_{OL}=12mA. V_{CC} = V_{CC} min.	-	-	0.45	V
Output High Voltage		V_{OH1}	I_{OH}=-2.5mA. V_{CC} = V_{CC} min.	2.4	-	-	V
Low V_{CC} Lock-Out Voltage		V_{LKO}		3.2	-	4.2	V

Notes (1) CE above are accessed through $\overline{CE1-4}$. These inputs must be operated simultaneoulsy for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

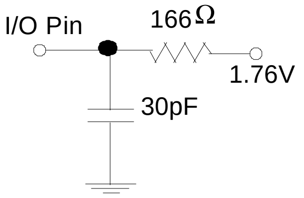
Capacitance (T$_A$=25°C,f=1MHz)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	Address, $\overline{OE}$, $\overline{WE}$	C_{IN1}	V_{IN}=0V	-	35	pF
	Other pins	C_{IN2}	V_{IN}=0V	-	14	pF
Output Capacitance	32 bit	C_{OUT32}	V_{OUT}=0V	-	54	pF

Note: These parameters are calculated, not measured.

AC Test Conditions

- * Input pulse levels : 0.0V to 3.0V
- * Input rise and fall times : 5 ns
- * Input and output timing reference levels : 1.5V
- * VCC = 5V +/- 10%
- * Module tested in 32 bit mode



AC OPERATING CONDITIONS

Read Cycle

Parameter	*Symbol*	90			
		min	typ	max	Unit
Read Cycle Time	t_{RC}	90	-	-	ns
Address to output delay	t_{ACC}	-	-	90	ns
Chip enable to output	t_{CE}	-	-	90	ns
Output enable to output	t_{OE}	-	-	40	ns
Output enable to output High Z	t_{DF}	-	-	20	ns
Output hold time from address	t_{OH}	0	-	-	ns

$\overline{CE}$ or $\overline{OE}$ whichever occurs first

Parameter	*Symbol*	120			150			
		min	typ	max	min	typ	max	Unit
Read Cycle Time	t_{RC}	120	-	-	150	-	-	ns
Address to output delay	t_{ACC}	-	-	120	-	-	150	ns
Chip enable to output	t_{CE}	-	-	120	-	-	150	ns
Output enable to output	t_{OE}	-	-	50	-	-	55	ns
Output enable to output High Z	t_{DF}	-	-	30	-	-	35	ns
Output hold time from address	t_{OH}	0	-	-	0	-	-	ns

$\overline{CE}$ or $\overline{OE}$ whichever occurs first

Write/Erase/Program

Parameter	*Symbol*	*90* min	typ	max	unit
Write Cycle time (2)	t_{WC}	90	-	-	ns
Address Setup time	t_{AS}	0	-	-	ns
Address Hold time	t_{AH}	45	-	-	ns
Data Setup Time	t_{DS}	45	-	-	ns
Data hold Time	t_{DH}	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	ns
Read Recover before Write	t_{GHWL}	0	-	-	ns
$\overline{CE}$ setup time	t_{CE}	0	-	-	ns
$\overline{CE}$ hold time	t_{CH}	0	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	45	-	-	ns
$\overline{WE}$ Pulse Width High	t_{WPH}	20	-	-	ns
Byte Programming operation	t_{WHWH1}	-	8	-	µs
Sector Erase operation (1)	t_{WHWH2}	-	1	15	sec
Vcc setup time (2)	t_{VCS}	50	-	-	µs

Parameter	*Symbol*	*120* min	typ	max	*150* min	typ	max	unit
Write Cycle time (2)	t_{WC}	120	-	-	150	-	-	ns
Address Setup time	t_{AS}	0	-	-	0	-	-	ns
Address Hold time	t_{AH}	50	-	-	50	-	-	ns
Data Setup Time	t_{DS}	50	-	-	50	-	-	ns
Data hold Time	t_{DH}	0	-	-	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHWL}	0	-	-	0	-	-	ns
$\overline{CE}$ setup time	t_{CE}	0	-	-	0	-	-	ns
$\overline{CE}$ hold time	t_{CH}	0	-	-	0	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	50	-	-	50	-	-	ns
$\overline{WE}$ Pulse Width High	t_{WPH}	20	-	-	20	-	-	ns
Byte Programming operation	t_{WHWH1}	-	8	-	-	8	-	µs
Sector Erase operation (1)	t_{WHWH2}	-	1	15	-	1	15	sec
Vcc setup time (2)	t_{VCS}	50	-	-	50	-	-	µs

Notes: (1) This does not include the preprogramming time.
(2) Not 100% tested.

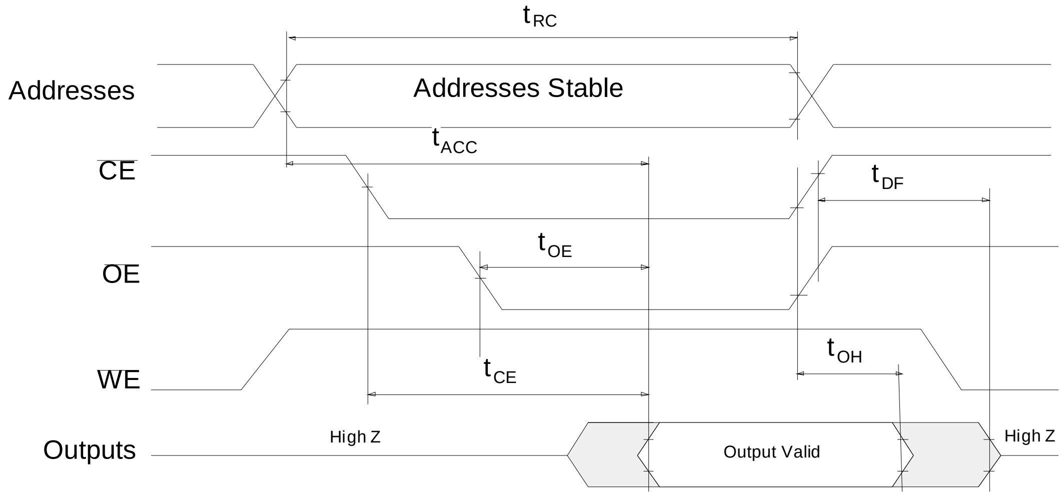
Write/Erase/Program Alternate $\overline{CE}$ controlled Writes

Parameter	*Symbol*	*90* min	typ	max	unit
Write Cycle time (2)	t_{WC}	90	-	-	ns
Address Setup time	t_{AS}	0	-	-	ns
Address Hold time	t_{AH}	45	-	-	ns
Data Setup Time	t_{DS}	45	-	-	ns
Data hold Time	t_{DH}	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	ns
Read Recover before Write	t_{GHEL}	0	-	-	ns
$\overline{WE}$ setup time	t_{WS}	0	-	-	ns
$\overline{WE}$ hold time	t_{WH}	0	-	-	ns
$\overline{CE}$ Pulse Width	t_{CP}	45	-	-	ns
$\overline{CE}$ Pulse Width High	t_{CPH}	20	-	-	ns
Programming operation	t_{WHWH1}	-	8	-	us
Sector Erase operation (1)	t_{WHWH2}	-	1	15	sec
Vcc setup time (2)	t_{VCS}	-	50	-	us

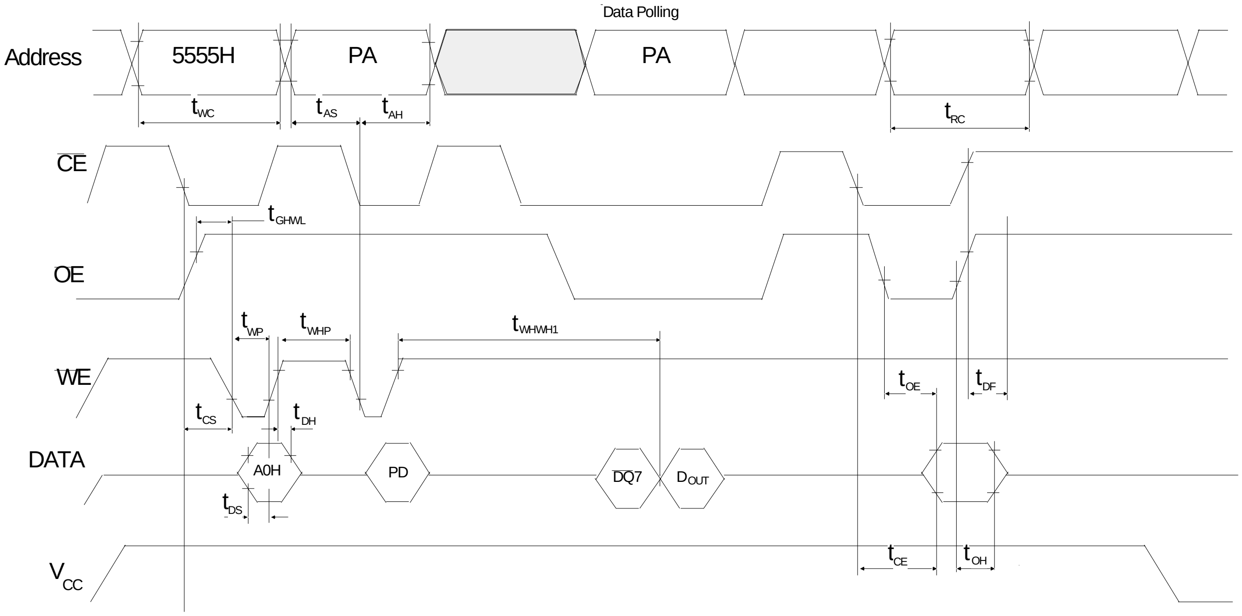
Parameter	*Symbol*	*120*			*150*			
		min	typ	max	min	typ	max	unit
Write Cycle time (2)	t_{WC}	120	-	-	150	-	-	ns
Address Setup time	t_{AS}	0	-	-	0	-	-	ns
Address Hold time	t_{AH}	50	-	-	50	-	-	ns
Data Setup Time	t_{DS}	50	-	-	50	-	-	ns
Data hold Time	t_{DH}	0	-	-	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHEL}	0	-	-	0	-	-	ns
$\overline{WE}$ setup time	t_{WS}	0	-	-	0	-	-	ns
$\overline{WE}$ hold time	t_{WH}	0	-	-	0	-	-	ns
$\overline{CE}$ Pulse Width	t_{CP}	50	-	-	50	-	-	ns
$\overline{CE}$ Pulse Width High	t_{CPH}	20	-	-	20	-	-	ns
Programming operation	t_{WHWH1}	-	8	-	-	8	-	us
Sector Erase operation (1)	t_{WHWH2}	-	1	15	-	1	15	sec
Vcc setup time (2)	t_{VCS}	-	50	-	-	50	-	us

Note: (1) Does not include pre-programming time.
(2) Not 100% tested.

AC Waveforms for Read Operation



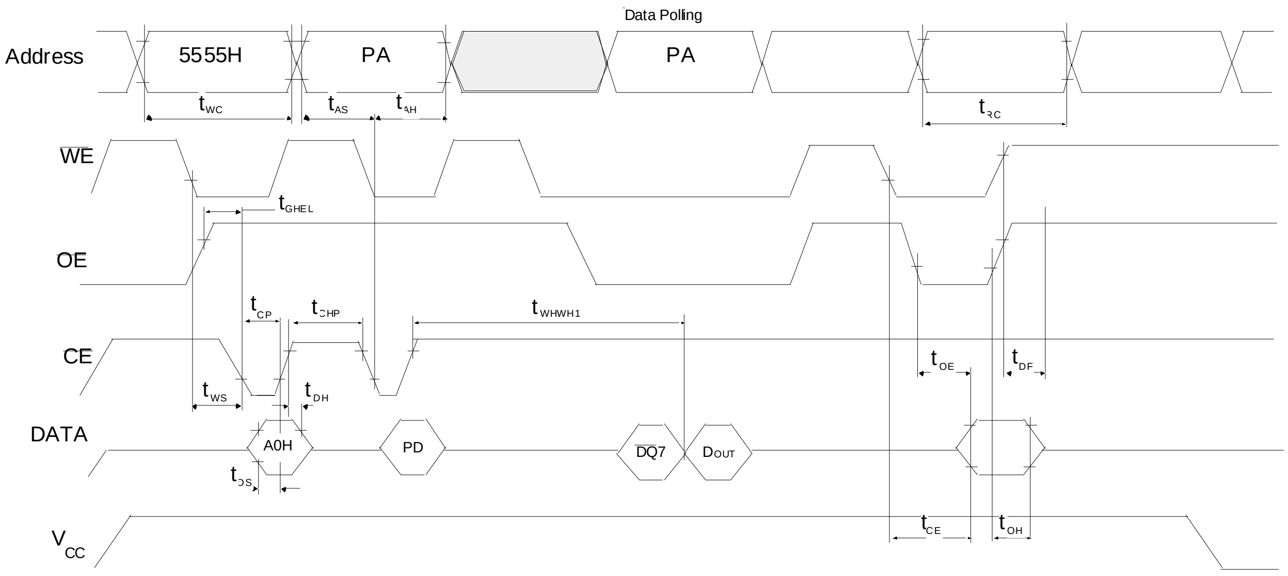
AC Waveforms Program



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the out put of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

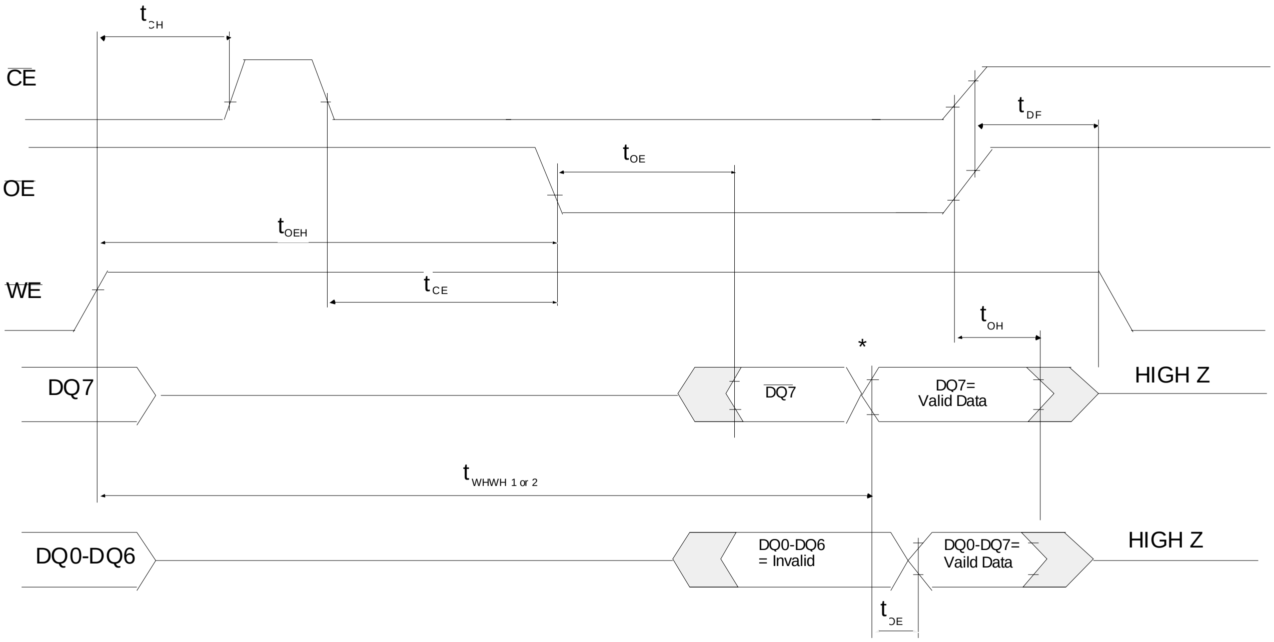
A.C Waveforms - Alternate CE controlled Program operation timings



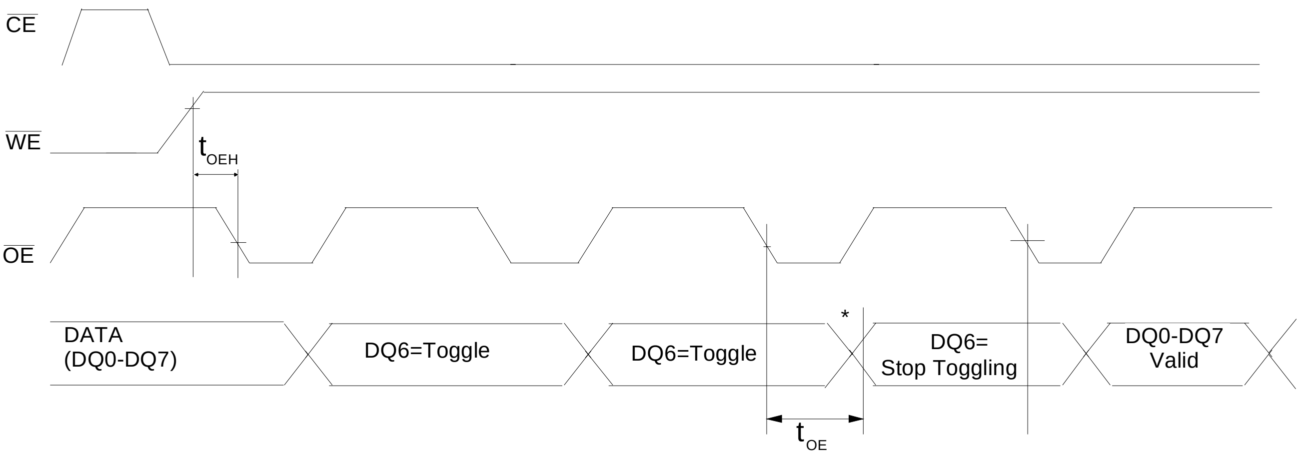
NOTES:

1. PA is address of memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC Waveforms for Data Polling During Embedded Algorithm Operations

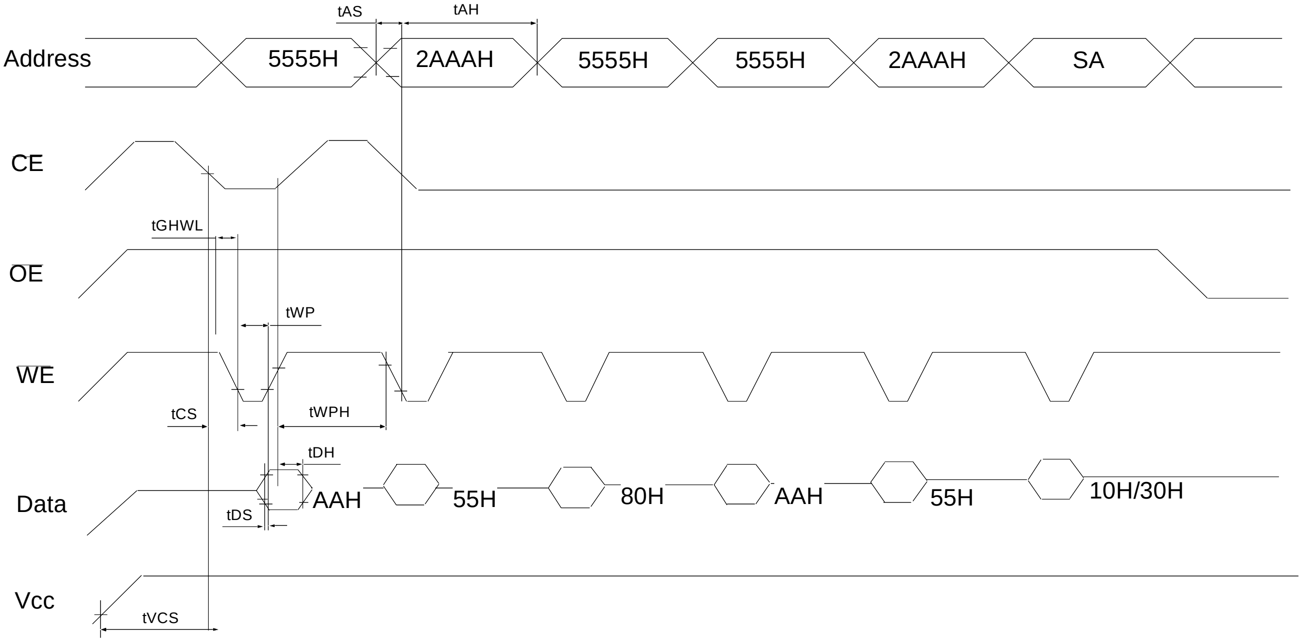


AC Waveforms for Toggle Bit During Embedded Algorithm Operations



* DQ6 stops toggling (the device has completed the embedded operations)

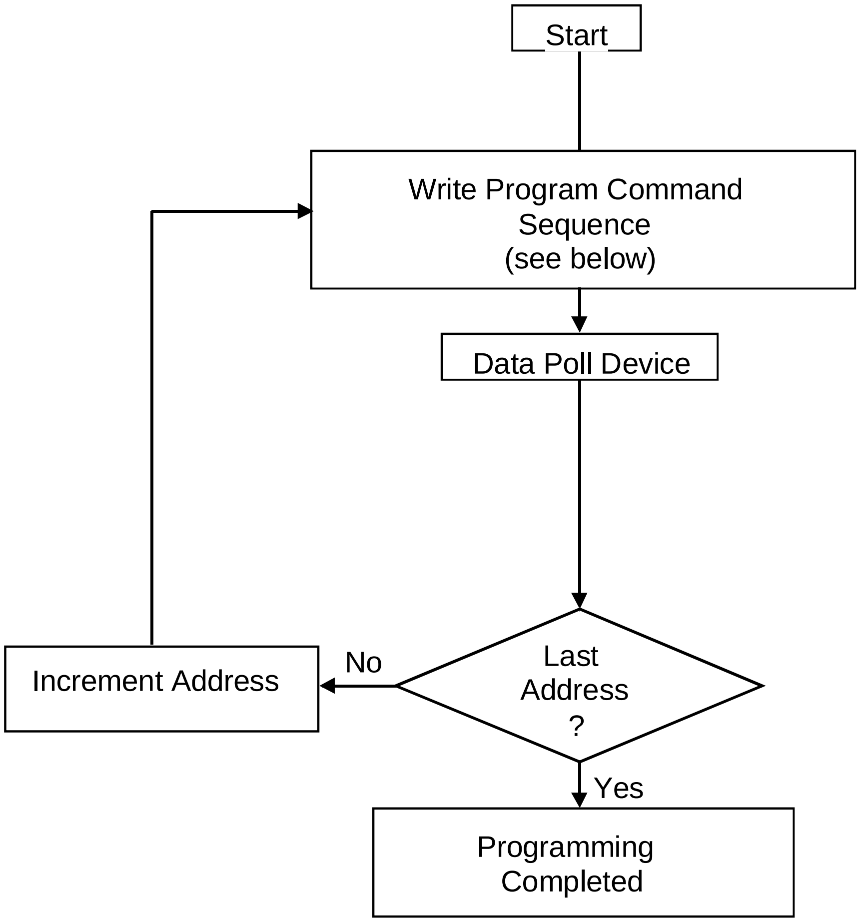
AC Waveforms Chip / Sector Erase



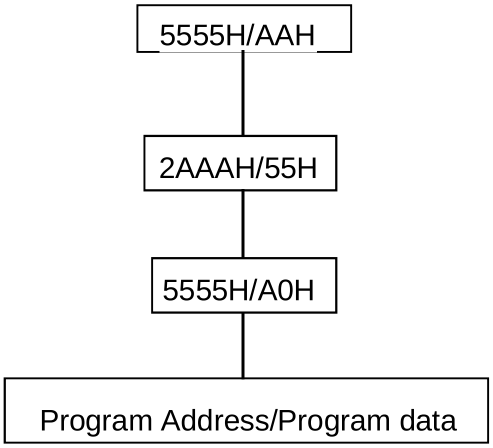
NOTES:

1. SA is the address for sector erase. Addresses = don't care for Chip Erase.

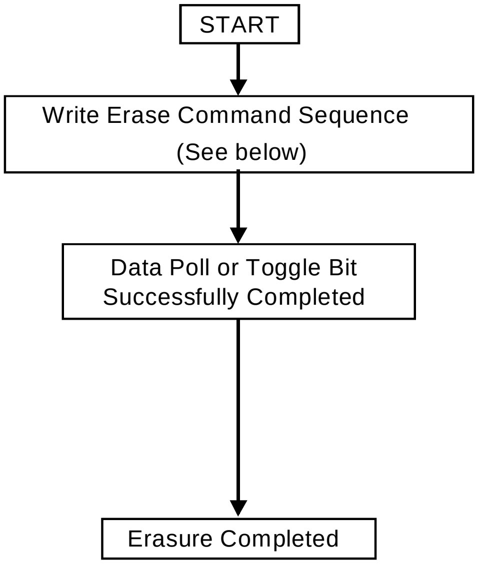
EMBEDDED PROGRAMMING ALGORITHM



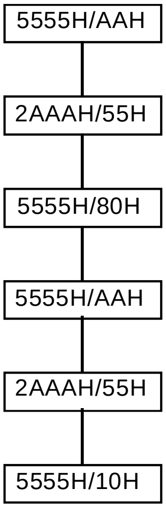
Program Command Sequence (Address /Command)



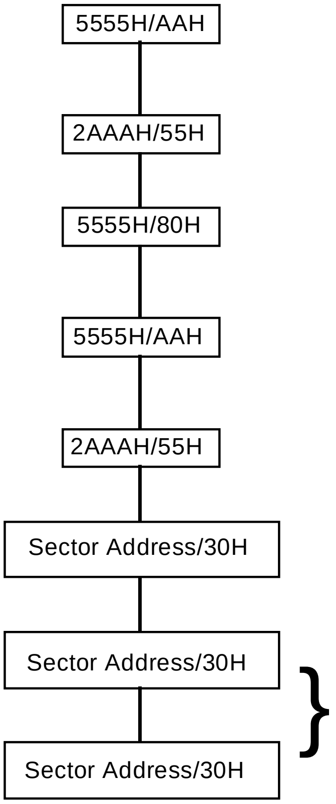
EMBEDDED ERASE ALGORITHM



Chip Erase Command Sequence
(Address/Command):

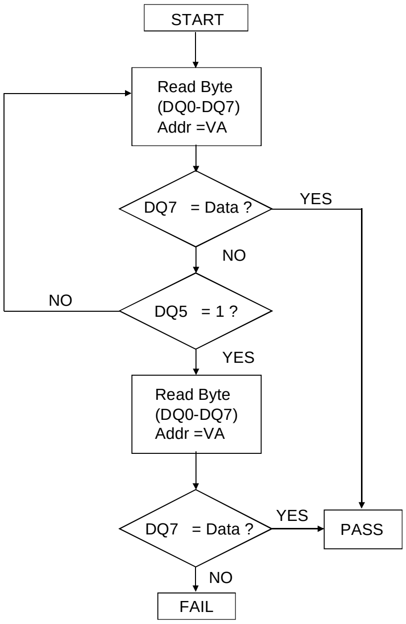


Individual Sector/Mulitiple Sector
Erase Command Sequence
(Address/Command):



Additional sector erase commands are optional

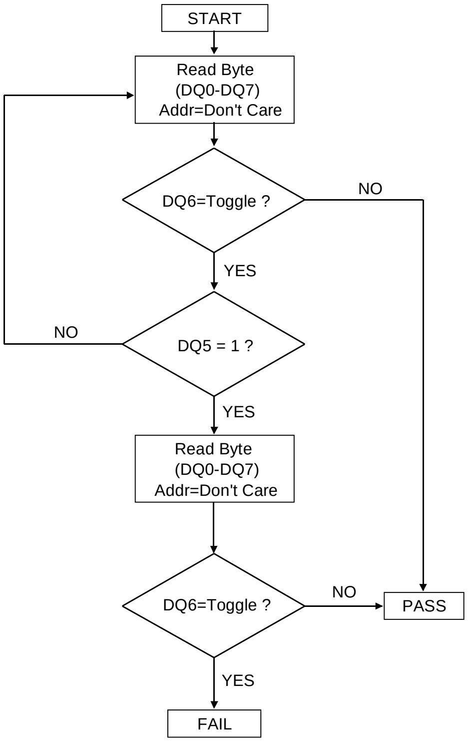
DATA POLLING ALGORITHM



NOTE:

1. DQ7 is rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.
2. VA = Byte address for programming.
   = Any of the sector addresses within the sector being erased during sector erase operation
   = Valid address equals any Non-protected sector group address during chip erase.

TOGGLE BIT ALGORITHM



NOTES:

1. DQ6 is rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same time as DQ5 changing to "1".

DEVICE OPERATION

The following description deals with the device operating in 8 bit mode accessed through CE1, however status flag definitions shown apply equally to the corresponding flag for each device in the module.

Read Mode

The device has two control functions which must be satisfied in order to obtain data at the outputs
CE1-4 is the power control and should be used for device selection
OE is the output control and should be used to gate data to the output pins if the device is selected.

Standby Mode

Two standby modes are available :
CMOS standby : CE1-4 held at Vcc +/- 0.3V
TTL standby : CE1-4 held at V_{IH}
In the standby mode the outputs are in a high impedance state independent of the OE input. If the device is deselected during erasure or programming the device will draw active current until the operation is completed.

Output Disable

With the OE input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify the die manufacturer and type. This mode is intended for use by programming equipment. This mode is functional over the full military temperature range. The autoselect codes for the first device are as follows :

Type	A17-A19	A6	A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacture Code	X	V_{IL}	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Device Code	X	V_{IL}	V_{IL}	V_{IH}	A4H	1	1	0	1	0	1	0	1
Sector Group Protection	Sector Group Address	V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

* Outputs 01H at protected sector address

To activate this mode the programming equipment must force V_{ID} on address A9 . Two identifier bytes may then be sequenced from each die device outputs by toggling A0 from V_{IL} to V_{IH}. All addresses are dont care apart from A0, A1, A6. All identifiers for manufacturer and device will exhibit odd parity with D7 defined as the parity bit. In order to read the proper device codes when executing the autoselect A1 must be V_{IL}.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The register is a latch used to store the commands along with the address and data information required to execute the command. The command register is written by bringing WE/WE1-4 to V_{IL} while CE1-4 is at V_{IL} and OE is at V_{IH}.Addresses are latched on the falling edge of WE/WE1-4 while data is latched on the rising edge.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. The following table defines these register command sequences.

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXXH	F0H										
Read/Reset	3	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	3	5555H	AAH	2AAAH	55H	5555H	90H	00H/ 01H	01H/D5H				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Erase Suspend	1	XXXXH	B0H										
Erase Resume	1	XXXXH	30H										

NOTES:

1. Address bit A15,A14,A13, A12, A11=X=Don't care.
2. RA=Address of the memory location to be read.
   PA=Address of memory location to be programmed. Addresses are latched on the falling edge of the $\overline{\text{WE}}$ pulse .
   SA=Address of the sector to be erased. The combination of A19, A18, A17 and A16 will uniquely select any sector.
3. RD=Data read from location RA during read operation.
   PD=Data to be programmed at location PA. Data is latched on the falling edge of $\overline{\text{WE}}$

Read / Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Sector Group Protection

The device features hardware sector group protection. This feature will disable both program and erase operations in any combination of sector groups of memory. The sector protect feature is enabled using programming equipment at the users site. The device is shipped with all sector groups unprotected.

It is also possible to determine if a sector is protected in the system by writing the autoselect command. Performing a read operation at XX02H , where the higher order addresses (A17, A18, A19) is the desired sector group address, will produce 01H data at DQ0 for a protected sector group.

Sector Address Table

	A19	A18	A17	A16	Address Range
SA0	0	0	0	0	000000h-00FFFFh
SA1	0	0	0	1	010000h-01FFFFh
SA2	0	0	1	0	020000h-02FFFFh
SA3	0	0	1	1	030000h-03FFFFh
SA4	0	1	0	0	040000h-04FFFFh
SA5	0	1	0	1	050000h-05FFFFh
SA6	0	1	1	0	060000h-06FFFFh
SA7	0	1	1	1	070000h-07FFFFh
SA8	1	0	0	0	080000h-08FFFFh
SA9	1	0	0	1	090000h-09FFFFh
SA10	1	0	1	0	0A0000h-0AFFFFh
SA11	1	0	1	1	0B0000h-0BFFFFh
SA12	1	1	0	0	0C0000h-0CFFFFh
SA13	1	1	0	1	0D0000h-0DFFFFh
SA14	1	1	1	0	0E0000h-0EFFFFh
SA15	1	1	1	1	0F0000h-0FFFFFh

Sector Group Address Table

	A19	A18	A17	Sectors
SGA0	0	0	0	SA0-SA1
SGA1	0	0	1	SA2-SA3
SGA2	0	1	0	SA4-SA5
SGA3	0	1	1	SA6-SA7
SGA4	1	0	0	SA8-SA9
SGA5	1	0	1	SA10-SA11
SGA6	1	1	0	SA12-SA13
SGA7	1	1	1	SA14-SA15

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target systems. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally a desired system design practice.

The device contains an autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 01H. A read cycle from address XX01H returns the device code D5H. Further, the write protect status of sectors can be read in this mode. Scanning the sector group addresses (A17, A18, A19) while (A6,A1,A0)=(0, 1, 0) will produce a logical '1' at device output DQ0 for a protected sector group.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycle. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of WE/WE1-4 or CE1-4, whichever happens later, while the data are latched on the rising edge of WE/WE1-4 or CE1-4 whichever happens first. The rising edge of WE/WE1-4 or CE1-4 begins programming. Upon executing the Embedded Program Algorithm Command sequence the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin. The automatic programming operation is completed when the data on D7 is equivalent to data written to this bit (see written Operations Status) at which time the device returns to read mode. Data Polling must be performed at the memory location which is being programmed.

Programming is allowed in any address sequence and across sector boundaries.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase doesn't require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase. The systems is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last WE pulse in the command sequence and terminates when the data on D7 is "1" (See Written Operation Section) at which time the device returns to read the mode.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock"write cycles. These are followed by writing the "Set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (30H) is latched on the rising edge of $\overline{WE}$. A time-out of 50us from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased sequentially by writing the six bus cycle operations as desribed above. This sequence is followed with writes of the sector erase command to addresses in other sectors desired to be sequentially erased. A time-out of 50us from the rising edge of the $\overline{WE}$ pulse for the last sector erase command will initiate the sector erase. If another sector erase command is wriiten within the 50us time-out window the timer is reset. Any command other than sector erase within the time-out window will reset the device to the read mode, ignoring the previous command string (refer to Write Operation Status section for Sector Erase Timer operation). Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7).

Sector erase doesn't require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 50us time-out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on D7 is "1" (see Written Operation Status Section) at which time the device returns to read mode. Data polling must be preformed at an address within any of the sectors being erased.

Erase Suspend

Erase suspend allows the user to interrupt a sector erase operation and then perform data reads or programs to a sector not being erased.

This command is only applicable during the sector erase operation which includes the time-out period for sector erase. Writing the erase suspend command during the sector erase time-out results in immediate termination of the time-out period & suspension of the erase operation. Writing the erase resume command resumes the erase operation.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Byte program. The end of the erase-suspend program operation is detected by data polling, or by the toggle bit. Note that DQ7 must be read from the byte program address.

To resume the sector erase operation, the resume command (30H) should be written. Any further writes of the resume command at this point will be ignored.

Operating Modes

The following modes are used to control the device.

OPERATION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	I /O
Auto-Select Manufacturer Code	L	L	H	L	L	L	V_{ID}	Code
Auto Select Device Code	L	L	H	H	L	L	V_{ID}	Code
Read(1)	L	L	X	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	High Z
Output Disable	L	H	H	X	X	X	X	High Z
Write	L	H	L	A0	A1	A6	A9	Din
Verify Sector Group Protect	L	L	H	L	H	L	V_{ID}	Code

1) L=V_{IL}, H=$V_{IH,}$ X=Don't Care

NOTE: 1) $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL} , $\overline{OE}$ at V_{IH} initiates write cycle.

WRITE OPERATIONS STATUS

	Status		DQ7	DQ6	DQ5	DQ3	DQ2
In Progress	Byte Program in Embedded Program Algorithm		$\overline{DQ7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspend Sector)	1	1	0	0	Toggle (Note 1)
		Erase Suspend Read (Non-Erase Suspend Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspend Sector)	$\overline{DQ7}$	Toggle (Note 2)	0	0	1 (Note 3)
Exceeded Time Limits	Byte Program in Embedded Program Algorithm		$\overline{DQ7}$	Toggle	1	0	1
	Program/Erase in Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspend Sector)	$\overline{DQ7}$	Toggle	1	1	N/A

Notes:

1. Performing successive read operations from the erase-suspended sector will cause DQ2 to toggle.
2. Performing successive read operations from any address will cause DQ6 to toggle.
3. Reading the byte address being programmed while in the erase-suspend program mode will indicate logic '1' at the DQ2 bit. However, successive reads from the erase-suspended sector will cause DQ2 to toggle.

D7 $\overline{\text{Data}}$ Polling

The device features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During the Embedded Programming Algorithm, an attempt to read the device will produce the complement of the data last written to D7. Upon completion of the Embedded Programming Algorithm an attempt to read the device will produce the true data last written to D7.

During the Embedded Erase Algorithm, D7 will be "0" until the erase operation is completed. Upon completion data at D7 is "1". For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspend, Erase-Suspend-Program, or sector erase time-out.

D6 Toggle Bit

The device also features the "toggle bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read data from the device will result in D6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, D6 will stop toggling and valid data will be read on successive attempts. During programming, the Toggle bit is valid after the rising edge of the forth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase, the Toggle bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector Erase, the toggle bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is active during the sector time-out.

D5 Exceeding Time Limits

D5 will indicate if the program or erase time has exceeded the specified limits. Under these conditions D5 will produce "1", indicating the program or erase cycle was not successfully completed . $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions .

The D5 failure condition may also appear if the user tries to program a non blank location without erasing. In this case the device locks out and never completes the embedded algorithm operation. Hence the system never reads a valid data on D7 and D6 never stops toggling. Once the device has exceeded timing limits, the D5 bit will indicate '1'

D3 Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. D3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, D3 may be used to determine if the sector erase timer window is still open. If D3 is high the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If D3 is low , the device will accept additional sector erase commands. To insure the command has been accepted, the software should check the status of D3 prior to and following each subsequent sector erase command. If D3 were high on the second status check, the command may not have been accepted.

DATA PROTECTION

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the internal state machine in the Read mode. Also, with its controls register architecture , alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from Vcc power up and power down transitions or system noise.

Low Vcc Write Inhibit

To avoid initiation of a write cycle during V_{CC} power up and power down, a write cycle is locked out for $V_{CC}<V_{LKO}$. If $V_{CC}<V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is usually correct to prevent unintentional writes when $V_{CC}>V_{LKO}$.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CE}$, $\overline{WE}$ will not initiate a write cycle

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE}=V_{IL}$, $\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be logical zero while OE is a logical one.

Power Up Write Inhibit

Power-up of the device with $\overline{WE}=\overline{CE}=V_{IL}$ and $\overline{OE}=V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

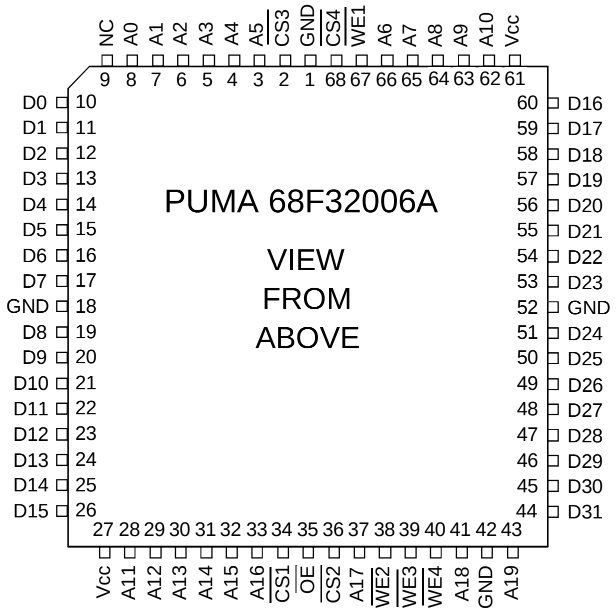
Sectors of the device may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

ERASE AND PROGRAMMING PERFORMANCE

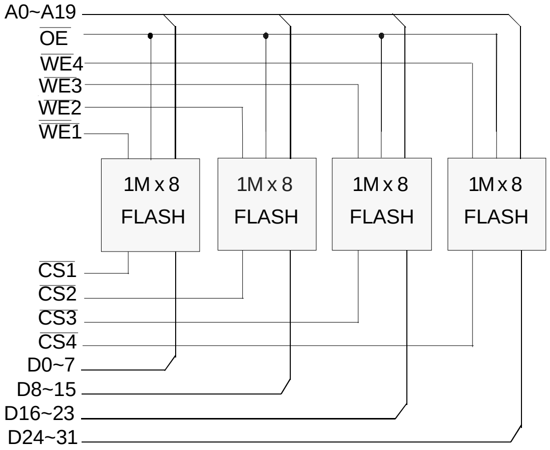
Parameter	Limits			Unit	Comments
	Min	**Typ**	**Max**		
Sector Erase Time	-	1 (Note 1)	15	sec	Excludes 00H programming prior to erasure.
Byte Programming Time	-	7 (Note 1)	1000	us	Excludes System-level overhead.
Chip Programming Time	-	7.2 (Note 1)	50	sec	Excludes system-level overhead.
Chip Erase Time	-	16 (Note 1)	240	sec	Exclude 00H programming prior to erase

Notes: (1) 25^{O}C, 5V V_{CC}, 100,000 cycles.

Version 'A' Pin Definition

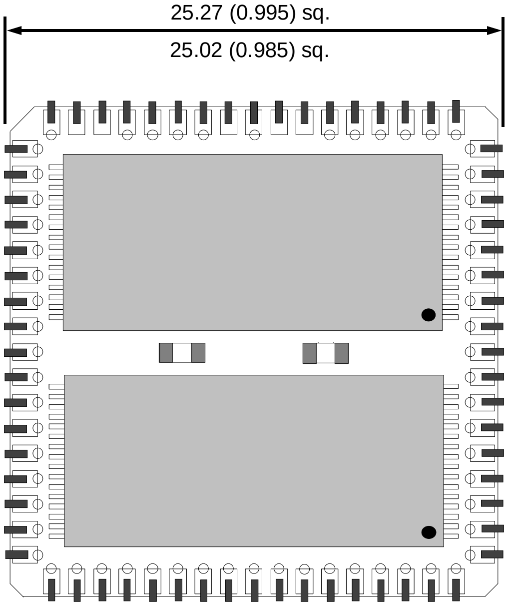


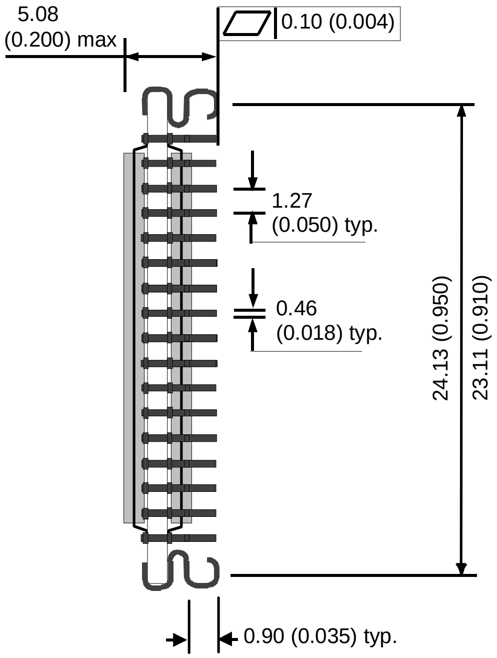
Version 'A' Block Diagram



Package Information Dimensions in mm(inches)

Plastic 68 Pin JEDEC Surface mount PLCC





Ordering Information

PUMA 68F32006AM-90E

Speed 90 = 90 ns
12 = 120 ns
15 = 150 ns

Temperature range Blank = Commercial Temperature
I = Industrial Temperature
M = Military Temperature (Restricted)

Special Features Blank = Single $\overline{WE}$
A = $\overline{WE1-4}$

Organisation 32006 = 1M x 32, user configurable as 2M x 16 and 4M x 8

Memory Type F = FLASH

Package PUMA 68 = 68 pin "J" Leaded PLCC

NOTE: The E variant is designated to parts with extended Erase/Write Cycle Endurance (100,000 Min.). If not specified when ordered only a Erase/Write Cycle Endurance of 10,000 Minimum can be guaranteed.

ISSUE HISTORY

PUMA 68F32006-90/12/15

Issue 4.1 DCN3964	First issue based on AMD29F080.
Issue 4.2	Restricted military Operating temperature from 125^{O}C to 115^{O}C