STEL-1130

Data Sheet

STEL-1130

Quadrature Amplitude/Vector Modulator

STANFORD TELECOM®

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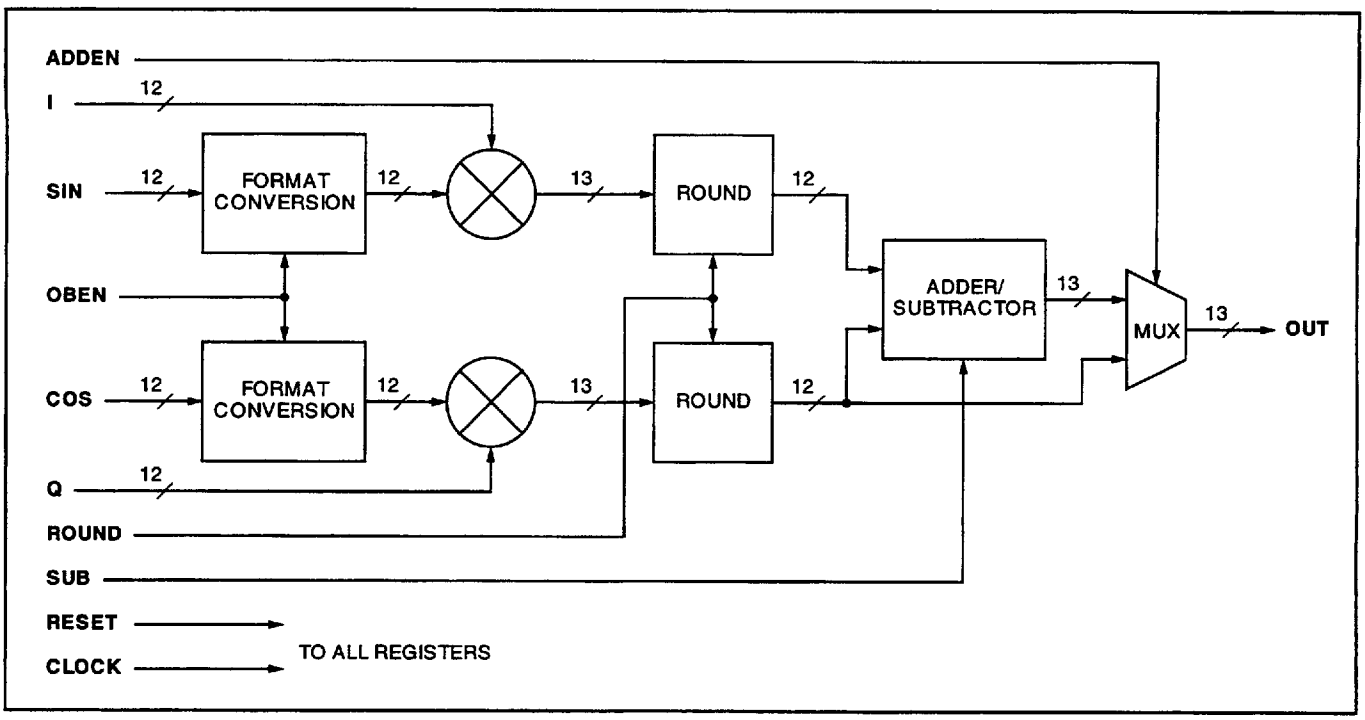
FEATURES

- **60 MHz THROUGHPUT CAPABILITY**
- **12-BIT INPUTS**
- **OFFSET BINARY OR TWO'S COMPLEMENT INPUTS AT NCO PORTS**
- **TWO'S COMPLEMENT OR UNSIGNED INPUTS AT MODULATION PORTS**
- **PRODUCTS CAN BE ADDED OR SUBTRACTED**
- **Q OUTPUT AVAILABLE INDIVIDUALLY**
- **12-BIT ROUNDED OR TRUNCATED PRODUCTS**

FUNCTIONAL DESCRIPTION

The STEL-1130 Quadrature Amplitude Modulator is intended to be used to amplitude modulate the output of a Numerically Controlled Oscillator (NCO). Quadrature Amplitude Modulation (QAM), also known as Vector Modulation, can be produced with a suitable NCO, such as the STEL-1172B and the STEL-1177. The STEL-1130 is cascaded with the outputs of the NCO, resulting in modulated digitized signals suitable for digital to analog conversion or digital signal processing. The format of the signals at the NCO input (**SIN, COS**) ports can be either offset binary or two's complement, making the STEL-1130 compatible with most NCOs. The format of the signals at the modulation (**I, Q**) ports can be either two's complement or unsigned magnitude, allowing the STEL-1130 to be used for both suppressed carrier and unsuppressed carrier modulation. The quadrature modulation capability also makes it suitable for single sideband (SSB) suppressed carrier modulation, as well as QAM modulation in data modems.

BLOCK DIAGRAM



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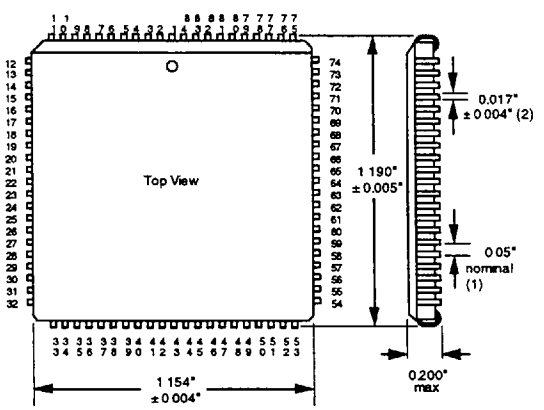
PIN CONFIGURATION

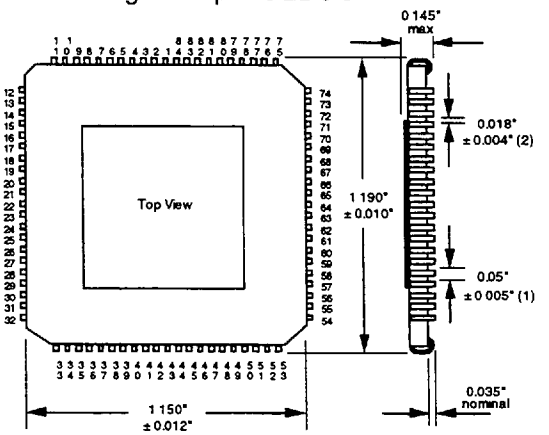
Package: 84 pin PLCC
Thermal coefficient, θ_{ja} = 36°C/W

Package: 84 pin CLDCC
Thermal coefficient, θ_{ja} = 34°C/W

Package: 84-pin PLCC



Package: 84-pin CLDCC



Notes: (1) Tolerances on pin spacing are not cumulative.
(2) Dimensions apply at seating plane.
(3) PLCC and CLDCC packages have different corners and may not fit into sockets designed for the other type. Universal sockets are available without alignment locators.

PIN CONNECTIONS

1	I_6	18	SIN_{10}	35	COS_9	52	SUB	69	I.C.
2	I_7	19	SIN_{11}	36	COS_{10}	53	V_{SS}	70	V_{SS}
3	I_8	20	V_{SS}	37	COS_{11}	54	V_{DD}	71	OUT_{11}
4	I_9	21	CLK	38	Q_0	55	OUT_0	72	OUT_{12}
5	I_{10}	22	V_{SS}	39	Q_1	56	OUT_1	73	I.C.
6	I_{11}	23	RESET	40	Q_2	57	I.C.	74	V_{DD}
7	SIN_0	24	V_{SS}	41	Q_3	58	V_{SS}	75	ADDEN
8	SIN_1	25	COS_0	42	Q_4	59	OUT_2	76	ROUND
9	SIN_2	26	COS_1	43	V_{SS}	60	OUT_3	77	OBEN
10	SIN_3	27	COS_2	44	Q_5	61	OUT_4	78	I_0
11	V_{DD}	28	COS_3	45	Q_6	62	OUT_5	79	I_1
12	SIN_4	29	COS_4	46	Q_7	63	OUT_6	80	I_2
13	SIN_5	30	COS_5	47	Q_8	64	V_{SS}	81	I_3
14	SIN_6	31	COS_6	48	Q_9	65	OUT_7	82	I_4
15	SIN_7	32	V_{DD}	49	Q_{10}	66	OUT_8	83	I_5
16	SIN_8	33	COS_7	50	Q_{11}	67	OUT_9	84	V_{SS}
17	SIN_9	34	COS_8	51	V_{SS}	68	OUT_{10}		

Note: I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.
N.C. denotes No Connection. Can be used for vias.

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FUNCTION BLOCK DESCRIPTION

FORMAT CONVERSION BLOCKS

These blocks are used to convert the format of the input signals on the SIN_{11-0} and COS_{11-0} input busses from offset binary to the two's complement format used internally when the **OBEN** signal is set high.

MULTIPLIER BLOCKS

The multiplier blocks form the core of the QAM function. The two 12-bit signed inputs to each multiplier produce a 23-bit product, but this is truncated in the multipliers and only the 13 most significant bits are actually generated. The two 12-bit by 12-bit multipliers are pipelined and start a new 13-bit product every clock cycle. As a result, the STEL-1130 has a maximum throughput rate of 60 MHz.

ROUNDING BLOCKS

The two rounding blocks modify the 13-bit products from the multipliers to produce 12-bit rounded products when the **ROUND** signal is set high. The products will be truncated to 12 bits when **ROUND** is set low.

ADD/SUBTRACT BLOCK

This block is used to add or subtract the products from the multipliers. The resulting 13-bit sum-of-products is brought out on the OUT_{12-0} bus in Two's Complement. Note that when **ADDEN** is set low the output is the 12-bit Q*COS signal, in which case the MSB (OUT_{12}) will be invalid.

MUX BLOCK

This block selects the data brought out on the OUT_{12-0} bus, depending on the state of the **ADDEN** input. When this signal is set high the function available at the OUT_{12-0} bus is $I*SIN \pm Q*COS$, and when it is set low the function available is Q*COS.

INPUT SIGNALS

RESET

The **RESET** input is asynchronous and active low, and clears all the registers in the device. When **RESET** goes low, all registers are cleared within 20 nsecs, and normal operation will resume after this signal returns high. The data on the OUT_{12-0} bus will remain at zero for 18 clock cycles after **RESET** returns high.

CLOCK

All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should be nominally a square wave at a maximum frequency of 60 MHz. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 5 nanoseconds.

I_{11} through I_0

Signals on the 12-bit I_{11-0} bus are multiplied by the signals on the SIN_{11-0} bus to form a 13-bit truncated product. This product is then rounded or truncated to a 12-bit product before being loaded into the Add/Subtract and Mux Blocks. There is a 16/18-cycle pipeline delay from when a value is applied at the I_{11-0} bus to the result of this value appearing at the output (see **ADDEN**).

Q_{11} through Q_0

Signals on the 12-bit Q_{11-0} bus are multiplied by the signals on the COS_{11-0} bus to form a 13-bit truncated product. This product is then rounded or truncated to a 12-bit product before being loaded into the Add/Subtract Block. There is a 16/18-cycle pipeline delay from when a value is applied at the Q_{11-0} bus to the result of this value appearing at the output (see **ADDEN**).

SIN_{11} through SIN_0

Signals on the 12-bit SIN_{11-0} bus are multiplied by the signals on the I_{11-0} bus to form a 13-bit truncated product. This product is then rounded or truncated to a 12-bit product before being loaded into the Add/Subtract and Mux Blocks. There is a 16/18-cycle pipeline delay from when a value is applied at the SIN_{11-0} bus to the result of this value appearing at the output (see **ADDEN**).

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COS_{11} through COS_0

Signals on the 12-bit COS_{11-0} bus are multiplied by the signals on the Q_{11-0} bus to form a 13-bit truncated product. This product is then rounded or truncated to a 12-bit product before being loaded into the Add/ Subtract Block. There is a 16/18-cycle pipeline delay from when a value is applied at the COS_{11-0} bus to the result of this value appearing at the output (see ADDEN).

OBEN

The Offset Binary Enable signal controls the function of the Format Conversion Blocks. When this signal is set high the signals on the SIN_{11-0} and COS_{11-0} busses are converted from Offset Binary Format to the Two's Complement format used internally. Offset Binary is the format of the output signals of most NCOs, including both the STEL-1172B and the STEL-1177. When it is set low no conversion takes place, allowing signals in Two's Complement format to be used on these busses.

ROUND

The **ROUND** signal controls the function of the Rounding Blocks. When this signal is set high the 13-bit products from the two multipliers are rounded to 12-bit products, and when it is set low the products are truncated to 12 bits. If this signal is changed during operation of the device the result will appear at the output after a 5 clock cycle delay.

SUB

The **Sub**tract signal controls the function of the Add/ Subtract Block. When this signal is set high the function performed is **I*SIN – Q*COS**, and when it is set low the function performed is **I*SIN + Q*COS**. If this signal is changed during operation of the device the result will appear at the output after a 4 clock cycle delay.

ADDEN

The **Add Enable** signal controls the function of the Mux Block. When this signal is set high the function available at the OUT_{12-0} bus is **I*SIN ± Q*COS**, and when it is set low the function available is **Q*COS**. When **ADDEN** is set low the output is the 12-bit **Q*COS** signal, in which case the MSB (OUT_{12}) will be invalid. If this signal is changed during operation of the device the result will appear at the output after a 1 clock cycle delay. Note that when **ADDEN** is set high the pipeline delays from the SIN_{11-0}, COS_{11-0}, I_{11-0}, and Q_{11-0}, inputs is increased from 16 to 18 clock cycles.

OUTPUT SIGNALS

OUT_{12-0}

The signal appearing on the OUT_{12-0} output bus is the output of the Mux Block. When **ADDEN** is set low the output is the 12-bit **Q*COS** signal, in which case the MSB (OUT_{12}) will be invalid. The output data format is Two's Complement at all times.

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{ss}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125 –65 to +150	°C (Plastic package) °C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to VDD + 0.3	volts
I_i	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 5% +5 ± 10%	Volts (Commercial Conditions) Volts (Military Conditions)
T_a	Operating Temperature (Ambient)	0 to +70 –55 to +125	°C (Commercial Conditions) °C (Military Conditions)

D.C. CHARACTERISTICS

(Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C, Military

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			2.0	mA/MHz	f_{CLK} = 60 MHz
$V_{IH(min)}$	High Level Input Voltage					
	Commercial Operating Conditions	2.0			volts	Logic '1'
	Military Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IL(max)}$	Low Level Input Current	–130	–45	–15	µA	All inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –4.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +4.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

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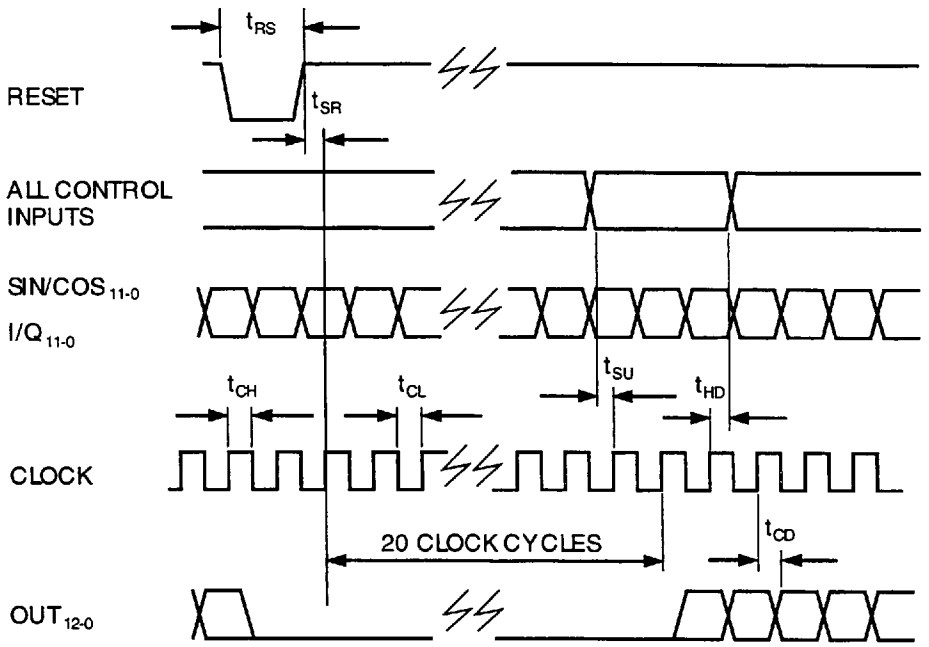
TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS

(Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C, Military

Symbol	Parameter	Commercial			Military			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{RS}	RESET pulse width	20			25			nsec.	
t_{SR}	RESET to CLOCK Setup	7			9			nsec.	
t_{CH}	CLOCK High	5			6			nsec.	
t_{CL}	CLOCK Low	5			6			nsec.	
t_{SU}	ADDEN, OBEN, ROUND, SUB, SIN_{11-0} or COS_{11-0} to CLOCK Setup	5			5			nsec.	
t_{HD}	ADDEN, OBEN, ROUND, SUB, SIN or COS to CLOCK Hold	6			7			nsec.	
t_{CD}	CLOCK to OUT_{11-0} Delay	3		12	2		20	nsec.	C_L = 15 pF

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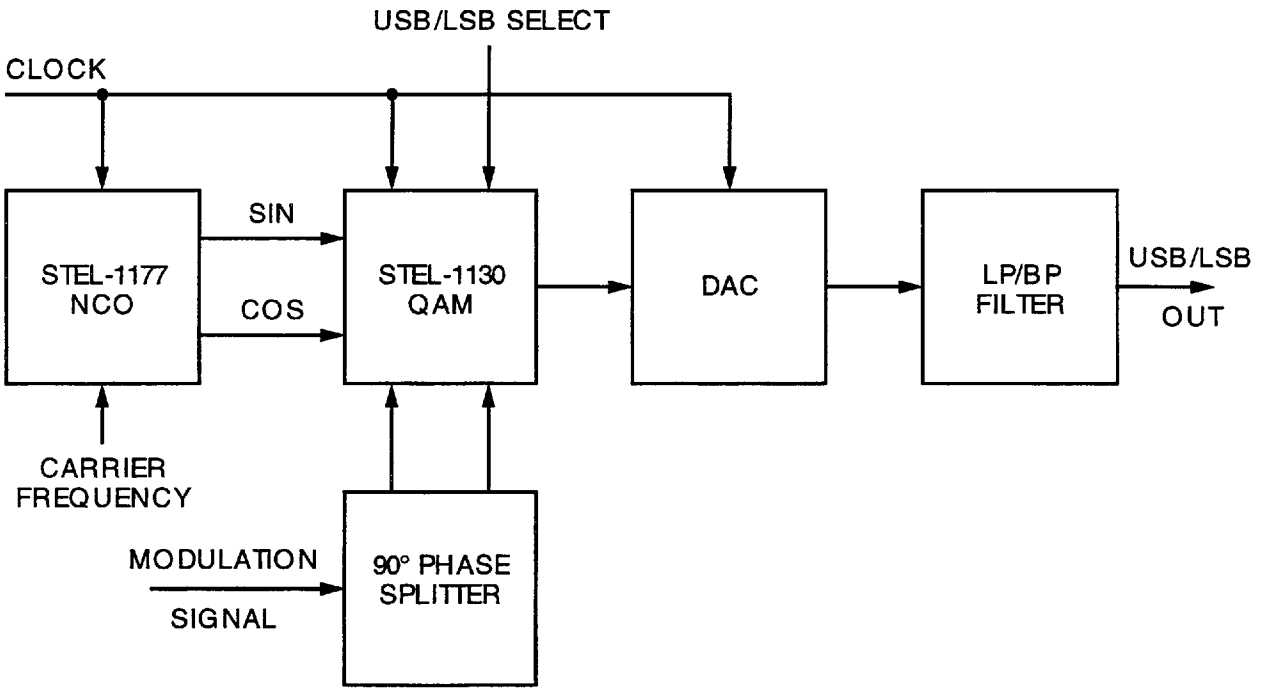
TYPICAL APPLICATION - SINGLE SIDEBAND MODULATOR



By utilizing the trigonometric identities:

$$\sin(\omega_c) \cdot \sin(\omega_m) = {}^1/_2 \cos(\omega_c - \omega_m) - {}^1/_2 \cos(\omega_c + \omega_m)$$

and $$\cos(\omega_c) \cdot \cos(\omega_m) = {}^1/_2 \cos(\omega_c - \omega_m) + {}^1/_2 \cos(\omega_c + \omega_m)$$

it is possible to generate either an upper sideband ($\omega_c + \omega_m$) or lower sideband ($\omega_c - \omega_m$) signal directly without any need for a sharp cutoff filter to eliminate the unwanted sideband. The sum of the products gives the lower sideband signal and the difference of the products gives the upper sideband. Thus it is even possible to switch the sideband generated simply by toggling the SUB control signal on the STEL-1130, a feat not possible in conventional SSB modulators without using dual sideband filters.

FOR FURTHER INFORMATION

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