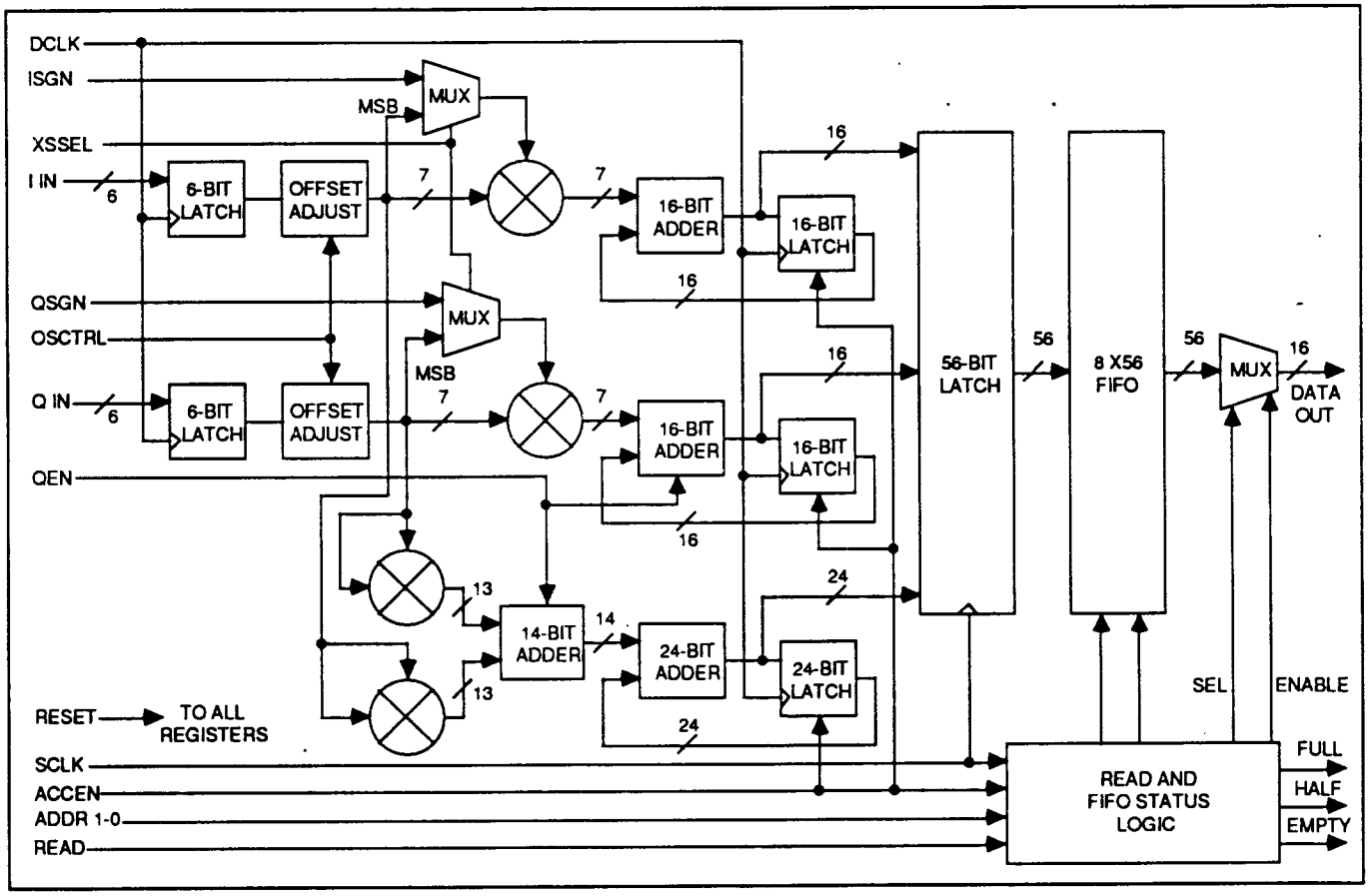
FEATURES

- PROVIDES 16-BIT IN-PHASE AND QUADRATURE AMPLITUDES OR MAGNITUDES
- PROVIDES 24-BIT ACCUMULATED POWER VALUE
- 6-BIT INPUTS, TWO'S COMPLEMENT OR OFFSET TWO'S COMPLEMENT
- OPERATES WITH BPSK OR QPSK SIGNALS WITH REAL-TIME SWITCHING
- 15 MHz SAMPLING RATE
- ASYNCHRONOUS MICROPROCESSOR INTERFACE WITH THREE-STATE OUTPUTS
- 68 PIN CERAMIC PGA PACKAGE

The STEL-2330 SQE provides the front-end processing for estimating E_b/N_o (bit-energy to noise density ratio) of real time data at speeds up to 15 Msamples/sec. This device may be used in conjunction with a host processor to obtain optimal statistical estimates of the means and variances of the in-phase and quadrature phase signals, allowing E_b/N_o to be calculated for both BPSK and QPSK signals. Both single estimates and running averages can be calculated, with single estimate accumulations ranging from 1 to 512 input samples.

Accumulators are provided for the averaged magnitudes (the absolute values) of both the I and Q channel signals, as well as the sum of the squares of both channels, which gives the total power level of the complex signal. E_b/N_o can be computed from these values. A rising edge on the **ACCEN** signal terminates these accumulations and transfers the current accumulator values into a FIFO which can hold up to eight sets of data values. This process clears the accumulators so that they are ready to start new accumulations when **ACCEN** goes low again. The data can be read out of the FIFO by means of the **READ** signal and the data to be read out is selected by the two address lines. Flags are provided to indicate the status of the FIFO, giving an indication of when it is full, half-full, or empty. The value of E_b/N_o can be calculated from the mean values of the magnitudes and squared magnitudes of the I and Q channel signals.

BLOCK DIAGRAM



INPUT SIGNALS

RESET
The **RESET** input is asynchronous and active low. When **RESET** goes low, all registers are cleared within 15 nsecs.

SCLK
All synchronous functions are referenced to the rising edge of the System Clock. The **SCLK** signal should nominally be a square wave at a maximum frequency of 70 MHz.

DCLK
The incoming data signals are latched into the input buffers on the rising edges of the Data Clock signal.

I IN_{5-0} and Q IN_{5-0}
The 6-bit **I IN_{5-0}** and **Q IN_{5-0}** busses are the inputs to the **I** and **Q** channels of the device, respectively. The signals can be presented in either two's complement or offset two's complement format. The formats are defined in the table:

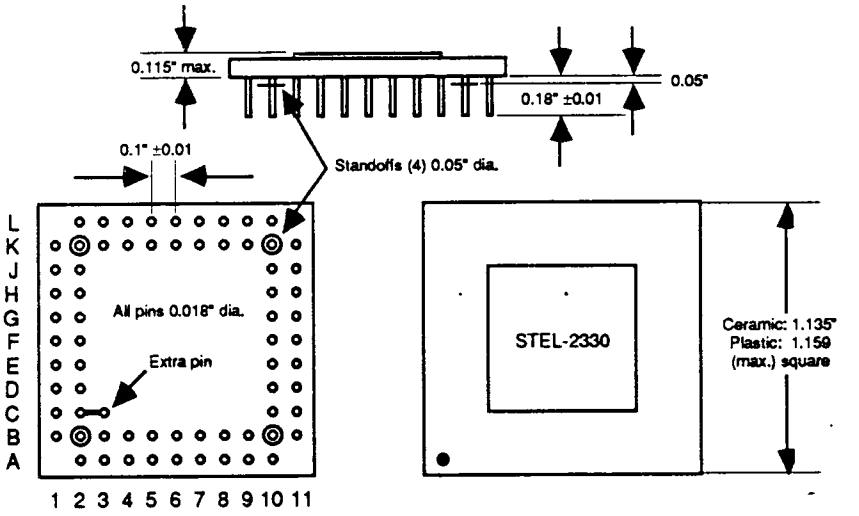
Input Data Code	Value	
	Two's comp. (OSCTRL=0)	Offset two's comp. (OSCTRL=1)
20	Most negative	Most negative
3F	–1 LSB	$-\frac{1}{2}$ LSB
00	Zero	$+\frac{1}{2}$ LSB
1F	Most positive	Most positive

QEN
When the **Q** Channel **En**able signal is set high both the I and Q channels of the system operate in a normal manner. When it is set low the Q channel input is disabled, and zero value data will be loaded into the Q accumulator and the Q channel of the $I^2 + Q^2$ accumulator.

OSCTRL
The formats of the data used on the **I IN_{0-5}** and **Q IN_{0-5}** busses is determined by the state of the **OSCTRL** input. When this

PIN CONFIGURATION

Package: 68 pin Ceramic PGA
Notes:
1. Tolerances on pin spacing are not cumulative.
2. Pins C2 and C3 (extra pin) are connected together.
3. I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.



Bottom View Top View

PIN CONNECTIONS

A2	V_{DD}	B7	FCLR	E10	$DATA_8$	J2	I.C.	L2	$Q\ IN_0$
A3	$I\ IN_0$	B8	$ADDR_1$	E11	$DATA_9$	J10	$DATA_3$	L3	$Q\ IN_2$
A4	$I\ IN_2$	B9	$DATA_{15}$	F1	SCLK	J11	$DATA_4$	L4	$Q\ IN_4$
A5	$I\ IN_4$	B10	V_{DD}	F2	V_{SS}	K1	V_{DD}	L5	BPSK
A6	V_{SS}	B11	V_{SS}	F10	V_{SS}	K2	V_{SS}	L6	V_{DD}
A7	I.C.	C1	I.C.	F11	V_{DD}	K3	$Q\ IN_1$	L7	HALF
A8	$ADDR_0$	C2	MAGSEL	G1	DCLK	K4	$Q\ IN_3$	L8	V_{DD}
A9	READ	C10	$DATA_{12}$	G2	V_{SS}	K5	$Q\ IN_5$	L9	$DATA_1$
A10	$DATA_{14}$	C11	$DATA_{13}$	G10	$DATA_6$	K6	V_{SS}	L10	V_{SS}
B1	IMAG	D1	OSCTRL	G11	$DATA_7$	K7	FULL		
B2	V_{SS}	D2	ACCEN	H1	V_{SS}	K8	EMPTY		
B3	$I\ IN_1$	D10	$DATA_{10}$	H2	V_{DD}	K9	$DATA_0$		
B4	$I\ IN_3$	D11	$DATA_{11}$	H10	V_{SS}	K10	V_{DD}		
B5	$I\ IN_5$	E1	V_{DD}	H11	$DATA_5$	K11	$DATA_2$		
B6	V_{DD}	E2	RESET	J1	QMAG				

input is low the input data is treated as two's complement format, and when high the data is treated as offset two's complement format. The offset effectively adds 0.5 to the LSB of the signal, effectively increasing it from a 6-bit word to a 7-bit word.

XSSEL
In normal operation the External Sign **Select** signal will be set low and the signs of the **I IN** and **Q IN** signals will be selected by the multiplexer. The magnitudes of the **I IN** and **Q IN** signals will then be multiplied by their own signs to generate absolute values. When **XSSEL** is set high the **ISGN** and **QSGN** signals will be selected by the multiplexer. The magnitudes of the **I IN** and **Q IN** signals will then be multiplied by the **ISGN** and **QSGN** signals.

ISGN and QSGN
The **ISGN** and **QSGN** inputs allow alternative sign values to be used to produce the absolute values of the **I IN** and **Q IN** signals. e.g., to produce despreading in a direct sequence spread spectrum system. The alternative sign values are loaded on these pins when **XSSEL** is set high.

ACCEN
When the **Accumulator Enable** signal is low the input signals are accumulated in the three accumulators. On the rising edge of this signal the contents of the accumulators are transferred to the FIFO and the accumulators are cleared. When **ACCEN** goes low again a new set of accumulations will start. **ACCEN** should be held high for a minimum of two cycles of **SCLK** after each rising edge.

$ADDR_{0-1}$
The two address lines allow the 54 bits of output data to be read out on the 16-bit data bus. The data is addressed as shown in the table below:

A1	A0	Data
0	0	Accumulation of I channel
0	1	Accumulation of Q channel
1	0	$I^2 + Q^2$ accumulation (16 LSBs)
1	1	$I^2 + Q^2$ accumulation (8 LSBs)

The data appears on bits 7-0 of the data bus when the address is 11. This data should be read out last, because on the rising edge of the **READ** signal the FIFO contents will be shifted forward if the address is 11.

READ
The **READ** input controls the status of the **$DATA_{15-0}$** bus. When READ is high the bus will be in a high impedance state, and no data will be available. When **READ** is low the data bus is active and data can be read from the FIFO. The rising edge of **READ** will cause the FIFO contents to be shifted forward if the address bus is set at 11 at the time.

FCLR
When the **FIFO Clear** signal is set low it will cause the FIFO to be cleared. The clearing will occur immediately and will not be synchronized to either of the clocks.

$TEST_1$, $TEST_2$
These two signals are used for test purposes only and should normally remain high at all times.

OUTPUT SIGNALS

$DATA_{15-0}$
All the output data is multiplexed onto the 16-bit **$DATA_{15-0}$** bus. The outpout data presented on this bus is selected by the adress lines **$ADDR_{1-0}$**. The buss will be in a high impedance state at all times except when the **READ** signal is low.

FULL
The **FULL** signal goes low to indicate that the FIFO is full, i.e. it contains eight 56-bit data words. When this happens any further data written into the FIFO, i.e., whenever there is a rising edge on ACCEN, will overwrite the last data word in the FIFO.

HALF
The **HALF** signal goes low to indicate that the FIFO is half full, i.e., it contains four or more data words.

EMPTY
The **EMPTY** signal goes low to indicate that the FIFO is empty, i.e., it contains no more data words.

FOR FURTHER INFORMATION
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