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# 2M x 8 SRAM MODULE

## SYS82000RKXC - 70/85/10/12

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### Description

The SYS82000RKXC is a plastic 16Mbit Static RAM Module housed in a standard 38 pin Single In-Line package organised as 2M x 8 with access times of 70, 85,100, or 120 ns.

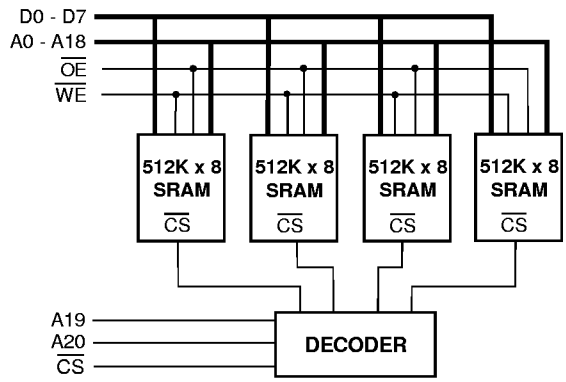
The module is constructed using four 512Kx8 SRAMs in TSOPII packages mounted onto an FR4 epoxy substrate. This offers an extremely high PCB packing density.

The device is offered in standard and low power versions, with the -L module having a low voltage data retention mode for battery backed applications.

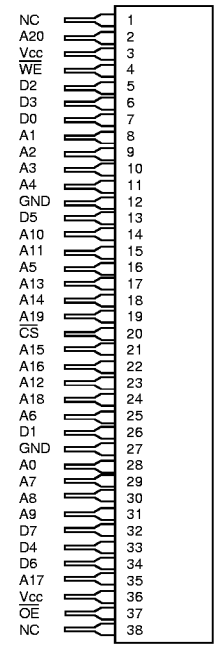
### Features

- Access Times of 70/85/100/120 ns.
- Low Power Disapation:
  Operating 600 mW (Max.)
  Standby-L Version 1.1 mW (Max.)
- 5 Volt Supply ± 10%.
- Completely Static Operation.
- Low Voltage $V_{CC}$ Data Retention.
- On-board Decoding & Decoupling Capacitors.
- 38 Pin Single-In-Line package (SIP).
- Upgrade path to SYS84000RKXC (32Mbits).

### Block Diagram




### Pin Definition




Pin 38 is A21 on the SYS84000RKXC upgrade module.

### Pin Functions

| | |
|---|---|
| *Address Inputs* | **A0 ~ A20** |
| *Data Input/Output* | **D0 ~ D7** |
| *Chip Select* | **$\overline{CS}$** |
| *Write Enable* | **$\overline{WE}$** |
| *Output Enable* | **$\overline{OE}$** |
| *No Connect* | **NC** |
| *Power (+5V)* | **$V_{cc}$** |
| *Ground* | **GND** |

### Package Details

Plastic 38 pin Single-In-Line (SIP)

## DC OPERATING CONDITIONS

### Absolute Maximum Ratings (1)

| *Parameter* | *Symbol* | *min* | *typ* | *max* | *unit* |
|---|---|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | -0.3 | - | +7 | V |
| Power Dissipation | $P_T$ | - | - | 4.0 | W |
| Storage Temperature | $T_{STG}$ | -55 | - | +125 | °C |

Notes :

(1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) $V_T$ can be -3.0 V pulse of less than 30 ns.

### Recommended Operating Conditions

| *Parameter* | *Symbol* | *min* | *typ* | *max* | *unit* |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | - | Vcc+0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | - | 0.8 | V |
| Operating Temperature | $T_A$ | 0 | - | 70 | °C |
| | $T_{AI}$ | -40 | - | 85 | °C (I) |

### DC Electrical Characteristics ($V_{CC}$=5V±10%) $T_A$ 0 to 70°C

| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|---|
| I/P Leakage Current | $I_{LI}$ | $V_{IN}$ = GND to $V_{CC}$ | -4 | - | 4 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CS}$ = $V_{IH}$, $V_{I/O}$ = GND to $V_{CC}$ | -4 | - | 4 | µA |
| Operating Supply Current | $I_{CC}$ | $\overline{CS}$ = $V_{IL}$, min cycle, Duty = 100% | - | - | 109 | mA |
| Standby Supply Current TTL levels | $I_{SB1}$ | $\overline{CS}$ = $V_{IH}$ | - | - | 12 | mA |
| -L Version | $I_{SB2}$ | $\overline{CS}$ = $V_{CC}$-0.2V, 0.2 > $V_{IN}$ > $V_{CC}$-0.2V | - | - | 200 | µA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 2.1mA | - | - | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1.0mA | 2.4 | - | - | V |

### Capacitance ($V_{CC}$=5V±10%, $T_A$=25°C) Note: Capacitance calculated, not measured.

| *Parameter* | *Symbol* | *Test Condition* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|
| Input Capacitance ($\overline{CS}$,A19,A20) | $C_{IN1}$ | $V_{IN}$ = 0V | - | 8 | pF |
| Input Capacitance (A0-18,$\overline{OE}$,$\overline{WE}$) | $C_{IN2}$ | $V_{IN}$ = 0V | - | 32 | pF |
| I/O Capacitance | $C_{I/O}$ | $V_{I/O}$ = 0V | - | 10 | pF |

## Operation Truth Table

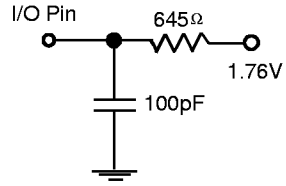
| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | DATA PINS | SUPPLY CURRENT | MODE |
|---|---|---|---|---|---|
| H | X | X | High Impedance | $I_{SB1}$ , $I_{SB2}$ | Standby |
| L | L | H | Data Out | $I_{CC}$ | Read |
| L | X | L | Data In | $I_{CC}$ | Write |
| L | H | H | High Impedance | $I_{CC}$ | Output Disabled |

Notes : H = $V_{IH}$ : L =$V_{IL}$ : X = $V_{IH}$ or $V_{IL}$

## AC Test Conditions

* Input pulse levels: 0 V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* $V_{CC}$ = 5V± 10%

## Output Load




## Low $V_{cc}$ Data Retention Characteristics - L Version Only ($T_{OP}$ = 0°C to 70°C)

| Parameter | Symbol | Test Condition | -L Part min | typ | max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ for Data Retention | $V_{DR}$ | $\overline{CS}\geq V_{CC}$-0.2V<br>0.2V≥$V_{in}$≥$V_{cc}$-0.2 | 2.0 | - | - | V |
| Data Retention Current | $I_{CCDR}$ | $V_{CC}$=3.0V,$\overline{CS}$=$V_{CC}$-0.2V,0.2V≥$V_{in}$≥$V_{cc}$-0.2 | - | - | 400 | µA |
| Chip Deselect to Data Ret. Time | $t_{CDR}$ | See Retention Waveform | 0 | - | - | ns |
| Operation Recovery Time | $t_R$ | See Retention Waveform | 5 | - | - | ms |

## AC OPERATING CONDITIONS

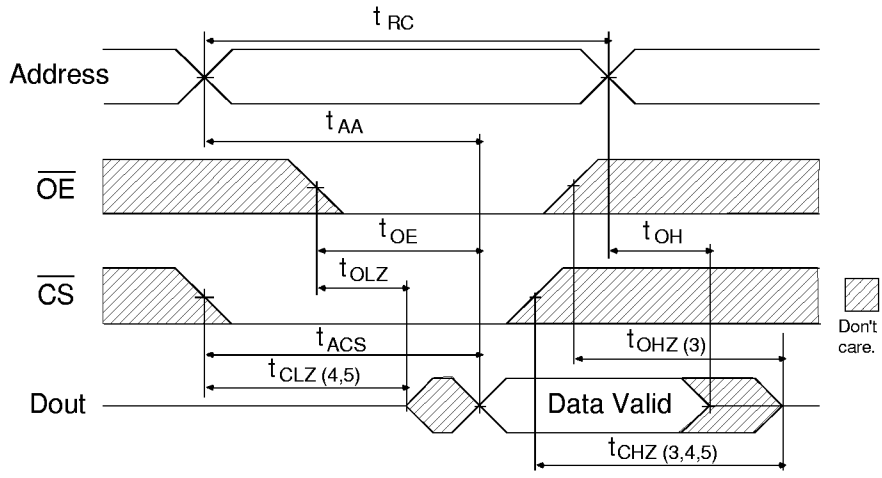
### Read Cycle

| | | -70 | | -85 | | -10 | | -12 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | min | max | min | max | min | max | min | max | Unit |
| Read Cycle Time | $t_{RC}$ | 70 | - | 85 | - | 100 | - | 120 | - | ns |
| Address Access Time | $t_{AA}$ | - | 70 | - | 85 | - | 100 | - | 120 | ns |
| Chip Select Access Time | $t_{ACS}$ | - | 70 | - | 85 | - | 100 | - | 120 | ns |
| Output Enable to Output Valid | $t_{OE}$ | - | 40 | - | 45 | - | 50 | - | 55 | ns |
| Output Hold from Address Change | $t_{OH}$ | 10 | - | 10 | - | 10 | - | 10 | - | ns |
| Chip Selection to Output in Low Z | $t_{CLZ}$ | 10 | - | 10 | - | 10 | - | 10 | - | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$ | 5 | - | 5 | - | 5 | - | 5 | - | ns |
| Chip Deselection to O/P in High Z | $t_{CHZ}$ | 0 | 30 | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| Output Disable to Output in High Z | $t_{OHZ}$ | 0 | 30 | 0 | 30 | 0 | 35 | 0 | 40 | ns |

### Write Cycle

| | | *-70* | | *-85* | | *-10* | | *-12* | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | min | max | min | max | min | max | min | max | Unit |
| Write Cycle Time | $t_{WC}$ | 70 | - | 85 | - | 100 | - | 120 | - | ns |
| Chip Selection to End of Write | $t_{CW}$ | 60 | - | 75 | - | 80 | - | 100 | - | ns |
| Address Setup Time | $t_{AS}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Address Valid to End of Write | $t_{AW}$ | 60 | - | 75 | - | 80 | - | 100 | - | ns |
| Write Pulse Width | $t_{WP}$ | 55 | - | 65 | - | 70 | - | 80 | - | ns |
| Write Recovery Time | $t_{WR}$ | 5 | - | 5 | - | 5 | - | 5 | - | ns |
| Write to Output in High Z | $t_{WHZ}$ | 0 | 25 | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| Data to Write Time Overlap | $t_{DW}$ | 30 | - | 35 | - | 40 | - | 45 | - | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Output active from end of write | $t_{OW}$ | 5 | - | 5 | - | 5 | - | 5 | - | ns |

## Read Cycle Timing Waveform (1,2)




### AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

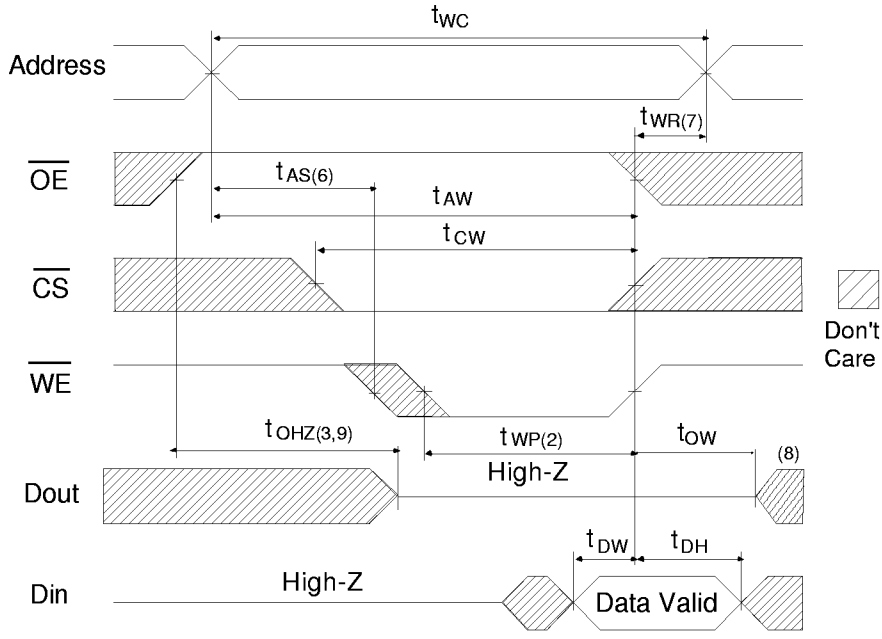
(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) $t_{CHZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

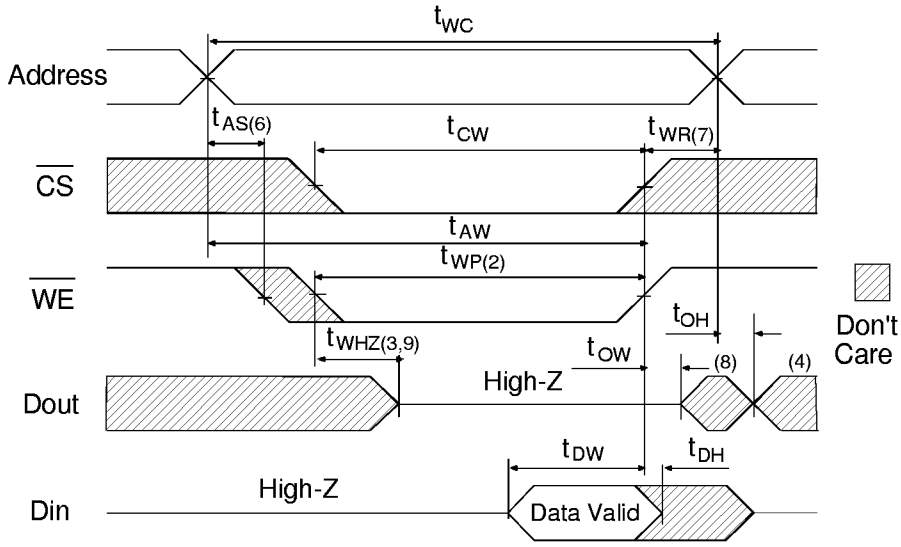
(4) At any given temperature and voltage condition, $t_{CHZ}$ (max) is less than $t_{CLZ}$ (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

## Write Cycle No.1 Timing Waveform (1,4)



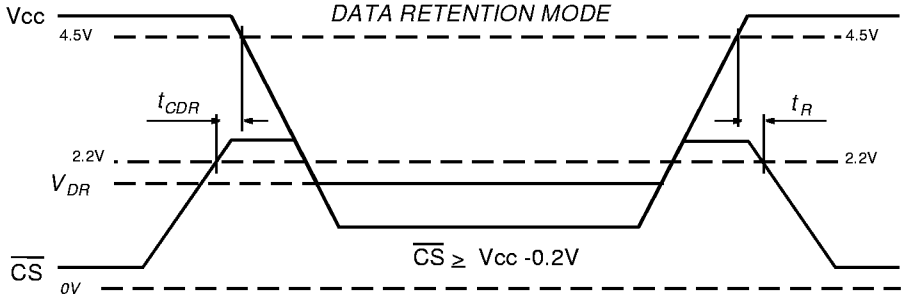
## Write Cycle No.2 Timing Waveform (1,5)




### AC Write Characteristics Notes

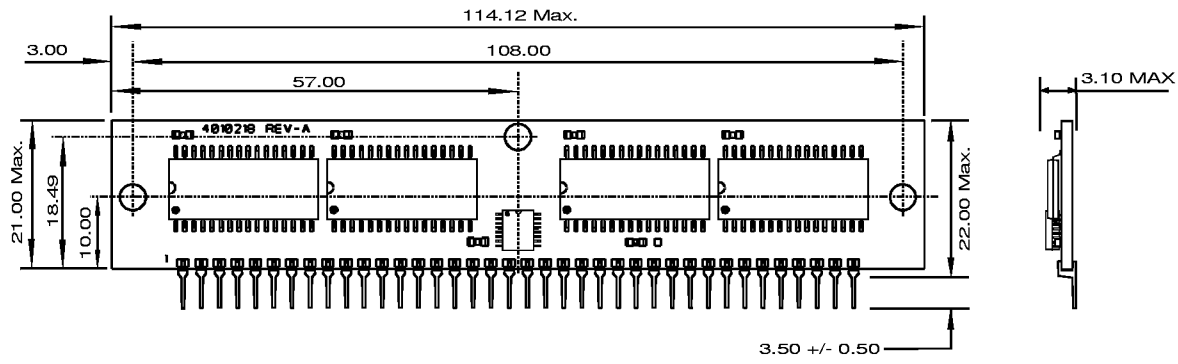
(1) All write cycle timing is referenced from the last valid address to the first transition address.
(2) All writes occur during the overlap of $\overline{CS}$ and $\overline{WE}$ low.
(3) If $\overline{OE}$, $\overline{CS}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.
(4) Dout is the Read data of the new address.
(5) $\overline{OE}$ is continuously low.
(6) Address is valid prior to or coincident with $\overline{CS}$ and $\overline{WE}$ low, too avoid inadvertant writes.
(7) $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
(8) When $\overline{CS}$ is low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.
(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

## Data Retention Waveform



## Package Information Dimensions in mm

### Plastic 38 Pin Single-In-Line (SIP)




## Ordering Information

**SYS82000RKXCLI - 70**

| | | |
|---|---|---|
| Speed | 70 | = 70 ns |
| | 85 | = 85 ns |
| | 10 | = 100 ns |
| | 12 | = 120 ns |
| Temperature Range | Blank | = Commercial Temperature |
| | I | = Industrial Temperature |
| Power Consumption | Blank | = Standard Part |
| | L | = Low Power Part |
| Package | RKXC | = Plastic 38 pin SIP |
| Organization | 82000 | = 2M x 8 |
| Memory Type | SYS | = Static RAM |

**Note :**

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Our products are subject to a constant process of development. Data may be changed at any time without notice.

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