T7274A Quad Differential Line Driver

Features

- Four line drivers per package
- Complementary outputs from each line driver
- 24-mA drive capability
- High output drive for 100-Ω, 110-Ω, and 150-Ω lines
- 2.0-ns minimum and 4.75-ns maximum propagation delays
- 0.1-ns output skew, typical
- 140 Mb/s data rate
- 300-mW maximum power dissipation
- Single 5 V supply
- 0 to 85 °C operating temperature

Description

The T7274A Quad Differential Line Driver integrated circuit is a single-input-to-balanced-output converter that drives differential transmission lines. The input requires typical CMOS signals, and the output has typical CMOS voltage swings and can drive 100-Ω, 110-Ω, and 150-Ω twisted pair lines through a resistor attenuation network.

This CMOS device is similar to the general-trade 26LS31 device; however, it has decreased power consumption and generates lower levels of electromagnetic interference (EMI).

The T7274A line driver is compatible with many line receivers, including the AT&T T7275B and 41LF devices and the general-trade 26LS32 device. The quad differential line driver is available in a 16-pin plastic DIP and small-outline J-lead (SOJ) package.

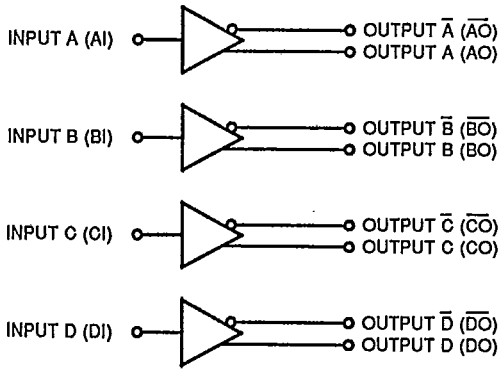

Figure 1. Logic Diagram

T-75-45-0

User Information

Pin Descriptions

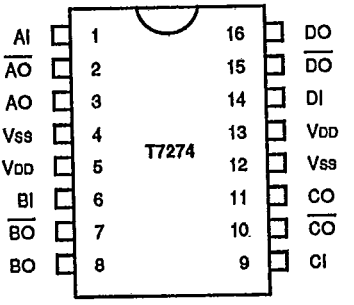

Figure 2. Pin Function Diagram

Table 1. Pin Descriptions

Symbol	Type	Name
AI	I	A-line driver input
$\overline{AO}$	O	Inverted A-line driver output
AO	O	A-line driver output
BI	I	B-line driver input
$\overline{BO}$	O	Inverted B-line driver output
BO	O	B-line driver output
CI	I	C-line driver input
$\overline{CO}$	O	Inverted C-line driver output
CO	O	C-line driver output
DI	I	D-line driver input
$\overline{DO}$	O	Inverted D-line driver output
DO	O	D-line driver output
VSS	—	Ground pins
VDD	—	5 V supply pins

Characteristics

Electrical Characteristics

T_A = 0 to 85 °C, V_{DD} = 5.0 V ± 0.25 V

Parameter	Sym	Min	Typ	Max	Unit
Output voltages, V_{DD} = 4.75 V:*					
low, I_{OL} = +12.5 mA	V_{OL}	—	—	0.5	V
high, I_{OH} = –12.5 mA	V_{OH}	4.25	—	—	V
Output impedance	—	—	20	40	Ω
Input voltages:**					
low	V_{IL}	—	—	1.0	V
high	V_{IH}	3.75	—	—	V
threshold	V_{TH}	—	$V_{DD}/2$	—	V
Output currents, short-circuit	I_{SC}	–100	—	–200	mA
Input currents, V_{DD} = 5.25 V:					
low, V_{IN} = 0.5 V	I_{IL}	—	—	–1.0	μA
high, V_{IN} = 5.25 V	I_{IH}	—	—	100	μA
Power supply current, V_{DD} = 5.25 V:					
DC conditions	I_{DD}	—	0.25	0.5	mA
100 Mb/s	I_{DD}	—	75	80	mA

* I_{OL} and I_{OH} can increase to 25 mA. The reduced V_{OL} and V_{OH} are computed from the output impedance.
** Each input has typically 100 kΩ to V_{SS}. Thus, a no connect input is pulled low.

T-75-45-07

Maximum Ratings

Power supply voltage (V_{DD}) ..... 7.0 V
Ambient operating temperature (T_A) range ..... 0 to 85 °C
Storage temperature (T_{stg}) range ..... −40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

T_A = 0 to 85 °C, V_{DD} = 5.0 V ± 0.25 V, test circuit connected to output (see Figure 3).*

Symbol	Description	Min	Typ	Max	Unit
	Propagation delay, input to output:				
t_{PD}	AO, BO, CO, and DO	2.0	3.0	4.75	ns
$t_{\overline{PD}}$	$\overline{AO}$, $\overline{BO}$, $\overline{CO}$, and $\overline{DO}$	2.0	3.0	4.75	ns
tskew	Difference between propagation delays $\lvert t_{PD} - t_{\overline{PD}} \rvert$	—	100	300	ps
t_{PWD}	Pulse width distortion, $\lvert t_{IN} - t_{OUT} \rvert$	—	200	500	ps
t_r, t_f	Rise and fall time (10% to 90%)	—	1.5	3.0	ns
t_{IN}	Input pulse width	7	—	—	ns

* Input rise and fall times (10% to 90%) of less than 4 ns are necessary to guarantee maximum propagation delay, pulse width distortion, and skew characteristics.

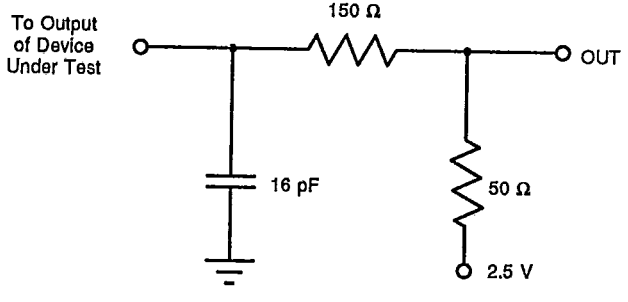

Figure 3. Timing Test Circuit

Timing Diagram

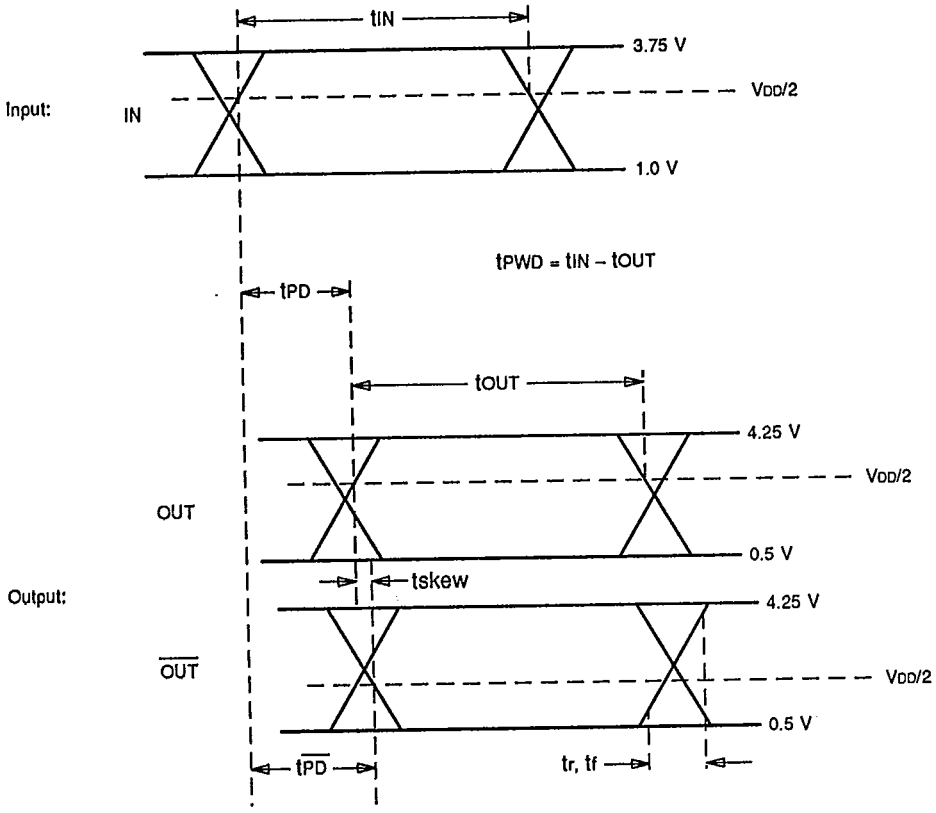

Figure 4. Timing Waveforms