

NEC**MOS INTEGRATED CIRCUIT**
 μ PD30450**VR4200™**
64-BIT MICROPROCESSOR**DESCRIPTION**

The μ PD30450 (VR4200) is one of NEC's RISC (Reduced Instruction Set Computer) microprocessors, VR series™, and is a high-performance 64-bit microprocessor employing the RISC architecture developed by MIPS.

The VR4200 is intended for high-performance, low-cost systems, and features low power dissipation and low cost to realize low-power application.

The detailed functions of the VR4200 are described in the following manual. Be sure to read this manual in designing your system.

• VR4200 User's Manual : IEU-1392

FEATURES

- Employment of RISC architecture developed by MIPS
- High-speed operation processing
 - 5-stage pipeline processing
 - Integer operation performance : 55 SPECint92
 - Floating-point operation performance : 30 SPECfp92
- 64-bit registers, integer operation unit, floating-point operation unit
- Instruction set compatible with VR4000™ series (conforming to MIPS-I/II/III)
- Internal operating frequency : 80 MHz (input clock : 40 MHz)
- Cache memory (instruction : 16 KB, data : 8 KB)
- Low power dissipation (1.5 W TYP.)
- Low power mode
- System interface compatible with VR4000PC™
- Supply voltage : 3.3 V

APPLICATION

- Work station of low-end model
- Battery-driven laptop or notebook type personal computers
- Embedded controller, etc.

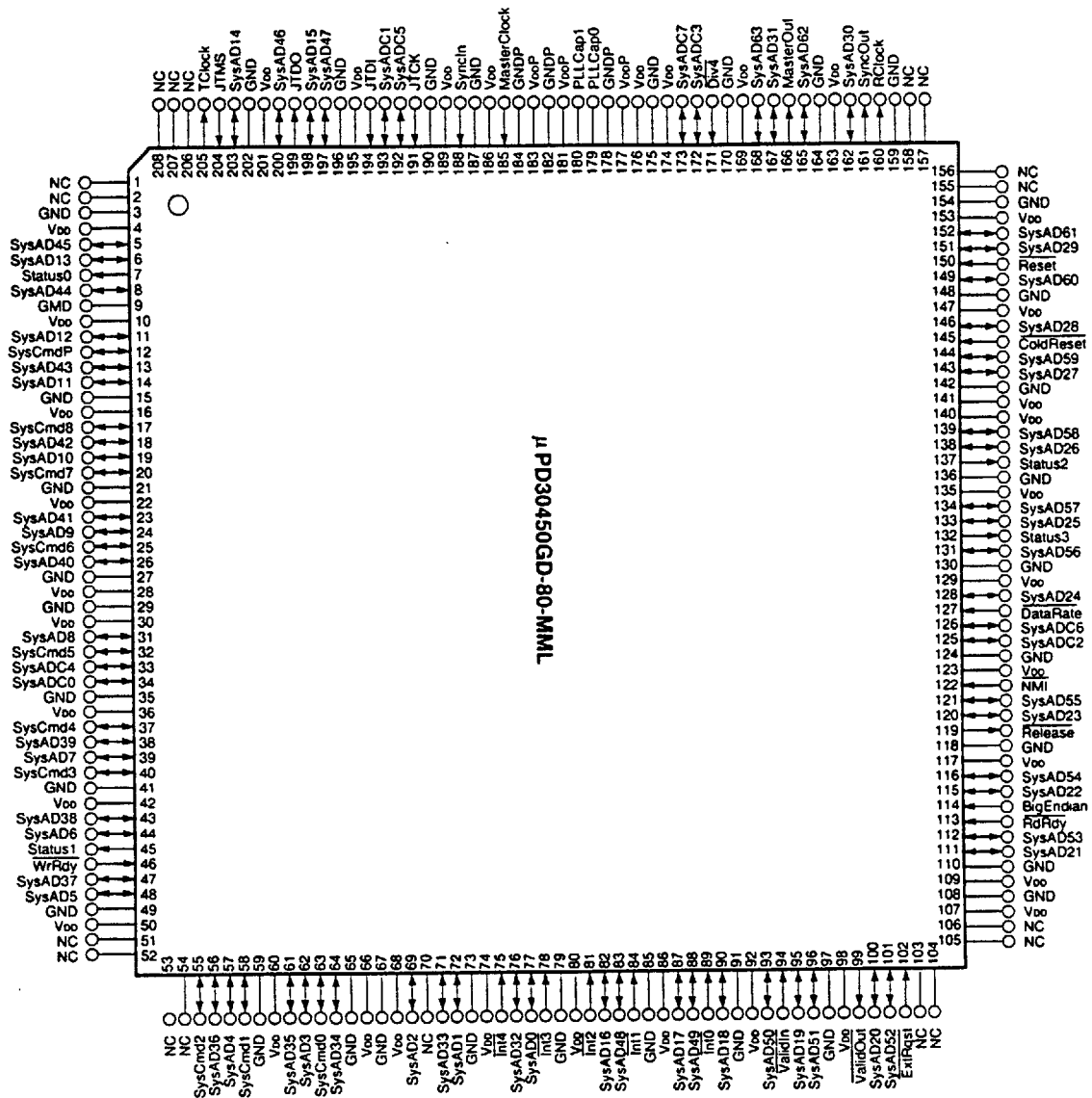
ORDERING INFORMATION

Part Number	Package	Maximum Internal Operating Frequency (MHz)	★
μ PD30450GD-80MML	208-pin plastic QFP (fine pitch) (28 × 28 mm)	80	

The information in this document is subject to change without notice.

PIN CONFIGURATION

- 208-pin plastic QFP (fine pitch) (28 × 28 mm) (Top View)



Pin Name

<u>BigEndian</u>	: Big endian
<u>ColdReset</u>	: Cold reset
<u>DataRate</u>	: Data Rate
<u>Div4</u>	: Divide by 4
<u>ExtRqst</u>	: External request
<u>Int (4:0)</u>	: Interrupt request
JTCK	: JTAG clock input
JTDI	: JTAG data in
JTDO	: JTAG data out
JTMS	: JTAG command signal
MasterClock	: Master clock
MasterOut	: Master clock out
<u>NMI</u>	: Non-maskable interrupt request
PLLCap (1:0)	: Phase Locked loop capacitance
RClock	: Receive clock
<u>RdRdy</u>	: Read ready
<u>Release</u>	: Release
<u>Reset</u>	: Reset
Status (3:0)	: Status
SyncIn	: Synchronization clock input
SyncOut	: Synchronization clock output
SysAD (63:0)	: System address/data bus
SysADC (7:0)	: System address/data check
SysCmd (8:0)	: System command/data ID bus
SysCmdP	: System command parity
TClock	: Transmit clock
<u>ValidIn</u>	: Valid in
<u>ValidOut</u>	: Valid out
<u>WrRdy</u>	: Write ready
V _{oo}	: Power supply
V _{ooP}	: Power supply for PLL
GND	: Ground
GNDP	: Ground for PLL
NC	: No Connection

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1. PIN FUNCTIONS

Pin Name	Function	I/O
$\overline{\text{ExtRqst}}$	External request. This signal is issued by an external agent to request permission to issue an external request.	I
$\overline{\text{Release}}$	Releases interface. This signal indicates that the processor releases the system interface to the slave status in response to the $\overline{\text{ExtRqst}}$ signal.	O
$\overline{\text{RdRdy}}$	Read ready. This signal indicates that the external agent is ready to accept a read request from the processor.	I
SysAD (63:0)	System address/data bus. These pins form a 64-bit address/data bus for communication between the processor and external agent.	I/O (3-state)
SysADC (7:0)	System address/data check bus. These pins form an 8-bit bus including a check bit for the SysAD bus.	I/O (3-state)
SysCmd (8:0)	System command/data ID bus. These pins form a 9-bit bus for communication of commands and data identifiers between the processor and external agent.	I/O (3-state)
SysCmdP	System command/data ID bus parity. This is an even parity bit for the SysCmd bus.	I/O (3-state)
$\overline{\text{ValidIn}}$	Valid in. This signal indicates that the external agent drives a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.	I
$\overline{\text{ValidOut}}$	Valid out. This signal indicates that the processor drives a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.	O
$\overline{\text{WrRdy}}$	Write ready. This signal indicates that the external agent is ready to accept a write request from the processor.	I
$\overline{\text{Int}}$ (4:0)	Interrupt. These are general processor interrupt requests by which the input statuses of bits 14 to 10 of the cause register can be checked.	I
$\overline{\text{NMI}}$	Non-maskable interrupt. This is an interrupt request that cannot be masked.	I
JTDI	JTAG data input. Inputs JTAG serial data.	I
JTCK	JTAG clock input. Inputs JTAG serial clock. If the tag interface is not used, please set it to low level.	I
JTDO	JTAG data output. Outputs JTAG serial clock.	O
JTMS	JTAG command. JTAG command signal. Indicates that the input serial data is command data.	I
MasterClock	Master clock. Inputs the master clock as the operating frequency of the processor.	I

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Pin Name	Function	I/O
MasterOut	Master clock output. Master clock output in synchronization with the master clock.	O
RClock	Receive clock. Received clock as the system interface frequency.	O
TClock	Transmit clock. Transmit clock as the system interface frequency.	O
SyncOut	Synchronization clock output. Outputs a synchronization clock. SyncOut must be connected to SyncIn via the model of delay cause among MasterOut, TClock, RClock, and external agent.	O
SyncIn	Synchronization clock input. Inputs a synchronization clock.	I
$\overline{\text{ColdReset}}$	Cold reset. This signal is asserted on power-ON reset or cold reset. SClock, TClock, and RClock start output in synchronization with the deassert edge of this signal. This signal must also be deasserted in synchronization with MasterClock.	I
$\overline{\text{Reset}}$	Reset. This signal is asserted on power-ON reset, cold reset, or software reset. This signal must be deasserted in synchronization with MasterClock.	I
Status (3:0)	Status display. These pins output the internal statuses of the current processor cycle.	O
BigEndian	Big endian. Sets the endian mode of the system interface. 0: little endian, 1: big endian	I
$\overline{\text{DataRate}}$	Data transfer rate. Sets the transfer rate of data at which the processor transfers data to the external agent. 0: DDx, 1: Dxx	I
$\overline{\text{Div4}}$	Divide by 4 (operating frequency of system interface). Sets the division ratio of the system interface frequency with respect to the pipeline clock. 0: 1/4PClock, 1: 1/2PClock However, a setting through this pin is not supported by the current V _a 4200. Fix this pin to 1.	I
PLLCap (1:0)	Phase Locked Loop capacitance. Connect a capacitor to adjust the internal PLL across these pins.	—
V _{DDP}	V _{DD} for PLL. Power supply for the internal PLL.	—
GNDP	Ground for PLL. Ground for the internal PLL.	—
V _{DD}	Power supply	—
GND	Ground	—

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2. CPU INTERNAL ARCHITECTURE

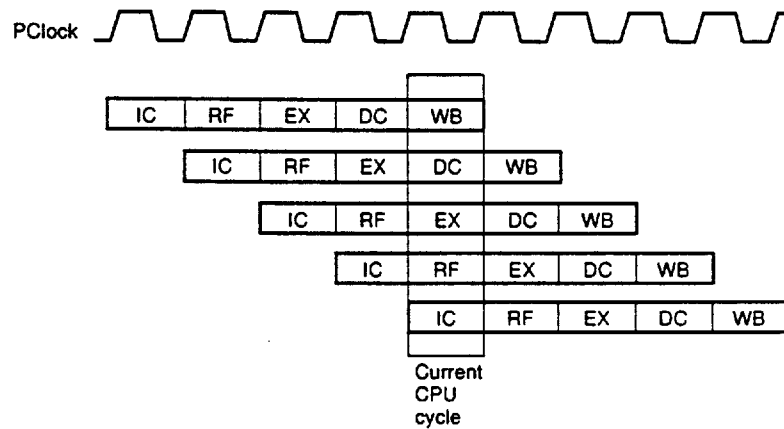
2.1 Pipeline

Each instruction is executed in the following five steps:

- (1) IC Instruction cache fetch
- (2) RF Register fetch
- (3) EX Execution
- (4) DC Data cache fetch
- (5) WR Write back

The V_R4200 uses a 5-stage pipeline. The pipeline operates in accordance with a clock (PClock) two times that of MasterClock, and instructions are executed at almost one per cycle. Therefore, ordinary instructions are executed overlapping with each other, as shown in Figure 2-1.

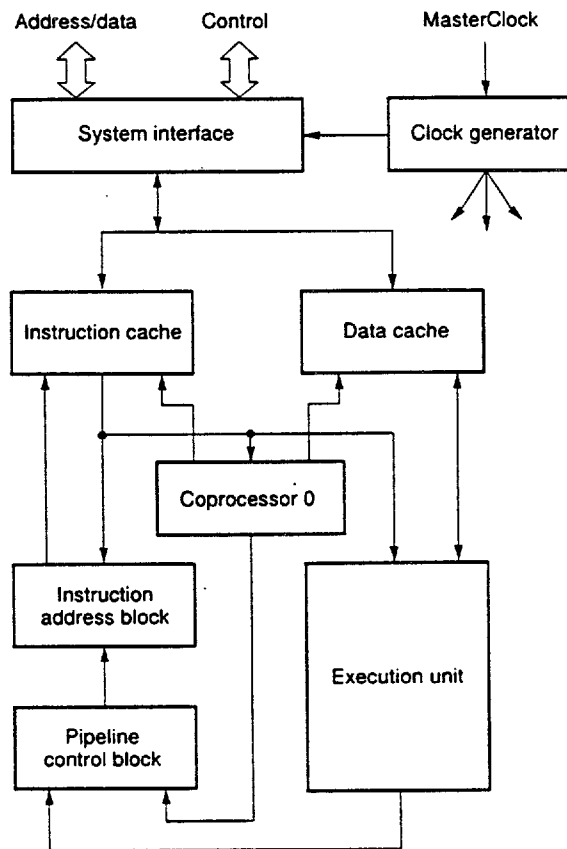
Figure 2-1. Pipeline of V_R4200 (5 stages)



2.2 Internal Function Blocks

The V_R4200 consists of several functional blocks, such as an execution unit, coprocessor 0, instruction cache, data cache, and system interface.

Figure 2-2. Internal Block Diagram



(1) System interface

This block performs interfacing when the processor accesses an external device (such as a memory). This interface is compatible with the system interface bus used by the V α 4000. The external device is accessed by a 64-bit address/data multiplexed bus.

(2) Clock generator

The clock generator doubles the frequency of an externally input clock (MasterClock) to generate a pipeline clock (PClock). PClock is further divided by two and used as a system interface clock.

(3) Instruction cache

The instruction cache consists of direct mapping, virtual index, and physical tag type, and has a capacity of 16K bytes.

(4) Execution unit

This block executes integer and floating-point operations. It consists of a 64-bit register file, 64-bit integer/mantissa data bus, and exponent data bus.

(5) Coprocessor 0 (CP0)

This block performs exception processing. It contains a memory management unit (MMU), and manages addresses. Virtual addresses are converted into physical addresses by TLB (Translation Lookaside Buffer: high-speed conversion buffer mechanism).

(6) Data cache

This cache consists of direct mapping, virtual index, and physical tag type, and has a capacity of 8K bytes.

(7) Instruction address block

This block calculates the effective address of the instruction to be fetched next. It consists of a program counter (PC) increment block, target address addition block, and branch address select block.

(8) Pipeline control block

This block controls stall so that the pipeline can operate normally.

2.3 Registers

2.3.1 CPU registers

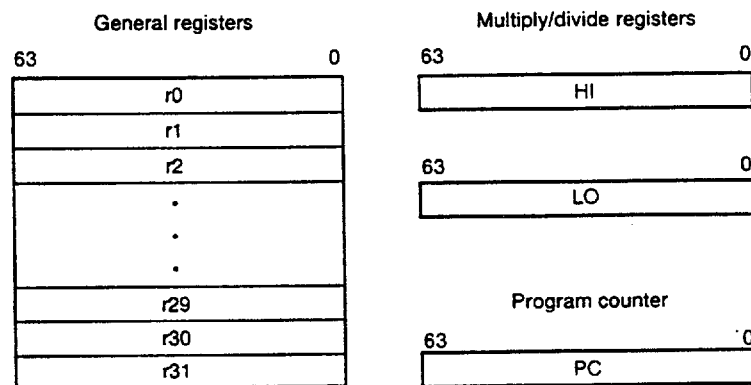
Figure 2-3 shows the CPU registers of the Vn4200. The bit width of these registers is determined by the operation mode of the processor (in 32-bit mode: 32 bits, in 64-bit mode: 64 bits).

Of the 32 general registers, the following two have special meanings:

- Register r0: The contents of this register are always 0. This register can be described as the target register of an instruction when the result of an operation is to be discarded. When the value of 0 is necessary, this register can be used as a source register.
- Register r31: This register is a link register for the JAL and JALR instructions. Therefore, do not use this register by any other instructions.

The two multiply/divide registers (HI, LO) store the result of an integer multiplication, or the quotient (LO) and remainder (HI) resulting from an integer division.

Figure 2-3. CPU Registers

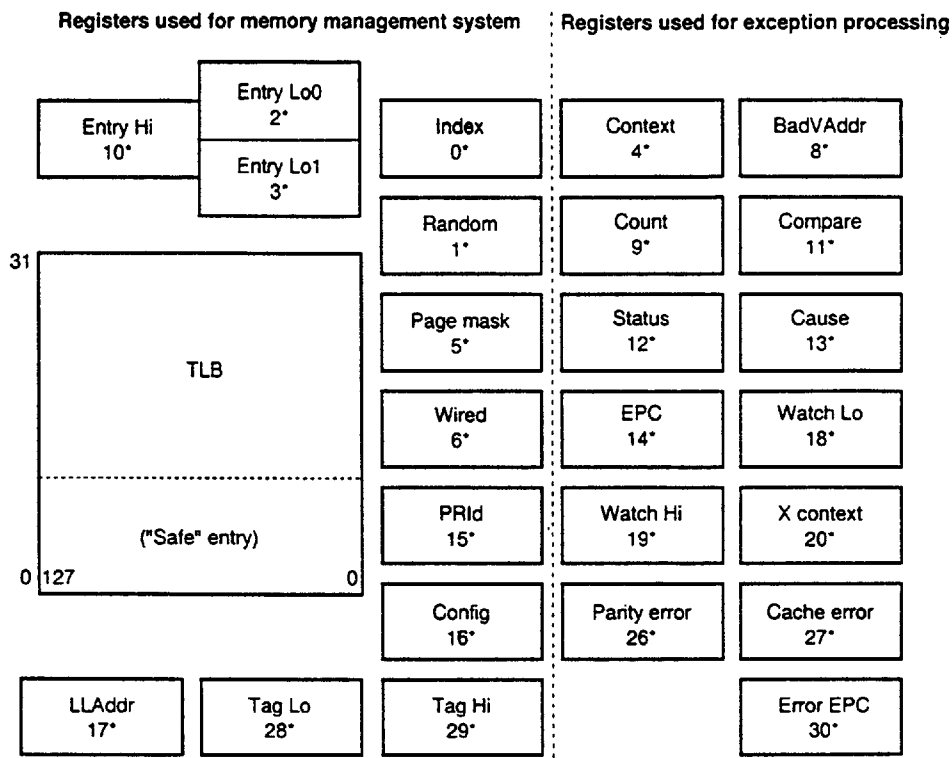


No program status word (PSW) is provided. The function of the PSW is executed by the status register and cause register integrated to the system control coprocessor (CP0).

2.3.2 CP0 registers

The system control coprocessor 0 (CP0) supports virtual memory systems and exception processing.

Figure 2-4. CP0 Registers



Remark "*" indicates a register number.

Table 2-1. CP0 Registers

No.	Register	Description
0	Index	Programmable pointer to TLB array
1	Random	Pseudo random pointer to TLB array (read only)
2	Entry Lo0	Second half of TLB entry for even VPN
3	Entry Lo1	Second half of TLB entry for odd VPN
4	Context	Pointer to virtual PTE table of kernel in 32-bit mode
5	Page master	Specifies page size
6	Wired	Number of wired TLB entries
7	—	RFU (Reserved for Future Use: reserved)
8	BadVAddr	Displays virtual address where error occurs last
9	Count	Timer count
10	Entry Hi	First half of TLB entry (including ASID)
11	Compare	Timer compare value
12	Status	Sets operation status
13	Cause	Displays cause of exception that occurs last
14	EPC	Exception program counter
15	PRId	Processor revision ID
16	Config	Sets memory system mode
17	LLAddr	Displays address of LL instruction
18	Watch Lo	Lower bits of memory reference trap address
19	Watch Hi	Higher bits of memory reference trap address
20	X context	Pointer to virtual PTE table of kernel in 64-bit mode
21–25	—	RFU
26	Parity error	Parity bit of cache
27	Cache error	Cache error and status register
28	Tag Lo	Cache tag register, low
29	Tag Hi	Cache tag register, high
30	Error EPC	Error exception program counter
31	—	RFU

2.4 Data Format

The V_R4200 uses four data formats: double word (64-bit), word (32-bit), half word (16-bit), and byte (8-bit) formats. The byte order can be configured in either big-endian or little-endian order.

Figure 2-5. Byte Address in Word

(a) Big endian

	31	24 23	16 15	8 7	0	Word address
Higher address	8	9	10	11		8
	4	5	6	7		4
Lower address	0	1	2	3		0

- The highest byte is the lowest address.
- A word is addressed by the address of the highest byte.

(b) Little endian

	31	24 23	16 15	8 7	0	Word address
Higher address	11	10	9	8		8
	7	6	5	4		4
Lower address	3	2	1	0		0

- The lowest byte is the lowest address.
- A word is addressed by the address of the lowest byte.

Figure 2-6. Byte Address in Double Word (1/2)

(a) Big endian

	63							0	Double word address
Higher address	16	17	18	19	20	21	22	23	16
	8	9	10	11	12	13	14	15	8
Lower address	0	1	2	3	4	5	6	7	0

- The highest byte is the lowest address.
- A word is addressed by the address of the lowest byte.

Figure 2-6. Byte Address in Double Word (2/2)

(b) Little endian

	63							0	Double word address
Higher address	23	22	21	20	19	18	17	16	16
	15	14	13	12	11	10	9	8	8
Lower address	7	6	5	4	3	2	1	0	0

- The lowest byte is the lowest address.
- A word is addressed by the address of the lowest byte.

2.5 Cache

(1) Instruction cache

The features of the instruction cache are as follows:

- Internal cache memory
- Capacity: 16K bytes
- Direct mapping
- Virtual index address
- Physical tag check
- 8-word (32-byte) cache line

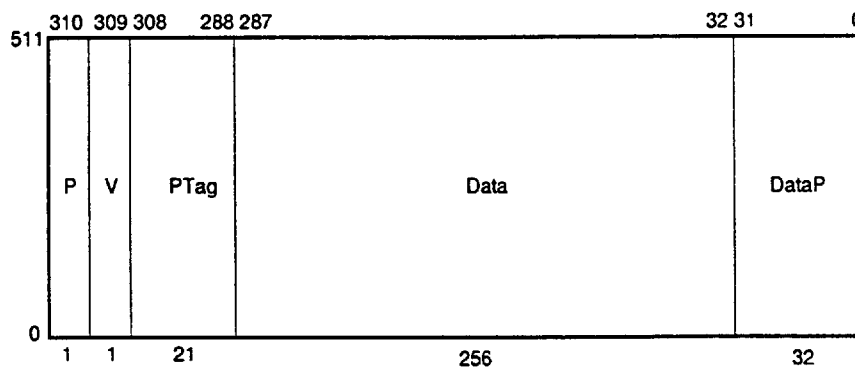
(2) Data cache

The features of the data cache are as follows:

- Internal cache memory
- Capacity: 8K bytes
- Write back
- Direct mapping
- Virtual index address
- Physical tag check
- 4-word (16-byte) cache line

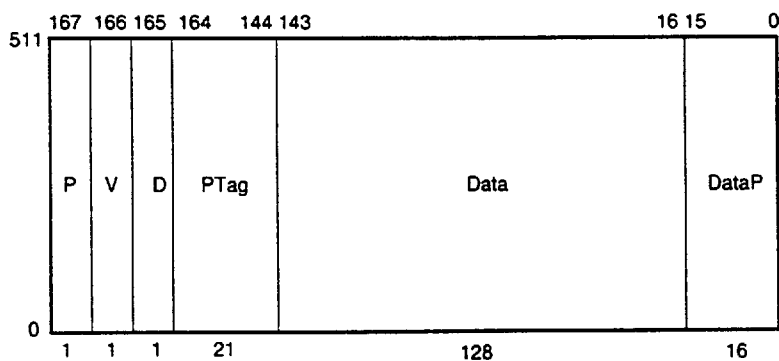
Figure 2-7. Cache Memory Block Diagram

(a) Instruction cache



DataP : parity bit for data
 Data : data (of 1 line)
 PTag : physical tag
 V : valid bit
 P : tag parity

(b) Data cache



DataP : parity bit for data
 Data : data (of 1 line)
 PTag : physical tag
 D : Dirty bit (shows that it has been written)
 V : valid bit
 P : tag parity

2.6 Virtual Storage

2.6.1 Virtual address space

The V_R4200 has two operation modes: 32-bit and 64-bit modes. In addition, it also has three types of operating modes: user mode, supervisor mode, and kernel mode. The following figures show the virtual address space in the respective modes:

Figure 2-8. User Mode Address Space

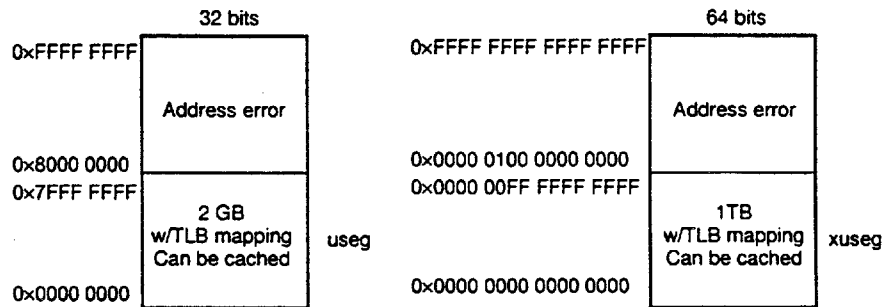


Figure 2-9. Supervisor Mode Address Space

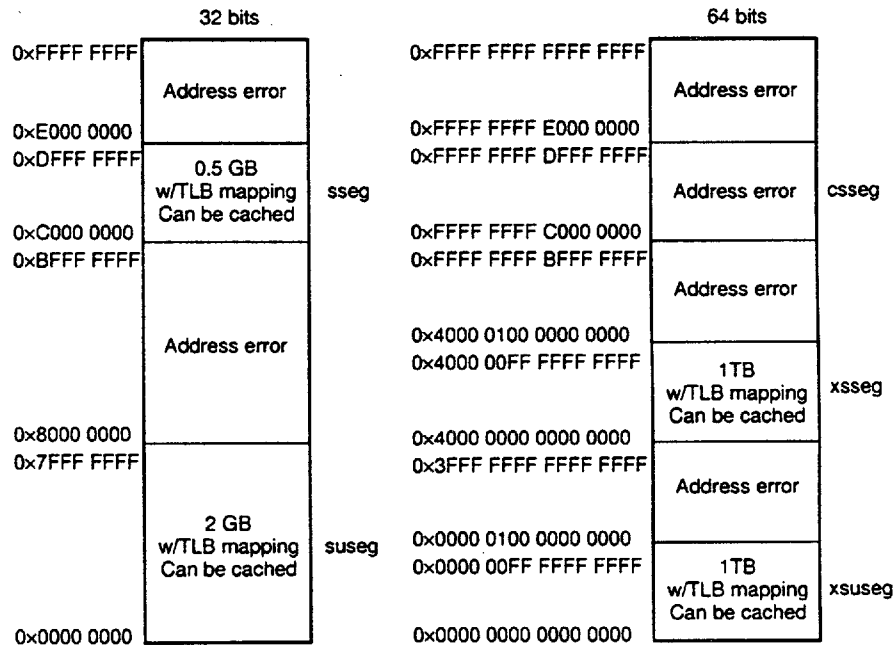
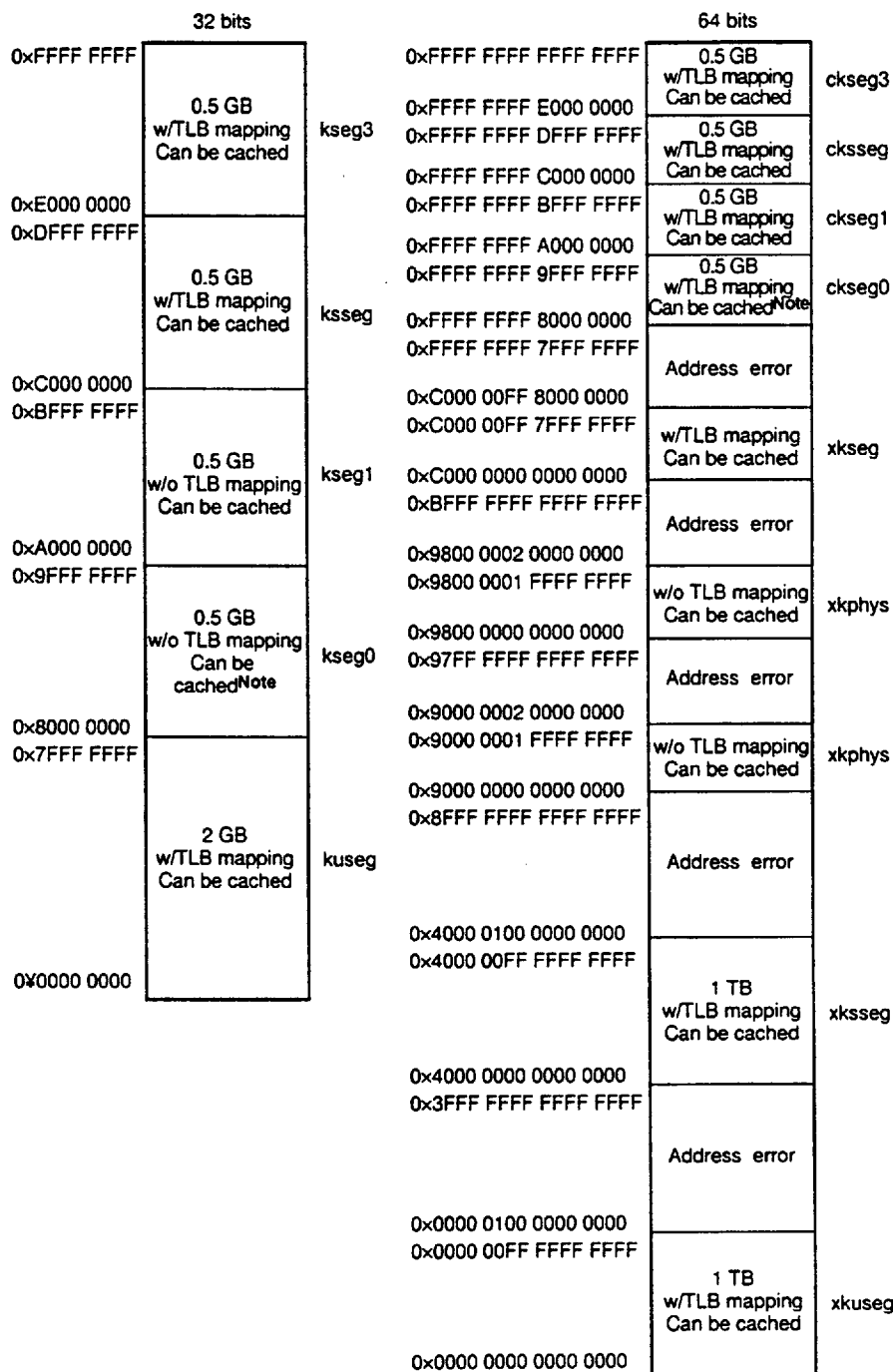


Figure 2-10. Kernel Mode Address Space



★ **Note** Whether kseg0 and ckseg0 are cache areas is determined by the K0 area of the config register.

Figure 2-11. Details of xkphys Area

0xBFFF FFFF FFFF FFFF	Address error
0xB800 0002 0000 0000	8 GB w/o TLB mapping Cache can be used
0xB800 0001 FFFF FFFF	
0xB800 0000 0000 0000	8 GB w/o TLB mapping Cache can be used
0xB7FF FFFF FFFF FFFF	
0xB000 0002 0000 0000	Address error
0xB000 0001 FFFF FFFF	8 GB w/o TLB mapping Cache can be used
0xB000 0000 0000 0000	
0xAFFF FFFF FFFF FFFF	Address error
0xA800 0002 0000 0000	8 GB w/o TLB mapping Cache can be used
0xA800 0001 FFFF FFFF	
0xA800 0000 0000 0000	8 GB w/o TLB mapping Cache can be used
0xA7FF FFFF FFFF FFFF	
0xA000 0002 0000 0000	Address error
0xA000 0001 FFFF FFFF	8 GB w/o TLB mapping Cache can be used
0xA000 0000 0000 0000	
0x9FFF FFFF FFFF FFFF	Address error
0x9800 0002 0000 0000	8 GB w/o TLB mapping Cache can be used
0x9800 0001 FFFF FFFF	
0x9800 0000 0000 0000	8 GB w/o TLB mapping Cache can be used
0x97FF FFFF FFFF FFFF	
0x9000 0002 0000 0000	Address error
0x9000 0001 FFFF FFFF	8 GB w/o TLB mapping Cannot be cached
0x9000 0000 0000 0000	
0x8FFF FFFF FFFF FFFF	Address error
0x8800 0002 0000 0000	8 GB w/o TLB mapping Cache can be used
0x8800 0001 FFFF FFFF	
0x8800 0000 0000 0000	8 GB w/o TLB mapping Cache can be used
0x87FF FFFF FFFF FFFF	
0x8000 0002 0000 0000	Address error
0x8000 0001 FFFF FFFF	8 GB w/o TLB mapping Cache can be used
0x8000 0000 0000 0000	

2.6.2 Address conversion

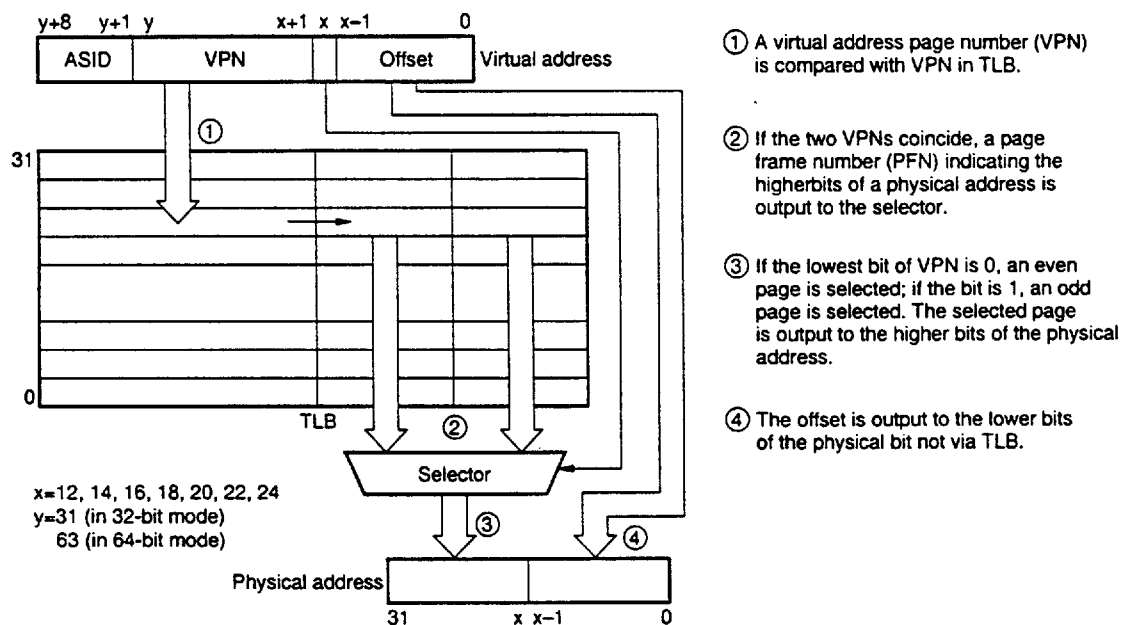
Conversion from a virtual address to a physical address is carried out in page units by the internal TLB (Translation Lookaside Buffer). TLB is of full-associative configuration and has 64 entries at the virtual address side and 32 entries at the physical address side. The page size is variable from 4K bytes to 16M bytes.

If a TLB entry is not hit, a TLB unmatched exception occurs in the 32-bit mode, and a XTLB unmatched exception occurs in the 64-bit mode. Exchange the contents of TLB by software.

The following figure illustrates the outline of address conversion.

Figure 2-12. Outline of Address Translation

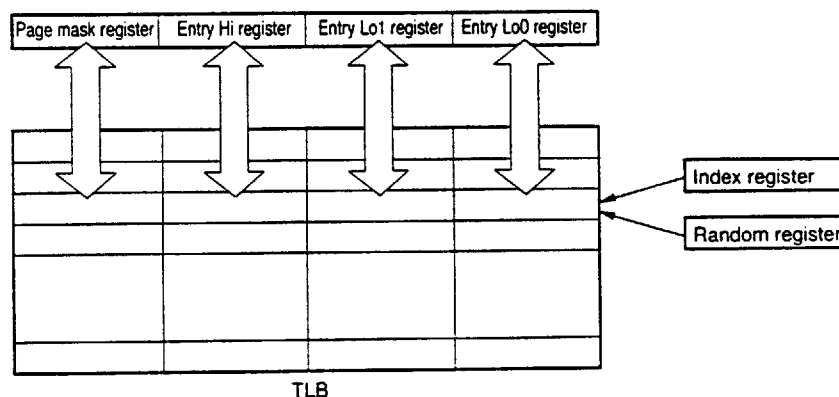
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A TLB entry is read/written by loading/storing the TLB entry indicated by the index register and random register among entry Hi, Entry Lo1, Entry Lo0, and page mask registers.

The following figure outlines TLB manipulation.

Figure 2-13. Outline of TLB Manipulation



2.7 Exception Processing

When an exception is detected, interrupts are disabled, the operating mode is changed to the kernel mode, and execution jumps to a specified exception handler.

If an exception occurs, the EPC register holds a restart address that is used to resume execution. The restart address is the address of the instruction that has caused the exception, or the address of the branch instruction immediately before if the instruction has been executed in the branch delay slot.

Table 2-2. Exceptions

Exception	Vector (32-bit mode)	Cause
Reset	0xBFC0 0000 (BEV bit is automatically set to 1.)	Generates if $\overline{\text{ColdReset}}$ signal has been made active once and then inactive.
Soft Reset		Generates when $\overline{\text{Reset}}$ signal has been made active once and then inactive.
NMI		Generates when $\overline{\text{NMI}}$ signal falls.
TLB Unmatch	0x8000 0000 (BEV=0) 0xBFC0 0200 (BEV=1)	If TLB entry matching address referenced in 32-bit mode is missing.
XTLB Unmatch	0x8000 0080 (BEV=0) 0xBFC0 0280 (BEV=1)	If TLB entry matching address referenced in 64-bit mode is missing.
Cache Error	0xA000 0100 (BEV=0) 0xBFC0 0300 (BEV=1)	Generates if parity error of system bus and cache is detected.
TLB Invalid	0x8000 0180 (BEV=0) 0xBFC0 0380 (BEV=1)	If TLB entry matching referenced physical address is invalid.
TLB Change		If TLB entry matching physical address referenced by store instruction is valid but cannot be written.
Address Error		If word not positioned is accessed, or if virtual address that cannot be used in user and supervisor modes is referenced.
Bus Error		If error is indicated by data identifier.
Integer Overflow		Generates if 2's complement overflow occurs as result of executing addition or subtraction.
Trap		If condition becomes true when trap instruction is executed.
System Call		Generates when SYSCALL instruction is executed.
Break Point		Generates when BREAK instruction is executed.
Reserved Instruction		If attempt is made to execute undefined instruction.
Coprocessor Cannot be Used		If use of corresponding coprocessor unit is not enabled when coprocessor instruction is executed.
Floating-point Operation		If error occurs when FPU instruction is executed.
Watch		If attempt is made to reference physical address in watch Lo/watch Hi register by load/store instruction.
Interrupt		If one of eight interrupt sources becomes active. Can be classified into three types: external, software, and timer.

Remark The higher 32 bits of the exception vector are all 1 in the 64-bit mode, and the lower 32 bits are the same as the vector address in the 32-bit mode.

3. FPU INTERNAL ARCHITECTURE

Unlike the V_R4000 and V_R4400™, The FPU (floating-point operation unit) of the V_R4200 is integrated to the CPU (integer operation unit). The CPU and FPU use the same data bus, and the FPU instructions are executed by the hardware of the CPU.

V_R4200 logically handles the FPU as an independent coprocessor and can execute all the floating-point instructions defined by MIPS ISA.

3.1 FPU Registers

(1) Floating-point general registers (FGRs)

These registers are physical general registers and can be directly accessed. There are 32 general registers. The bit length of these registers varies depending on the content of the FR bit of the status register.

(2) Floating-point registers (FPRs)

These 64-bit logical registers hold a floating-point value when a floating-point operation is executed. The number of FPRs varies depending on the contents of the FR bit of the status register.

(3) Floating-point control registers (FCRs)

There are the following two FCRs:

(a) Control/status register (FCR31)

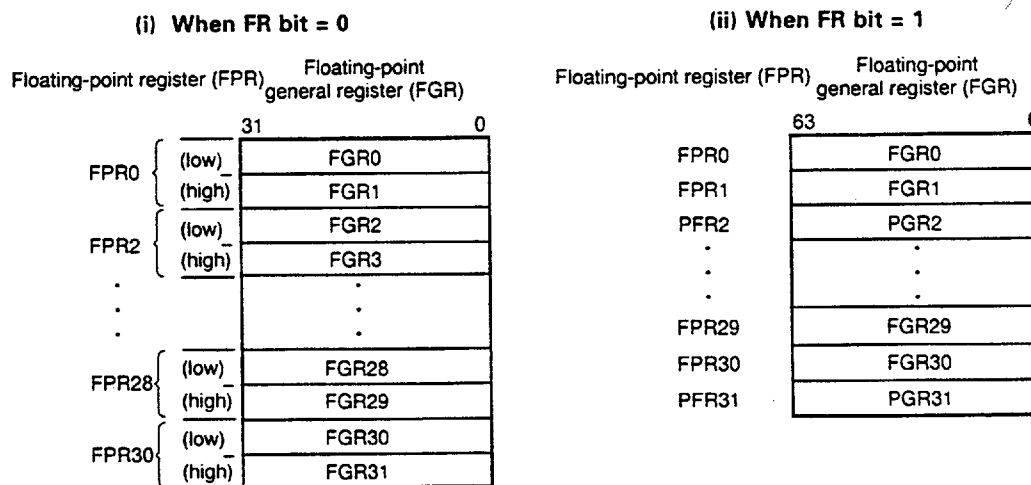
This register controls and monitors exceptions, holds the result of a comparison operation, and sets a rounding mode.

(b) Processor/revision register (FCR0)

This register holds the revision information of the FPU.

Figure 3-1. FPU Registers

(a) FGR and FPR

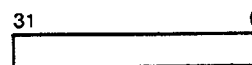


(b) FCR

(i) Control/status register (FCR31)



(ii) Processor/revision register (FCR0)



3.2 Data Format

(1) Floating-point format

FPU supports 32-bit (single-precision) and 64-bit (double-precision) IEEE754 floating-point operations.

(2) Fixed-point format

The value of a fixed point is computed in the format of 2's complement.

4. INTERFACE

4.1 System Interface

The input/output timing of the processor is as follows:

- The processor output starts changing at the rising edge of SClock.
- The processor input is latched at the rising edge of SClock.

The following two buses are used for system interfacing:

- SysAD (63: 0) : This bus transfers addresses and data.
- SysCmd (8: 0) : This bus transfers commands and data identifiers.

The SysAD and SysCmd buses are bidirectional buses and are driven by the processor or external agent.

These buses enter the following two states depending on the direction in which they are driven:

- Master state : The buses are driven by the processor to issue a processor request.
- Slave state : The buses are driven by the external agent to issue an external request.

The following two cycles are used depending on the information included in the SysAD bus:

- Address cycle : The valid address is included in the SysAD bus.
- Data cycle : The valid data is included in the SysAD bus.

Here are brief descriptions of the interface control signals:

- ValidOut : This signal is asserted by the processor when the SysAD and SysCmd buses are valid in the master state.
- ValidIn : This signal is asserted by the external agent when the SysAD and SysCmd buses are valid in the slave state.
- ExtRqst : This signal is asserted by the external agent when the external agent issues an external request.
- Release : This signal is used by the processor to place the system interface in the slave state.
- RdRdy : This signal is used by the external agent to inform that it is ready to accept a processor read request.
- WrRdy : This signal is used by the external agent to inform that it is ready to accept a processor write request.

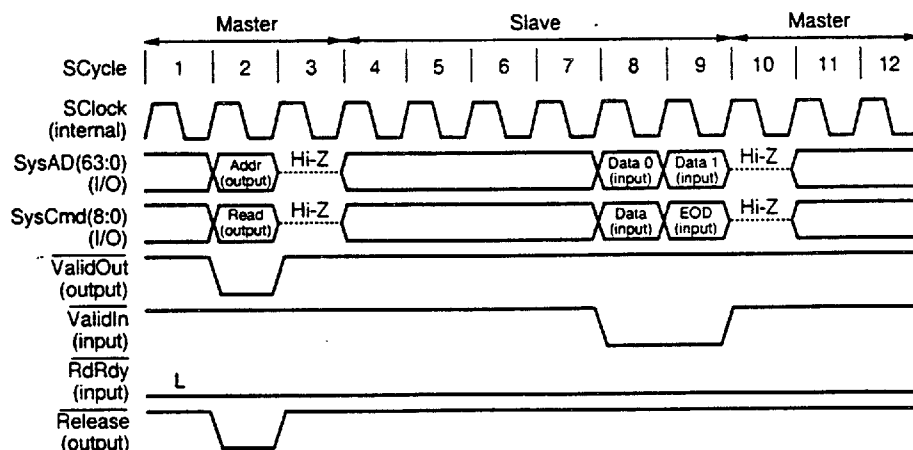
4.1.1 System interface request

The system interface supports the following requests:

Request	Outline	Data Unit
Processor Read Request	Read request to main memory or I/O	1-7 bytes, 2/4/8 words
Processor Write Request	Write request to main memory or I/O	
External null Request	Request to release system interface	—
External Write Request	Interrupt request from system bus	1 word

As an example of the protocol of the system interface request, Figure 4-1 shows the timing of the processor read request and read response.

Figure 4-1. Timing of Processor Read Request and Read Response (block transfer)



4.1.2 Data transfer rate control

The system interface supports a data transfer rate of double words per 1 SCycle maximum.

(1) To transfer data from external agent to processor

The external agent can transfer data at any transfer rate. The data is accepted only in a cycle in which ValidIn is asserted.

(2) To transfer data from processor to external agent

The transfer rate is selected by the DataRate pin at reset from DDx and Dxx (D: data cycle, x: vacant cycle).

4.1.3 Clock interface

The input clock of the V_A4200 is called MasterClock. This clock is internally multiplied to generate PClock based on which the pipeline operation is performed.

The system bus operates based on SClock. However, SClock is externally output. Instead, the CPU supplies the external agent with RClock as the reference input clock and TClock as the reference output clock. The operating frequencies of SClock, RClock, and TClock are usually half that of PClock, and the same as that of MasterClock.

4.1.4 Setting division ratio of system interface

The division ratio of the system interface is set from the Div4 pin at reset^{Note}. The pipeline operating frequency can be divided by two or four.

Where the external clock is 40 MHz, the pipeline operates at 80 MHz; therefore, the operating frequency of the system bus is 40 MHz or 20 MHz.

Note Setting by this pin is not supported by the current V_A4200.

5. INTERNAL/EXTERNAL CONTROL FUNCTION

5.1 Reset Function

Reset can be effected in three ways: power-ON reset, cold reset, and soft reset.

Cold reset and soft reset is effected with the power turned ON.

The internal status is initialized at reset. When soft reset is effected, however, only the contents of the system interface and cache memory become undefined, and the other internal status is not initialized but the status before reset is retained.

(1) Power-ON reset and cold reset

Power-ON reset or cold reset is effected when both the $\overline{\text{ColdReset}}$ and $\overline{\text{Reset}}$ signals are made active.

During reset, data is input from the initial setting pin to set the internal initial status of the processor.

Table 5-1 shows the set contents of each pin.

Table 5-1. Setting of Initial Status

Pin Name	Set Contents
BigEndian	Byte order 0: little endian 1: big endian
DataRate	Data transfer rate of external device 0: DDx pattern 1: Dxx pattern
Div4 <small>Note</small>	Operating speed of system interface (vs. PClock) 0: 1/4 1: 1/2

Note Setting of this pin is not supported by the current V_{R4200}.
Set this pin to 1.

(2) Soft reset

Soft reset is executed by making the $\overline{\text{Reset}}$ signal active. This reset does not input the initial status from the initial setting pin, but the status before reset is retained.

5.2 Interrupt Function

(1) Maskable interrupt

This interrupt is subject to mask control. Mask processing is performed by the status register (whether each interrupt is processed or interrupts are processed all at once can be specified).

No priority is assigned to each interrupt.

(a) Hardware interrupts (5 sources)

These interrupts are accepted when an external write request is issued or when the $\overline{\text{Int}}(4:0)$ signal is asserted.

(b) Software interrupt (2 sources)

These interrupts are accepted when the IP0 and IP1 bits of the cause register are set to 1.

(c) Timer interrupt (1 source)

This interrupt is accepted when the value of the count register becomes equal to the value of the compare register and when the IP7 bit of the cause register is set to 1.

(2) Non-maskable interrupt (1 source)

This interrupt cannot be masked. It is accepted when the external write request is issued or when the NMI signal is asserted.

5.3 JTAG Boundary Scan Function

Mutual connection of each device on the board can be tested by the boundary interface that uses the JTAG protocol (the V_R4200 itself cannot be tested).

A TAP controller, JTAG instruction register, JTAG boundary scan register, and JTAG bypass register are incorporated according to the specifications of JTAG (however, JTAG of the V_R4200 only has the external test function of the JTAG boundary scan register).

5.4 Low Power Dissipation Design

The V_R4200 has made the following improvements to reduce the power dissipation, as compared with the V_R4000 and V_R4400:

- Power management of cache in bank units
- Cache prefetch (Two instructions are simultaneously fetched.)
- 3.3-V operation
- Employment of write back cache (to reduce the number of times the system bus is accessed)
- Integrating integer operation unit and floating-point operation unit
- Employment of simple 5-stage pipeline
- Power management by modular execution unit

These features make it possible that the V_R4200 operates on 1.5 W (TYP.).

Moreover, a low power mode in which the power dissipation can be dynamically reduced during operation can also be used (refer to **5.5 Low Power Mode**).

5.5 Low Power Mode

The V_R4200 is set in the low power mode when the bit 27 (RP bit) of the status register is set to 1.

Normally, the processor operates with the frequency of the CPU internal clock (PClock) two times higher than that of MasterClock and the frequency of the system bus clock (SClock, TClock, RClock) the same as that of MasterClock.

In the low power mode, however, the frequencies of PClock and the clock of the system bus are reduced to the 1/4 of those in the normal operation mode. This means that the frequency of PClock is reduced to the 1/2 of that of MasterClock and that the frequency of the clock of the system bus is reduced to the 1/4 of that of MasterClock.

This mode can therefore reduce the power dissipation of the CPU to about the 1/4 of that in the normal operation mode.

5.6 Hardware Debug Support Function

The V_R4200 has a function to output which instruction is currently executed by the pipeline to Status (3:0).

Moreover, it can also output a branch destination physical address from SysAD (63:0) if the instruction address is changed as a result of execution of a branch or jump instruction or generation of an exception.

These functions can be used when the bit 24 (ITS bit: instruction trace) of the status register is set to 1.

5.6.1 Output of internal processor status

Status (3:0) outputs the current operation status of the pipeline and the category of the instruction executed in the WB stage.

Status (3:0) is output in synchronization with the rising edge of PClock.

5.6.2 Output of branch destination address

This function forcibly generates an instruction cache miss in the following cases:

- If the branch condition is satisfied when a branch instruction is executed
- If the contents of PC are changed as a result of executing a jump instruction or generation of an exception.

If an instruction cache miss occurs, SysAD (63:0) issues a processor block read request, which allows the external agent to know changes in addresses.

In response to the processor block read request, return response data in the same manner as to the normal request. The output address is not the value of the PC (virtual address), but a physical address.

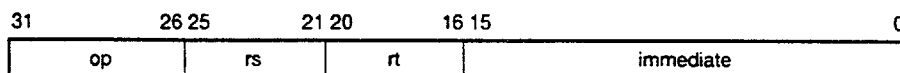
6. INSTRUCTION SET

An instruction of the V_R4200 consists of 1 word (32 bits) located at the word boundary. There are the three types of instruction formats, as shown in Figure 6-1. By using only three instruction formats, decoding an instruction is simplified. Operations and addressing modes that are complicated and are not used so frequently are realized by the compiler.

6.1 Instruction Format

Figure 6-1. Instruction Format

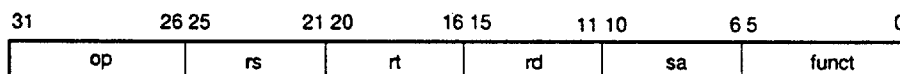
I-type (immediate type)



J-type (jump type)



R-type (register type)



op	6-bit op code
rs	5-bit source register specifier
rt	5-bit target (source/destination) register or branch condition
immediate	16-bit immediate, branch displacement, or address displacement
target	26-bit unconditional branch target address
rd	5-bit destination register specifier
sa	5-bit shift amount
funct	6-bit function field

6.2 CPU Instruction Set

The CPU instructions of the V_R4200 can be classified into an instruction set that is common to all the V_R series processors (ISA: Instruction Set Architecture), the instruction set that is executed by the V_R4000 series (extended ISA), and a system control coprocessor instruction set. The list of each instruction set is shown on the following pages.

Table 6-1. CPU Instruction Set: ISA (1/3)

Instruction	Description	Format			
Load/store instructions		op	base	rt	offset
LB	Load Byte	LB		rt, offset (base)	
LBU	Load Byte Unsigned	LBU		rt, offset (base)	
LH	Load Halfword	LH		rt, offset (base)	
LHU	Load Halfword Unsigned	LHU		rt, offset (base)	
LW	Load Word	LW		rt, offset (base)	
LWL	Load Word Left	LWL		rt, offset (base)	
LWR	Load Word Right	LWR		rt, offset (base)	
SB	Store Byte	SB		rt, offset (base)	
SH	Store Halfword	SH		rt, offset (base)	
SW	Store Word	SW		rt, offset (base)	
SWL	Store Word Left	SWL		rt, offset (base)	
SWR	Store Word Right	SWR		rt, offset (base)	
ALU immediate instructions		op	rs	rt	offset
ADDI	Add Immediate	ADDI		rt, rs, immediate	
ADDIU	Add Immediate Unsigned	ADDIU		rt, rs, immediate	
SLTI	Set On Less Than Immediate	SLTI		rt, rs, immediate	
SLTIU	Set On Less Than Immediate Unsigned	SLTIU		rt, rs, immediate	
ANDI	And Immediate	ANDI		rt, rs, immediate	
ORI	Or Immediate	ORI		rt, rs, immediate	
XORI	Exclusive Or Immediate	XORI		rt, rs, immediate	
LUI	Load Upper Immediate	LUI		rt, immediate	
3-operand type instructions		op	rs	rt	rd sa funct
ADD	Add	ADD		rd, rs, rt	
ADDU	Add Unsigned	ADDU		rd, rs, rt	
SUB	Subtract	SUB		rd, rs, rt	
SUBU	Subtract Unsigned	SUBU		rd, rs, rt	
SLT	Set On Less Than	SLT		rd, rs, rt	
SLTU	Set On Less Than Unsigned	SLTU		rd, rs, rt	
AND	And	AND		rd, rs, rt	
OR	Or	OR		rd, rs, rt	
XOR	Exclusive Or	XOR		rd, rs, rt	
NOR	Nor	NOR		rd, rs, rt	
Shift instructions		op	rs	rt	rd sa funct
SLL	Shift Left Logical	SLL		rd, rt, sa	
SRL	Shift Right Logical	SRL		rd, rt, sa	
SRA	Shift Right Arithmetic	SRA		rd, rt, sa	
SLLV	Shift Left Logical Variable	SLLV		rd, rt, sa	
SRLV	Shift Right Logical Variable	SRLV		rd, rt, rs	
SRAV	Shift Right Arithmetic Variable	SRAV		rd, rt, rs	

Table 6-1. CPU Instruction Set: ISA (2/3)

Instruction	Description	Format					
Multiply/divide instructions		op	rs	rt	rd	sa	funct
MULT	Multiply				MULT	rs, rt	
MULTU	Multiply Unsigned				MULTU	rs, rt	
DIV	Divide				DIV	rs, rt	
DIVU	Divide Unsigned				DIVU	rs, rt	
MFHI	Move From HI				MFHI	rd	
MFLO	Move From LO				MFLO	rd	
MTHI	Move to HI				MTHI	rs	
MTLO	Move To LO				MTLO	rs	
Jump instructions (1)		op	target				
J	Jump				J	target	
JAL	Jump And Link				JAL	target	
Jump instructions (2)		op	rs	rt	rd	sa	funct
JR	Jump Register				JR	rs	
JALR	Jump And Link Register				JALR	rs, rd	
Branch instructions (1)		op	rs	rt	offset		
BEQ	Branch On Equal				BEQ	rs, rt, offset	
BNE	Branch On Not Equal				BNE	rs, rt, offset	
BLEZ	Branch On Less Than Or Equal To Zero				BLEZ	rs, offset	
BGTZ	Branch On Greater Than Zero				BGTZ	rs, offset	
Branch instructions (2)		REGIMM	rs	sub	offset		
BLTZ	Branch On Less Than Zero				BLTZ	rs, offset	
BGEZ	Branch On Greater Than Or Equal to Zero				BGEZ	rs, offset	
BLTZAL	Branch On Less Than Zero And Link				BLTZAL	rs, offset	
BGEZAL	Branch On Greater Than Or Equal To Zero And Link				BGEZAL	rs, offset	
Special instructions		SPECIAL	rs	rt	rd	sa	funct
SYNC	Synchronize				SYNC		
SYSCALL	System Call				SYSCALL		
BREAK	Breakpoint				BREAK		
Coprocessor instructions (1)		op	base	rt	offset		
LWCz	Load Word To Coprocessor z				LWCz	rt, offset (base)	
SWCz	Store Word From Coprocessor z				SWCz	rt, offset (base)	
Coprocessor instructions (2)		COPz	sub	rt	rd	0	
MTCz	Move To Coprocessor z				MTCz	rt, rd	
MFCz	Move From Coprocessor z				MFCz	rt, rd	
CTCz	Move Control To Coprocessor z				CTCz	rt, rd	
CFCz	Move Control From Coprocessor z				CFCz	rt, rd	

Table 6-1. CPU Instruction Set: ISA (3/3)

Instruction	Description	Format
Coprocessor instructions (3)	COPz CO	cofun
COPz	Coprocessor z Operation	COPz cofun
Coprocessor instructions (4)	COPz BC br	offset
BCzT BCzF	Branch On Coprocessor z True Branch On Coprocessor z False	BCzT offset BCzF offset

Table 6-2. CPU Instruction Set: extended ISA (1/2)

Instruction	Description	Format
Load/store instructions	op base rt	offset
LD LDL LDR LL LLD LWU SC SCD SD SDL SDR	Load Doubleword Load Doubleword Left Load Doubleword Right Load Linked Load Linked Doubleword Load Word Unsigned Store Conditional Store Conditional Doubleword Store Doubleword Store Doubleword Left Store Doubleword Right	LD rt, offset (base) LDL rt, offset (base) LDR rt, offset (base) LL rt, offset (base) LLD rt, offset (base) LWU rt, offset (base) SC rt, offset (base) SCD rt, offset (base) SD rt, offset (base) SDL rt, offset (base) SDR rt, offset (base)
ALU immediate instructions	op rs rt	immediate
DADDI DADDIU	Doubleword Add Immediate Doubleword Add Immediate Unsigned	DADDI rt, rs, immediate DADDIU rt, rs, immediate
3-operand type instructions	op rs rt rd sa funct	
DADD DADDU DSUB DSUBU	Doubleword Add Doubleword Add Unsigned Doubleword Subtract Doubleword Subtract Unsigned	DADD rd, rs, rt DADDU rd, rs, rt DSUB rd, rs, rt DSUBU rd, rs, rt
Shift instructions	op rs rt rd sa funct	
DSLL DSRL DSRA DSLLV DSRLV DSRAV DSLL32 DSRL32 DSRA32	Doubleword Shift Left Logical Doubleword Shift Right Logical Doubleword Shift Right Arithmetic Doubleword Shift Left Logical Variable Doubleword Shift Right Logical Variable Doubleword Shift Right Arithmetic Variable Doubleword Shift Left Logical+32 Doubleword Shift Right Logical+32 Doubleword Shift Right Arithmetic+32	DSLL rd, rt, sa DSRL rd, rt, sa DSRA rd, rt, sa DSLLV rd, rt, rs DSRLV rd, rt, rs DSRAV rd, rt, rs DSLL32 rd, rt, sa DSRL32 rd, rt, sa DSRA32 rd, rt, sa

Table 6-2. CPU Instruction Set: extended ISA (2/2)

Instruction	Description	Format					
Multiply/divide instructions		op	rs	rt	rd	sa	funct
DMULT	Doubleword Multiply					DMULT	rs, rt
DMULTU	Doubleword Multiply Unsigned					DMULTU	rs, rt
DDIV	Doubleword Divide					DDIV	rs, rt
DDIVU	Doubleword Divide Unsigned					DDIVU	rs, rt
Branch instructions (1)		op	rs	rt	offset		
BEQL	Branch On Equal Likely					BEQL	rs, rt, offset
BNEL	Branch On Not Equal Likely					BNEL	rs, rt, offset
BLEZL	Branch On Less Than Or Equal To Zero Likely					BLEZL	rs, offset
BGTZL	Branch On Greater Than Zero Likely					BGTZL	rs, offset
Branch instructions (2)		REGIMM	rs	sub	offset		
BLTZL	Branch On Less Than Zero Likely					BLTZL	rs, offset
BGEZL	Branch On Greater Than Or Equal To Zero Likely					BGEZL	rs, offset
BLTZALL	Branch On Less Than Zero And Link Likely					BLTZALL	rs, offset
BGEZALL	Branch On Greater Than Or Equal To Zero And Link Likely					BGEZALL	rs, offset
Special instructions		SPECIAL	rs	rt	rd	sa	funct
TGE	Trap If Greater Than Or Equal					TGE	rs, rt
TGEU	Trap If Greater Than Or Equal Unsigned					TGEU	rs, rt
TLT	Trap If Less Than					TLT	rs, rt
TLTU	Trap If Less Than Unsigned					TLTU	rs, rt
TEQ	Trap If Equal					TEQ	rs, rt
TNE	Trap If Not Equal					TNE	rs, rt
Exception immediate instructions		REGIMM	rs	sub	immediate		
TGEI	Trap If Greater Than Or Equal Immediate					TGEI	rs, immediate
TGEIU	Trap If Greater Than Or Equal Immediate Unsigned					TGEIU	rs, immediate
TLTI	Trap If Less Than Immediate					TLTI	rs, immediate
TLTIU	Trap If Less Than Immediate Unsigned					TLTIU	rs, immediate
TEQI	Trap If Equal Immediate					TEQI	rs, immediate
TNEI	Trap If Not Equal Immediate					TNEI	rs, immediate
Coprocessor instructions (1)		COPz	sub	rt	rd	0	
DMFCz	Doubleword Move From Coprocessor z					DMFCz	rt, rd
DMTCz	Doubleword Move To Coprocessor z					DMTCz	rt, rd
Coprocessor instructions (2)		op	base	rt	offset		
LDCz	Load Doubleword To Coprocessor z					LDCz	rt, offset (base)
SDCz	Store Doubleword From Coprocessor z					SDCz	rt, offset (base)
Coprocessor instructions (3)		COPz	BC	br	offset		
BCzTL	Branch On Coprocessor z True Likely					BCzTL	offset
BCzFL	Branch On Coprocessor z False Likely					BCzFL	offset

Table 6-3. System Control Coprocessor(CP0) Instruction Set

Instruction	Description	Format				
System control coprocessor instructions (1)		COP0	sub	rt	rd	0
MFC0	Move From Coprocessor 0				MFC0	rt, rd
MTC0	Move To Coprocessor 0				MTC0	rt, rd
DMFC0	Doubleword Move From Coprocessor 0				DMFC0	rt, rd
DMTC0	Doubleword Move To Coprocessor 0				DMTC0	rt, rd
System control coprocessor instructions (2)		COP0	CO	funct		
TLBR	Read Indexed TLB Entry				TLBR	
TLBWI	Write Indexed TLB Entry				TLBWI	
TLBWR	Write Random TLB Entry				TLBWR	
TLBP	Probe TLB For Matching Entry				TLBP	
ERET	Exception Return				ERET	
System control coprocessor instructions (3)		CACHE	base	sub	offset	
CACHE	Cache operation				CACHE	sub, offset (base)

6.3 FPU Instruction Set

All the FPU instructions are 32 bits long and positioned at a word boundary.

Table 6-4 lists the FPU instructions.

Table 6-4. FPU Instruction Set

Instruction	Description	Format			
Load/store instructions		op	base	ft	offset
LWC1	Load Word To FPU	LWC1		ft, offset (base)	
SWC1	Store Word From FPU	SWC1		ft, offset (base)	
LDC1	Load Doubleword To FPU	LDC1		ft, offset (base)	
SDC1	Store Doubleword From FPU	SDC1		ft, offset (base)	
Transfer instructions		COP1	sub	rt	fs
MTC1	Move Word To FPU	MTC1		rt, fs	
MFC1	Move Word From FPU	MFC1		rt, fs	
CTC1	Move Control Word To FPU	CTC1		rt, fs	
CFC1	Move Control Word From FPU	CFC1		rt, fs	
DMTC1	Doubleword Move To FPU	DMTC1		rt, fs	
DMFC1	Doubleword Move From FPU	DMFC1		rt, fs	
Conversion instructions		COP1	fmt	0	fs
CVT.S.fmt	Floating-point Convert To Single Floating-point Format	CVT.S.fmt		fd, fs	
CVT.D.fmt	Floating-point Convert To Double Floating-point Format	CVT.D.fmt		fd, fs	
CVT.L.fmt	Floating-point Convert To Long Fixed-point Format	CVT.L.fmt		fd, fs	
CVT.W.fmt	Floating-point Convert To Single Fixed-point Format	CVT.W.fmt		fd, fs	
ROUND.L.fmt	Floating-point Round To Long Fixed-point Format	ROUND.L.fmt		fd, fs	
ROUND.W.fmt	Floating-point Round To Single Fixed-point Format	ROUND.W.fmt		fd, fs	
TRUNC.L.fmt	Floating-point Truncate To Long Fixed-point Format	TRUNC.L.fmt		fd, fs	
TRUNC.W.fmt	Floating-point Truncate To Single Fixed-point Format	TRUNC.W.fmt		fd, fs	
CEIL.L.fmt	Floating-point Ceiling To Long Fixed-point Format	CEIL.L.fmt		fd, fs	
CEIL.W.fmt	Floating-point Ceiling To Single Fixed-point Format	CEIL.W.fmt		fd, fs	
FLOOR.L.fmt	Floating-point Floor To Long Fixed-point Format	FLOOR.L.fmt		fd, fs	
FLOOR.W.fmt	Floating-point Floor To Single Fixed-point Format	FLOOR.W.fmt		fd, fs	
Arithmetic operation instructions		COP1	fmt	ft	fs
ADD.fmt	Floating-point Add	ADD.fmt		fd, fs, ft	
SUB.fmt	Floating-point Subtract	SUB.fmt		fd, fs, ft	
MUL.fmt	Floating-point Multiply	MUL.fmt		fd, fs, ft	
DIV.fmt	Floating-point Divide	DIV.fmt		fd, fs, ft	
SQRT.fmt	Floating-point Square Root	SQRT.fmt		fd, fs	
ABS.fmt	Floating-point Absolute value	ABS.fmt		fd, fs	
MOV.fmt	Floating-point Move	MOV.fmt		fd, fs	
NEG.fmt	Floating-point Negate	NEG.fmt		fd, fs	
Compare instructions		COP1	fmt	ft	fs
C.cond.fmt	Floating-point Compare	C.cond.fmt		fs, ft	
FPU branch instructions		COP1	BC	br	offset
BC1T	Branch On FPU True	BC1T		offset	
BC1F	Branch On FPU False	BC1F		offset	
BC1TL	Branch On FPU True Likely	BC1TL		offset	
BC1FL	Branch On FPU False Likely	BC1FL		offset	

6.4 Instruction Execution Time

In principle, the V_R4200 executes an instruction in one cycle. Some instructions, however, are executed in two cycles. This section describes the case where two cycles are required to execute an instruction.

6.4.1 CPU instruction

- (1) The data loaded by a load instruction cannot be used in a delay slot. When an instruction that uses loaded data is located in a delay slot, the pipeline is stalled.

The store instruction causes the pipeline to be stalled by the delay slot if it is followed by a load or store instruction.

When the condition of a branch instruction is satisfied, and when a jump instruction is executed, the instruction at the destination address is executed after the delay slot.

Table 6-5. Number of Delay Slot Cycles

Instruction Category	Necessary Number of Cycles (PCycle)
Load	1
Store	1
Jump	1
Branch	1

- (2) When an integer multiply or divide instruction is executed, the pipeline is stalled for the duration of the following number of cycles:

Table 6-6. Number of Stall Cycles of Integer Multiply/Divide Instruction

Instruction	Necessary Number of Cycles (PCycle)
MULT	12
MULTU	13
DIV	39
DIVU	39
DMULT	23
DMULTU	24
DDIV	71
DDIVU	71

6.4.2 FPU instruction

(1) To execute the load/store/transfer instruction, the following number of cycles is necessary:

Table 6-7. Number of Execution Cycles of Load/Store/Transfer Instruction

Instruction	Number of Cycles (PCycle)
LWC1	2/1 ^{Note}
SWC1	1
LDC1	2/1 ^{Note}
SDC1	1
MTC1	1
MFC1	1
DMTC1	1
DMFC1	1
CTC1	1
CFC1	1

Note If the load result is used by an instruction in the delay slot, the pipeline is interlocked for the duration of one cycle.

- (2) The following number of cycles is appended when the compare/arithmetic operation/branch instruction is executed:

Table 6-8. Number of Delay Cycles of FPU Instruction Note 1

Instruction	Number of Cycles (PCycle) <small>Note 2</small>			
	S	D	W	L
Add.fmt	3	3		
Sub.fmt	2	2		
Mul.fmt	11	20		
Div.fmt	29	58		
Sqrt.fmt	31	60		
Abs.fmt	1	1		
Mov.fmt	1	1		
Neg.fmt	1	1		
Round.W.fmt	5	5		
Trunc.W.fmt	5	5		
Ceil.W.fmt	5	5		
Floor.W.fmt	5	5		
Round.L.fmt	5	5		
Trunc.L.fmt	5	5		
Ceil.L.fmt	5	5		
Floor.L.fmt	5	5		
Cvt.S.fmt	—	2	5	5
Cvt.D.fmt	1	—	5	5
Cvt.W.fmt	5	5		
Cvt.L.fmt	5	5		
C.cond.fmt	1	1		
BC1T <small>Note 3</small>	1			
BC1F <small>Note 3</small>	1			
BC1TL <small>Note 3</small>	1			
BC1FL <small>Note 3</small>	1			

- Notes**
1. If the next instruction needs the result of a floating-point operation instruction, one more PCycle is necessary for bypassing the hardware interlock.
 2. The multi-cycle floating-point operation instructions for which the results are apparent are not shown in the above table. All these instructions need 2 PCycle to be completely executed.
 3. The branch delay slot of 1 PCycle defined in terms of structure is applied to all the FPU branch instructions.

7. ELECTRICAL SPECIFICATIONS

Thermal condition The temperature characteristics shown below is under a forcibly ventilated condition. The ventilation condition differs depending on the operating condition. In the worst case, however, a forced ventilation of 1.5 m/s min. is necessary.

Absolute Maximum Rating ($T_A = 25\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}		-0.5 to +4.0	V
Input Voltage ^{Note}	V_I		-0.5 to $V_{DD} + 0.3$	V
		Pulse of less than 10 ns	-1.5 to $V_{DD} + 0.3$	V
Operating Case Temperature	T_C		0 to +85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-65 to +150	$^{\circ}\text{C}$

Note The upper limit of input voltage ($V_{DD} + 0.3$) is 4.0V.

Cautions 1. Do not short-circuit two or more outputs at the same time.

2. If the absolute maximum rating of even one of the above parameters is exceeded, the quality of the product may be degraded. Therefore, unless the absolute maximum rating is strictly observed, the product may be physically damaged. Use this product without any parameter nearing these ratings.

The specifications and conditions shown in DC Characteristics and AC Characteristics below are the range within which the product can operate normally, and within which the quality of the product is guaranteed.

DC Characteristics ($T_C = 0\text{ to }+85\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3 \pm 6\%$)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
High-Level Output Voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	2.4		V
High-Level Output Voltage ^{Note 1}	V_{OHc}	$I_{OH} = -400\text{ }\mu\text{A}$	2.7		V
Low-Level Output Voltage	V_{OL}	$I_{OL} = 2.5\text{ mA}$		0.4	V
High-Level Input Voltage ^{Note 2}	V_{IH}		2.0	$V_{DD} + 0.3$	V
Low-Level Input Voltage ^{Note 2}	V_{IL}		-0.5	+0.8	V
		Pulse of less than 10 ns	-1.5	+0.8	V
High-Level Input Voltage ^{Note 3}	V_{IHc}		0.8 V_{DD}	$V_{DD} + 0.3$	V
Low-Level Input Voltage ^{Note 3}	V_{ILc}		-0.5	0.2 V_{DD}	V
		Pulse of less than 10 ns	-1.5	0.2 V_{DD}	V
Supply Current	I_{DD}			0.67	A
High-Level Input Leakage Current	I_{LH}	$V_I = V_{DD}$		10	μA
Low-Level Input Leakage Current	I_{LL}	$V_I = 0\text{ V}$		-10	μA
High-Level Output Leakage Current	I_{LOH}	$V_O = V_{DD}$		20	μA
Low-Level Output Leakage Current	I_{LOL}	$V_O = 0\text{ V}$		-20	μA

Notes 1. Applied to the TClock, RClock, and MasterOut pins

2. Applied to pins other than MasterClock

3. Applied to the MasterClock pin only.

Remark The supply current during operation is almost proportional to the operating clock frequency.

Capacitance ($T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input Capacitance	C_{in}	$f_c = 1\text{ MHz}$, 0 V at pins other than those not measured		10	pF
Output Capacitance	C_{out}			10	pF

★ AC Characteristics ($T_c = 0\text{ to }+85\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\pm6\%$)

Master clock and clock parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MasterClock High-Level Width	$t_{MCKHigh}$		6		ns
MasterClock Low-Level Width	t_{MCKLow}		6		ns
★ MasterClock Frequency <small>Note</small>			20	40	MHz
★ MasterClock Cycle	t_{MCKP}		25	50	ns
Clock Jitter	$t_{MCJitter}$			± 500	ps
MasterClock Rise Time	t_{MCRise}			5	ns
MasterClock Fall Time	t_{MCFall}			5	ns
JTAG Clock Cycle	$t_{JTAGCKP}$		$4 \times t_{MCKP}$		ns

Note The operation of the V_R4200 is guaranteed only when PLL is enabled. In the RP mode, it is guaranteed at 40 MHz.

System Interface Parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data Output Delay Time <small>Note 1</small>	t_{DO}	$C_L = 50\text{ pF}$	2.0	10	ns
Data Setup Delay Time <small>Note 1</small>	t_{DS}		3.5		ns
Data Hold Delay Time <small>Note 1</small>	t_{DH}		1.5		ns
Mode Data Setup Delay Time <small>Note 2</small>	t_{MDS}		3.5		ns
Mode Data Hold Delay Time <small>Note 2</small>	t_{MDH}		1.5		ns
Status Output Delay Time	t_{SO}	$C_L = 20\text{ pF}$	3.5	7.5	ns
Clock Rise Time <small>Note 3</small>	t_{CORise}	$C_L = 50\text{ pF}$		5	ns
Clock Fall Time <small>Note 3</small>	t_{COFall}			5	ns
Clock High-Level Width <small>Note 3</small>	t_{COHigh}		6		ns
Clock Low-Level Width <small>Note 3</small>	t_{COLow}		6		ns

Notes 1. Applied to all the interface pins except Status (3:0), BigEndian, DataRate, and Div4.

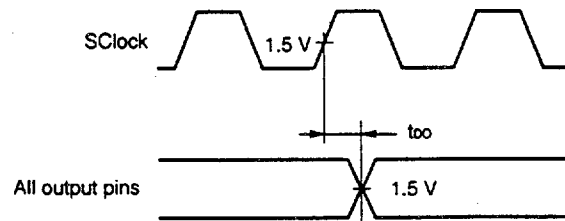
2. Applied to the BigEndian, DataRate, and Div4 pins. (However, the function of the Div4 is not supported by the current V_R4200.)

3. Applied to the RClock, TClock, and MaterOut pins.

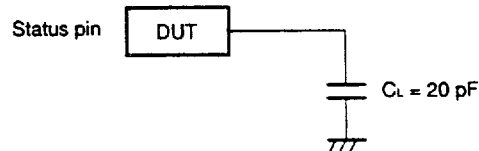
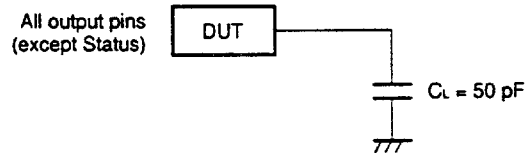
Load Coefficient

Parameter	Symbol	Condition	Rating		Unit
			MIN.	MAX.	
Load Coefficient	CLD			2	ns/25 pF

Test Condition

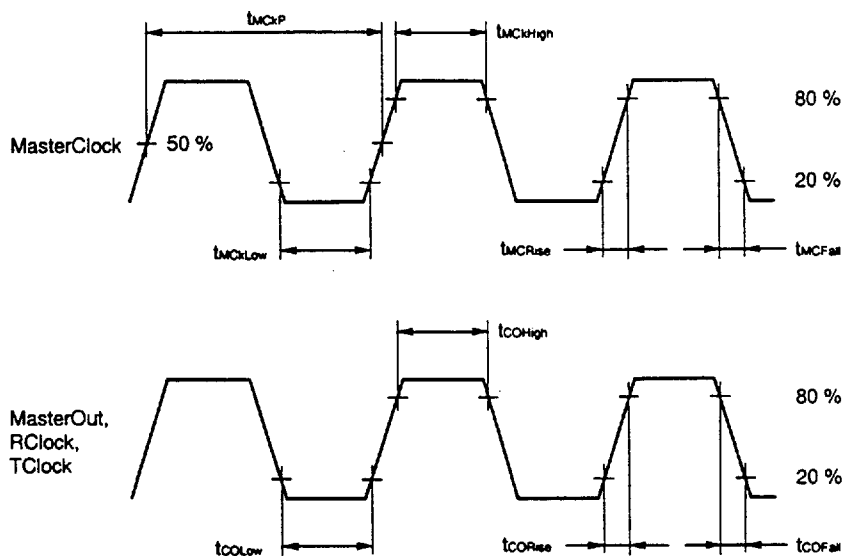


Test Load

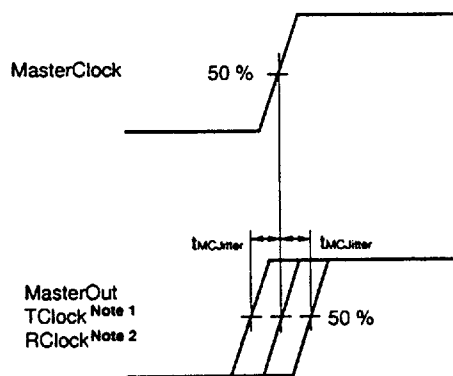


Timing Chart

Clock timing



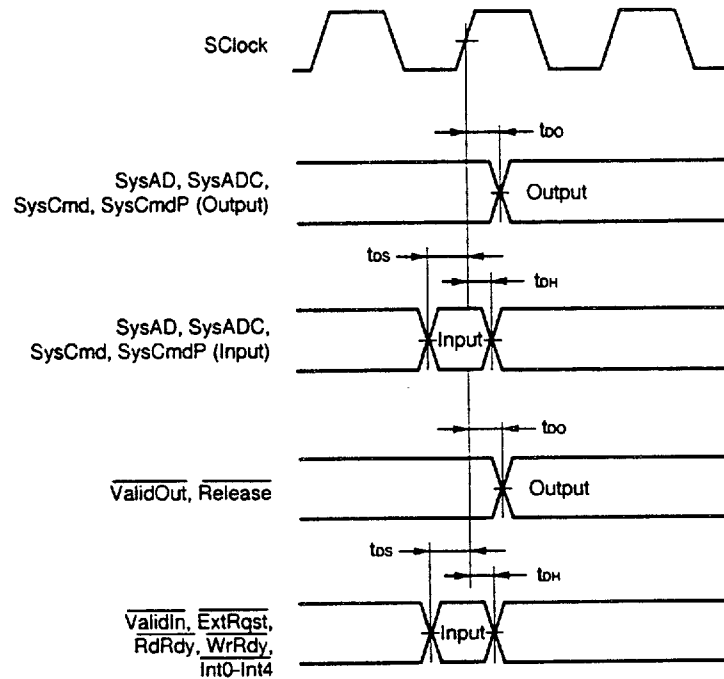
Clock jitter



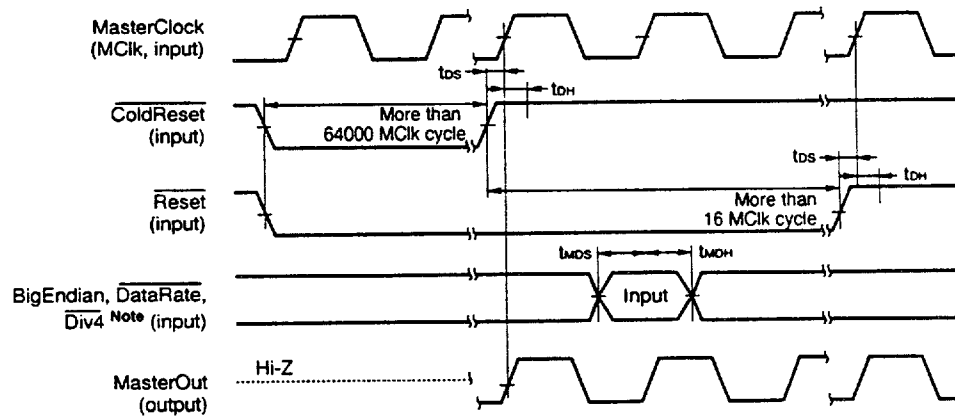
- Notes**
1. When SyncOut and SyncIn is connected with the shortest path, the point of TClock of 50% is the point of MasterClock of 50%.
 2. RClock advances TClock 90 degrees in phase.

Remark To match the MasterClock edge, keep the wiring capacitances of the SyncIn/SyncOut bus, TClock, and RClock the same.

System interface edge timing

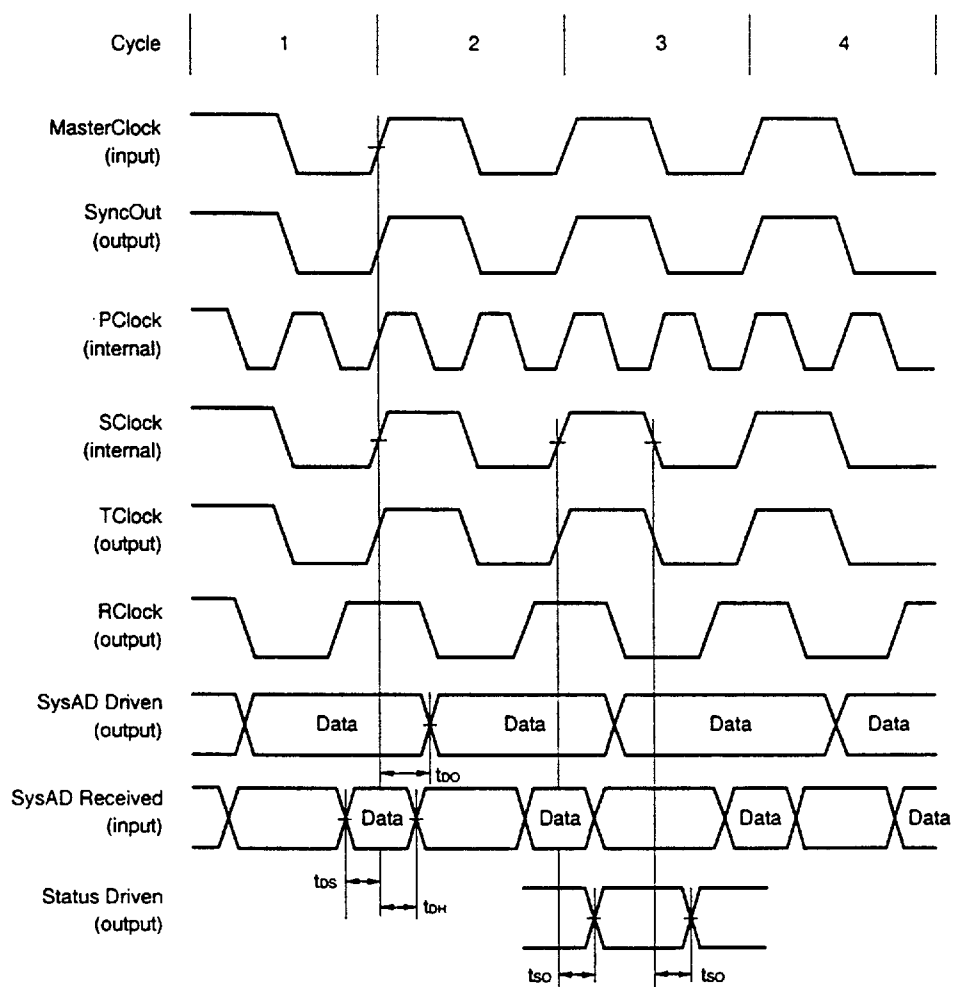


Reset timing



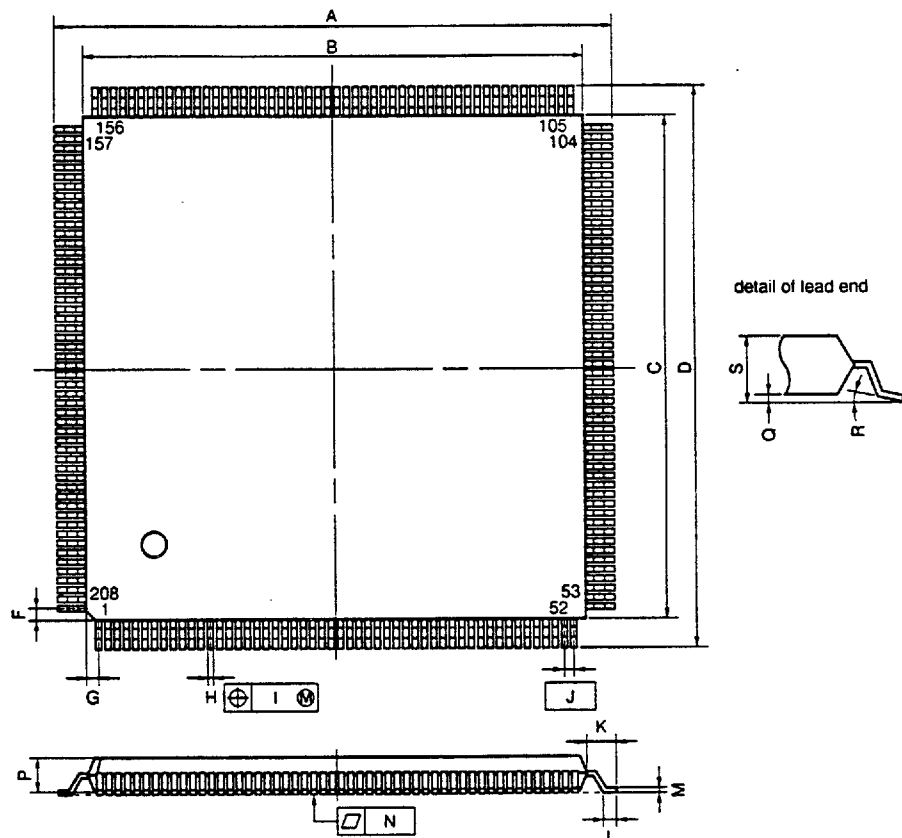
Note The function of the $\overline{\text{Div4}}$ pin is not supported by the current V_R4200.

Relations of clocking (Div2 mode)



8. PACKAGE DRAWING

208 PIN PLASTIC QFP (FINE PITCH) (□28)



NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	30.6±0.3	1.205±0.012
B	28.0±0.2	1.102 ^{+0.009} _{-0.008}
C	28.0±0.2	1.102 ^{+0.009} _{-0.008}
D	30.6±0.3	1.205±0.012
F	1.25	0.049
G	1.25	0.049
H	0.20±0.10	0.008±0.004
I	0.08	0.003
J	0.5 (T.P.)	0.020 (T.P.)
K	1.3±0.2	0.051±0.008
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.15±0.05	0.006±0.002
N	0.10	0.004
P	3.2	0.126
Q	0.4±0.1	0.016 ^{+0.004} _{-0.005}
R	5°±5°	5°±5°
S	3.8 MAX.	0.150 MAX.

P208GD-50-LML, MML-1

★ 9. RECOMMENDED SOLDERING CONDITIONS

Soldering this product under the following soldering conditions is recommended.

For the details of the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (IEI-1207)**.

For the soldering methods and recommended other than those recommended, consult NEC.

Table 9-1. Soldering Conditions of Surface Mount Type

μPD30450GD-80-MML: 208-pin plastic QFP (fine pitch) (28 × 28 mm)

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX. (210 °C MIN.), Number of times: 2 MAX., Number of days: 7 ^{Note} (After this, prebaking is necessary for 36 hours at 125 °C.) <Precaution> (1) Do not start second reflow until the device temperature that has risen as a result of the first reflow has dropped to room temperature. (2) Do not clean flux with water after the first reflow.	IR35-367-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX. (200 °C MIN.), Number of times: 2 MAX., Number of days: 7 ^{Note} (After this, prebaking is necessary for 36 hours at 125°C.) <Precaution> (1) Do not start second reflow until the device temperature that has risen as a result of the first reflow has dropped to room temperature. (2) Do not clean flux with water after the first reflow.	VP15-367-2
Pin partial heating	Pin temperature: 300 °C MAX., Time: 3 seconds MAX. (per side of device)	—

Note Number of days the device can be stored at 25 °C, 65 % RH after the dry pack has been opened.

Caution Do not use two or more soldering methods in combination (except the pin partial heating method).

APPENDIX DIFFERENCES AMONG V_R4200, V_R4000PC, AND V_R4400PC™

Item	V _R 4200	V _R 4000PC	V _R 4400PC
Operating Frequency (MHz)	Internal: 80 external: 40	Internal: 100, 80 external: 50, 40	Internal: 200, 150, 133, 100 external: 100, 75, 67, 50
Pipeline	5-stage pipeline	8-stage super pipeline	
Delay Slot	Branch: 1, load: 1	Branch: 3, load: 2	
FPU	Provided (common to integer operation block)	Provided	
Physical Address	33 bits	36 bits	
TLB	33 entry pairs	48 entry pairs	
Cache Size	Instruction: 16 KB, data: 8 KB	Instruction: 8 KB, data: 8 KB	Instruction: 16 KB, data: 16 KB
Cache Line Size	Instruction: 8 words, data: 4 words	4/8 words selectable	
System Interface Division Ratio (vs. PClock)	2/4 selectable ^{Note 1}	2/3/4 selectable	2/3/4/6/8 selectable
System Bus Check	Byte parity	ECC/byte parity selectable	
Write Data Transfer Rate	DDx/Dxx selectable (2 choices)	D-Dxxx selectable (9 choices)	
Bus Status of Unused Cycle	Holds value of previous cycle (only data at beginning and in middle of block)	Undefined	
Store Buffer	1 entry	None	1 entry
External Normal Interrupt	Int (4:0)	Int (5:0) (Int5 is shared by timer interrupt)	
Initial Setting at Reset	Set by dedicated pins (BigEndian, DataRate, Div4 ^{Note 2})	Set by BTMC (input from dedicated serial pin)	
Status Indication	Output from Status (3:0) pin	None	
Low Power Mode	Reduces power to 1/4	None	
PRId Register	Value of Imp area = 0×0A	Value of Imp area = 0×04	
Package	208-pin QFP	179-pin PGA	
Supply Voltage	3.3 V	5 V	5 V, 3.3 V (separate products)

Note 1. The current V_R4200 only support 2 division.

2. Setting by this function is not supported by the current V_R4200.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related documents VR4000, VR4400	User's manual – architecture (IEU-1344)
VR4000PC, VR4400PC	User's manual – hardware (IEU-1329)
VR4400PC	Data sheet (IC-3374)

Some related documents are preliminary versions. This document, however, is not indicated as "Preliminary".

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices in "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact NEC Sales Representative in advance.

Anti-radioactive design is not implemented in this product.

M4 94.11

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