

NEC

NEC Electronics Inc.

μPD4264800, 4265800**8,388,608 x 8-Bit****Dynamic CMOS RAM****Preliminary**

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Description

The μPD4264800 and μPD4265800 are 64M-bit dynamic RAMs organized as 8,388,608 words by 8 bits. They are designed to operate from a single +3.3-volt power supply and have an optional fast-page mode.

Advanced polycide technology minimizes silicon areas and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state outputs are controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{\text{CAS}}$ low. Data outputs return to high impedance when $\overline{\text{CAS}}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{\text{CAS}}$.

Refreshing may be accomplished by a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{\text{RAS}}$ -only refresh cycles or by normal read or write cycles during a 64-ms refresh period.

Two versions of the 8M x 8-bit DRAM are available. The μPD4264800 uses 8192 combinations of $A_0 - A_{12}$ for

$\overline{\text{RAS}}$ -only refreshing and 4096 address combinations of $A_0 - A_{11}$ to perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ and hidden refreshing of the memory during a 64-ms period. The μPD4265800 uses 4096 address combinations of $A_0 - A_{11}$ during a 64-ms period for all refresh modes.

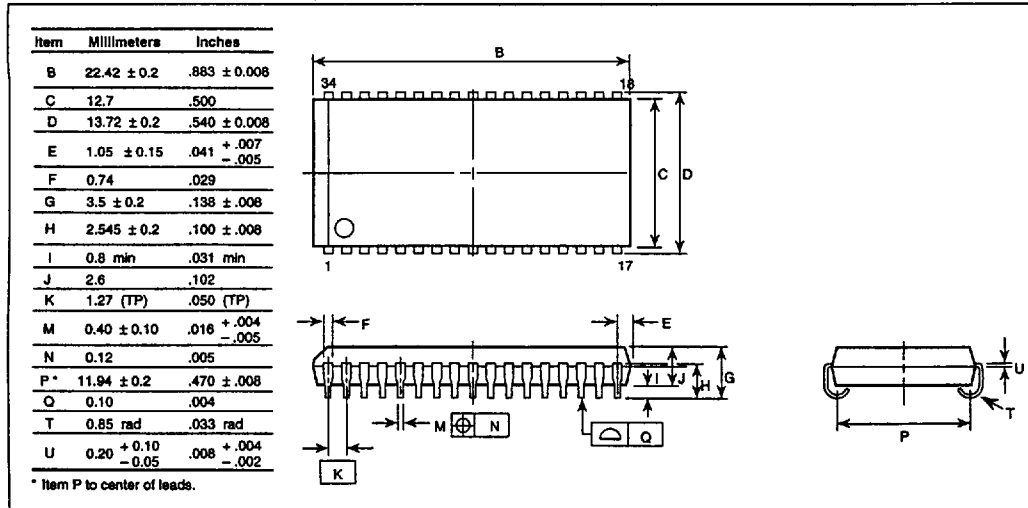
The μPD4264800 and μPD4265800 are available in a 34-pin plastic SOJ and 34-pin plastic TSOP.

Features

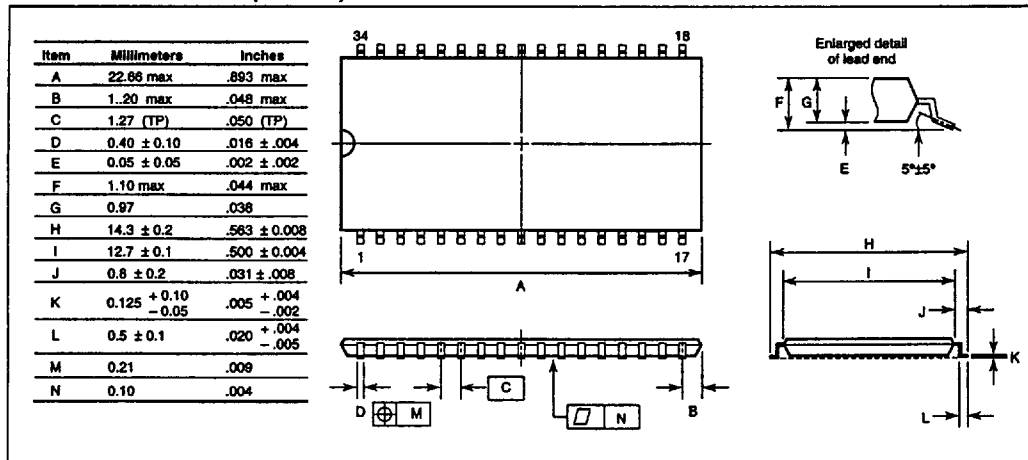
- 8,388,608 x 8-bit organization
- Single +3.3-volt power supply
- Fast-page option
- Low power dissipation: 1.80 mW (max) standby
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 34-pin plastic SOJ and TSOP packaging

Ordering Information

Part Number	Access Time (max)	R/W Cycle (max)	Fast-Page Cycle (max)	Active Power (max)	Package
μPD4264800LG-A50	50 ns	90 ns	35 ns	378 mW	34-pin plastic SOJ
-A60	60 ns	110 ns	40 ns	342 mW	
-A70	70 ns	130 ns	45 ns	306 mW	
-A80	80 ns	150 ns	50 ns	270 mW	
μPD4264800G7-A50	50 ns	90 ns	35 ns	378 mW	34-pin plastic TSOP
-A60	60 ns	110 ns	40 ns	342 mW	
-A70	70 ns	130 ns	45 ns	306 mW	
-A80	80 ns	150 ns	50 ns	270 mW	
μPD4265800LG-A50	50 ns	90 ns	35 ns	486 mW	34-pin plastic SOJ
-A60	60 ns	110 ns	40 ns	414 mW	
-A70	70 ns	130 ns	45 ns	378 mW	
-A80	80 ns	150 ns	50 ns	342 mW	
μPD4265800G7-A50	50 ns	90 ns	35 ns	486 mW	34-pin plastic TSOP
-A60	60 ns	110 ns	40 ns	414 mW	
-A70	70 ns	130 ns	45 ns	378 mW	
-A80	80 ns	150 ns	50 ns	342 mW	

μPD4264800, 4265800**34-Pin Plastic SOJ (500-mil)****SOJ or TSOP**

VCC	1	34	VSS
IO ₁	2	33	IO ₈
IO ₂	3	32	IO ₇
IO ₃	4	31	IO ₆
IO ₄	5	30	IO ₅
NC	6	29	VSS
VCC	7	28	CAS
WE	8	27	OE
RAS	9	26	NC
NC	10	25	A ₁₂
A ₀	11	24	A ₁₁
A ₁	12	23	A ₁₀
A ₂	13	22	A ₉
A ₃	14	21	A ₈
A ₄	15	20	A ₇
A ₅	16	19	A ₆
VCC	17	18	VSS

34-Pin Plastic TSOP (500 mil)

A ₀ to A ₁₁ (A ₁₂)	Address inputs
IO ₁ to IO ₈	Data inputs/outputs
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
OE	Output enable
VCC	Supply voltage
VSS	Ground
NC	No connection

NEC**NEC Electronics Inc.**

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