V96DPC Rev. B1

LOCAL BUS TO PCI BRIDGE FOR i960®Cx/Hx/Jx/Sx AND PowerPC™401Gx PROCESSORS

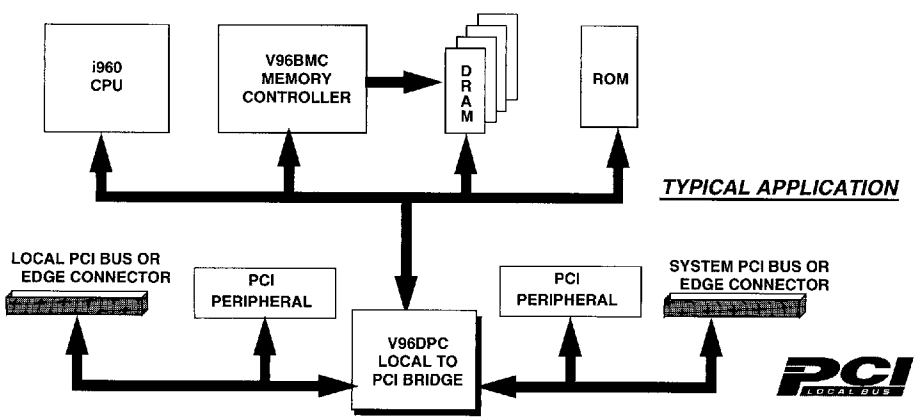
- Glueless interface between i960Sx/Jx/Cx/Hx, PPC401Gx processors and two PCI buses
- Provides PCI-to-PCI data bridging capability
- Each bridge is configurable for system master, bus master, or target operation
- Over 1K-byte FIFO using V3's unique *DYNAMIC BANDWIDTH ALLOCATION™* architecture
- Up to 33MHz PCI bus operation, independent of local processor speed
- Bi-Directional address space remapping
- On-the-fly byte order (endian) conversion
- 4 channel DMA controller
- Bi-directional mailboxes w/doorbell interrupts
- Support for real-mode DOS configuration
- Flexible PCI and local interrupt management
- Serial EEPROM configuration interface
- Fully compliant with PCI 2.1 specification
- Available in 33 and 40MHz versions
- 313-pin BGA package

The V96DPC delivers two independent i960-to-PCI bridges in a single low-cost component. It is ideal for PCI-based add-in cards. For example, when you need a PCI interface to the host slot or you have a large embedded systems with up to 8 PCI loads.

The V96DPC supports independent interface speeds allowing the PCI bus to run at the full 33 MHz frequency, regardless of processor clock rate. The unique *DYNAMIC BANDWIDTH ALLOCATION™* feature of the dual 576-byte FIFOs (>1K byte total) allows the designer to dynamically adjust the "draining" and "filling" of the read and write FIFOs to most efficiently meet the requirements of the data streams. Inclusion of this large FIFO array insures that high-speed peripherals - such as ATM and 100 Mbit Ethernet adapters - won't overrun the bridge's buffering capability.

The i960 processor gains access to the PCI bus through two programmable address apertures. Two more apertures are provided for PCI-to-local bus accesses. The V96DPC also includes bi-directional address remapping capabilities, and on-the-fly byte order conversion. The integrated DMA controllers provide a total of four channels. Each DMA channel can perform transfers from PCI-to-Local, Local-to-PCI, or PCI to PCI. Mailbox registers are provided for each bridge, and are accessible from all interfaces.

The V96DPC operates up to 40MHz, and is packaged in a 313-pin BGA.



This document contains the product codes, pinouts, package mechanical information, DC characteristics, and AC characteristics for the V96DPC. Detailed functional information is contained in the User's Manual.

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1.0 Product Codes

Table 1: Product Codes

Product Code	Processor	Bus Type	Package	Frequency
V96DPC-33LP	i960Cx/Hx/Jx/Sx PPC401GF	16/32-bit multiplexed 32-bit demultiplexed	313-pin BGA	33MHz
V96DPC-40LP	i960Cx/Hx/Jx/Sx PPC401GF	16/32-bit multiplexed 32-bit demultiplexed	313-pin BGA	40MHz

2.0 Pin Description and Pinout

Table 2 below lists the pin types found on the V96DPC. Table 3 describes the function of each pin on the V96DPC. Table 5 lists the pins by pin number. Figure 1 through Figure 3 show the pinout for the 313-pin BGA package and Figure 4 shows the mechanical dimensions of the package.

Table 2: Pin Types

Pin Type	Description
PCI I	PCI input only pin.
PCI O	PCI output only pin.
PCI I/O	PCI tri-state I/O pin.
PCI I/OD	PCI input with open drain output.
I/O_4	TTL I/O pin with 4mA output drive.
I	TTL input only pin.
O_4	TTL output pin with 4mA output drive.

Table 3: Signal Descriptions

Primary PCI Bus Interface			
Signal	**Type**	**R[a]**	**Description**
P_AD[31:0]	PCI I/O	Z	Address and data, multiplexed on the same pins.
P_C/$\overline{BE}$[3:0]	PCI I/O	Z	Bus Command and Byte Enables, multiplexed on the same pins.
P_PAR	PCI I/O	Z	Parity represents even parity across AD[31:0] and P_C/$\overline{BE}$[3:0].
$\overline{P\_FRAME}$	PCI I/O	Z	Cycle Frame indicates the beginning and burst length of an access.
$\overline{P\_IRDY}$	PCI I/O	Z	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
$\overline{P\_TRDY}$	PCI I/O	Z	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
$\overline{P\_STOP}$	PCI I/O	Z	Stop indicates the current target is requesting the master to stop the current transaction (retry or disconnect).
$\overline{P\_DEVSEL}$	PCI I/O	Z	Device Select, when actively driven by a target, indicates the driving device has decoded its address as the target of the current access. As an input to the initiator, $\overline{P\_DEVSEL}$ indicates whether any device on the bus has been selected.
P_IDSEL	PCI I		Initialization Device Select is used as a chip select during configuration read and write transactions. It must be driven high in order to access the chip's internal configuration space.
$\overline{P\_REQ}$	PCI O	H	Request indicates to the arbiter that this agent requests use of the bus.
$\overline{P\_GNT}$	PCI I		Grant indicates to the agent that access to the bus has been granted.
P_PCLK	PCI I		PCLK provides timing for all transactions on the Primary PCI bus.
$\overline{P\_PRST}$	PCI I/O	Z/L	Acts as an input when RDIR is high, an output when P_RDIR is low. As an input it is asserted low to bring all internal PBC operation to a reset state.
$\overline{P\_PERR}$	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
$\overline{P\_SERR}$	PCI I/OD	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
$\overline{P\_INT[A:D]}$	PCI I/OD	Z	Level-sensitive interrupt requests may be received or generated.

Secondary PCI Bus Interface			
Signal	**Type**	**R**	**Description**
S_AD[31:0]	PCI I/O	Z	Address and data, multiplexed on the same pins.
S_C/$\overline{BE}$[3:0]	PCI I/O	Z	Bus Command and Byte Enables, multiplexed on the same pins.

Table 3: Signal Descriptions (cont'd)

S_PAR	PCI I/O	Z	Parity represents even parity across AD[31:0] and S_C/$\overline{BE}$[3:0].
$\overline{S\_FRAME}$	PCI I/O	Z	Cycle Frame indicates the beginning and burst length of an access.
$\overline{S\_IRDY}$	PCI I/O	Z	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
$\overline{S\_TRDY}$	PCI I/O	Z	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
$\overline{S\_STOP}$	PCI I/O	Z	Stop indicates the current target is requesting the master to stop the current transaction (retry or disconnect).
$\overline{S\_DEVSEL}$	PCI I/O	Z	Device Select, when actively driven by a target, indicates the driving device has decoded its address as the target of the current access. As an input to the initiator, $\overline{S\_DEVSEL}$ indicates whether any device on the bus has been selected.
S_IDSEL	PCI I		Initialization Device Select is used as a chip select during configuration read and write transactions. It must be driven high in order to access the chip's internal configuration space.
$\overline{S\_REQ}$	PCI O	H	Request indicates to the arbiter that this agent requests use of the bus.
$\overline{S\_GNT}$	PCI I		Grant indicates to the agent that access to the bus has been granted.
S_PCLK	PCI I		PCLK provides timing for all transactions on the Secondary PCI bus.
$\overline{S\_PRST}$	PCI I/O	Z/L	Acts as an input when RDIR is high, an output when S_RDIR is low. As an input it is asserted low to bring all internal PBC operation to a reset state.
$\overline{S\_PERR}$	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
$\overline{S\_SERR}$	PCI I/OD	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
$\overline{S\_INT[A:D]}$	PCI I/OD	Z	Level-sensitive interrupt requests may be received or generated.

i960Sx Processor Interface			
Signal	**Type**	**R**	**Description**
LA[31:16]	I/O4	Z	Local address bus.
LAD[15:0]	I/O4	Z	Local multiplexed address and data bus.
LA[5:2]	I/O4	Z	Local address bus.
$\overline{BE}$[1:0]	I/O4	Z	Local bus byte enables.
W/$\overline{R}$	I/O4	Z	Write/Read.
ALE	I/O4	Z	Address Latch Enable: used to latch the address during the address phase.

Table 3: Signal Descriptions (cont'd)

$\overline{ADS}$	I/O4	Z	i960Sx $\overline{AS}$ signal. Asserted low to indicate the beginning of a bus cycle.
$\overline{READY}$	I/O4	Z	Local Bus data ready.
P_HOLD	O4	L	i960Sx HOLD signal. Primary Local bus hold request: asserted by the chip to initiate a local bus master cycle.
S_HOLD	O4	L	i960Sx HOLD signal. Secondary Local bus hold request: asserted by the chip to initiate a local bus master cycle.
P_HOLDA	I		i960Sx HLDA signal. Primary Local bus hold acknowledge.
S_HOLDA	I		i960Sx HLDA signal. Secondary Local bus hold acknowledge.
LPAR[1:0]	I/O4	Z	Local bus parity.
$\overline{BLAST}$	I/O4	Z	Burst last.
$\overline{P\_LINT}$	O4	H	i960Sx $\overline{LINT}$ signal. Primary Local interrupt request.
$\overline{S\_LINT}$	O4	H	i960Sx $\overline{LINT}$ signal. Secondary Local interrupt request.
$\overline{P\_LRST}$	I/O4	L/Z	i960Sx $\overline{LRST}$ signal. Primary Local bus RESET signal.
$\overline{S\_LRST}$	I/O4	L/Z	i960Sx $\overline{LRST}$ signal. Secondary Local bus RESET signal.
LCLK	I		Local bus clock.

i960Jx Processor Interface			
Signal	**Type**	**R**	**Description**
LAD[31:0]	I/O4	Z	Local multiplexed address and data bus.
LA[5:2]	I/O4	Z	Local address bus.
$\overline{BE[3:0]}$	I/O4	Z	Local bus byte enables.
W/$\overline{R}$	I/O4	Z	Write/Read.
ALE	I/O4	Z	Address Latch Enable: used to latch the address during the address phase.
$\overline{ADS}$	I/O4	Z	Asserted low to indicate the beginning of a bus cycle.
$\overline{RDYRCV}$	I/O4	Z	Local Bus data ready.
P_HOLD	O4	L	i960Jx HOLD signal. Primary Local bus hold request: asserted by the chip to initiate a local bus master cycle.
S_HOLD	O4	L	i960Jx HOLD signal. Secondary Local bus hold request: asserted by the chip to initiate a local bus master cycle.
P_HOLDA	I		i960Jx HOLDA signal. Primary Local bus hold acknowledge.
S_HOLDA	I		i960Jx HOLDA signal. Secondary Local bus hold acknowledge.
LPAR[3:0]	I/O4	Z	Local bus parity.
$\overline{BLAST}$	I/O4	Z	Burst last.
$\overline{BTERM}$	I/O4	Z	Bus Time-out. Burst terminate.
$\overline{P\_LINT}$	O4	H	i960Jx $\overline{LINT}$ signal. Primary Local interrupt request.

Table 3: Signal Descriptions (cont'd)

S_LINT	O4	H	i960Jx LINT signal. Secondary Local interrupt request.
P_LRST	I/O4	L/Z	i960Jx LRST signal. Primary Local bus RESET signal.
S_LRST	I/O4	L/Z	i960Jx LRST signal. Secondary Local bus RESET signal.
LCLK	I		Local bus clock.

i960Cx/Hx Processor Interface			
Signal	**Type**	**R**	**Description**
LD[31:0]	I/O4	Z	Local multiplexed address and data bus.
LA[31:2]	I/O4	Z	Local address bus.
BE[3:0]	I/O4	Z	Local bus byte enables.
W/R	I/O4	Z	Write/Read.
ADS	I/O4	Z	Asserted low to indicate the beginning of a bus cycle.
READY	I/O4	Z	Local Bus data ready
P_HOLD	O4	L	i960Cx/Hx HOLD signal. Primary Local bus hold request: asserted by the chip to initiate a local bus master cycle.
S_HOLD	O4	L	i960Cx/Hx HOLD signal. Secondary Local bus hold request: asserted by the chip to initiate a local bus master cycle.
P_HOLDA	I		i960Cx/Hx HOLDA signal. Primary Local bus hold acknowledge.
S_HOLDA	I		i960Cx/Hx HOLDA signal. Secondary Local bus hold acknowledge.
LPAR[3:0]	I/O4	Z	Local bus parity.
BLAST	I/O4	Z	Burst request. Burst last.
BTERM	I/O4	Z	Bus Time-out. Burst terminate.
P_LINT	O4	H	i960Cx/Hx LINT signal. Primary Local interrupt request.
S_LINT	O4	H	i960Cx/Hx LINT signal. Secondary Local interrupt request.
P_LRST	I/O4	L/Z	i960Cx/Hx LRST signal. Primary Local bus RESET signal.
S_LRST	I/O4	L/Z	i960Cx/Hx LRST signal. Secondary Local bus RESET signal.
LCLK	I		Local bus clock.

Serial EEPROM Interface			
Signal	**Type**	**R**	**Description**
P_SCL/LPERR	O4	X	Primary EEPROM clock. Local parity error.
S_SCL/LPERR	O4	X	Secondary EEPROM clock. Local parity error.
P_SDA	I/O4	X	Primary EEPROM data.
S_SDA	I/O4	X	Secondary EEPROM data.

Table 3: Signal Descriptions (cont'd)

Configuration			
Signal	**Type**	**R**	**Description**
P_RDIR	I		Primary Reset direction. Tie low to drive $\overline{\text{P\_PRST}}$ out and $\overline{\text{P\_LRST}}$ in, high to drive $\overline{\text{P\_LRST}}$ out and $\overline{\text{P\_PRST}}$ in.
S_RDIR	I		Secondary Reset direction. Tie low to drive $\overline{\text{S\_PRST}}$ out and $\overline{\text{S\_LRST}}$ in, high to drive $\overline{\text{S\_LRST}}$ out and $\overline{\text{S\_PRST}}$ in.

Power and Ground Signals			
Signal	**Type**	**R**	**Description**
V_{CC}	-		POWER leads intended for external connection to a V_{CC} board plane.
GND	-		GROUND leads intended for external connection to a GND board plane.

a. **R** indicates state during reset.

2.1 Test Mode Pins

Several device pins are used to put the V96DPC device into various test modes. ***These pins must be maintained at proper levels during reset to insure proper operation.*** This is typically handled through pull-up or pull-down resistors (typically 1K to 10K) on the signal pins if they are not guaranteed to be at the proper level during reset. Table 4 below shows the reset states for test mode pins:

Table 4: RESET State for Test Mode Pins

Processor	AE7 Pin	Y6 Pin	AB2 Pin
i960Sx	Pull-Down	Pull-Down	Pull-Down
i960Jx PPC401GF	Pull-Down	Pull-Up	Pull-Down
i960Cx/Hx	Pull-Up	Pull-Up	Pull-Up

Table 5: Pin Assignments

Pin #	i960Sx	i960Jx	i960Cx/Hx	Pin #	i960Sx	i960Jx	i960Cx/Hx
A1	P_AD0	P_AD0	P_AD0	P2	NC	NC	NC
A3	P_AD1	P_AD1	P_AD1	P4	NC	NC	NC
A5	P_AD2	P_AD2	P_AD2	P6	NC	NC	NC
A7	P_AD3	P_AD3	P_AD3	P8	NC	NC	NC
A9	P_AD4	P_AD4	P_AD4	P10	GND	GND	GND
A11	P_AD5	P_AD5	P_AD5	P12	GND	GND	GND
A13	NC	NC	NC	P14	GND	GND	GND
A15	S_AD0	S_AD0	S_AD0	P16	GND	GND	GND
A17	S_AD1	S_AD1	S_AD1	P18	NC	NC	NC
A19	S_AD2	S_AD2	S_AD2	P20	NC	NC	NC
A21	S_AD3	S_AD3	S_AD3	P22	NC	NC	NC
A23	S_AD4	S_AD4	S_AD4	P24	NC	NC	NC
A25	S_AD5	S_AD5	S_AD5	R1	NC	NC	NC
B2	P_AD6	P_AD6	P_AD6	R3	NC	NC	NC
B4	P_AD7	P_AD7	P_AD7	R5	NC	NC	NC
B6	P_C/$\overline{BE0}$	P_C/$\overline{BE0}$	P_C/$\overline{BE0}$	R7	NC	NC	NC
B8	P_AD8	P_AD8	P_AD8	R9	V_{CC}	V_{CC}	V_{CC}
B10	P_AD9	P_AD9	P_AD9	R11	GND	GND	GND
B12	P_AD10	P_AD10	P_AD10	R13	GND	GND	GND
B14	S_AD6	S_AD6	S_AD6	R15	GND	GND	GND
B16	S_AD7	S_AD7	S_AD7	R17	V_{CC}	V_{CC}	V_{CC}
B18	S_C/$\overline{BE0}$	S_C/$\overline{BE0}$	S_C/$\overline{BE0}$	R19	NC	NC	NC
B20	S_AD8	S_AD8	S_AD8	R21	NC	NC	NC
B22	S_AD9	S_AD9	S_AD9	R23	NC	NC	NC
B24	S_AD10	S_AD10	S_AD10	R25	NC	NC	NC
C1	P_AD11	P_AD11	P_AD11	T2	NC	NC	NC
C3	P_AD12	P_AD12	P_AD12	T4	NC	NC	NC
C5	P_AD13	P_AD13	P_AD13	T6	NC	NC	NC
C7	P_AD14	P_AD14	P_AD14	T8	NC	NC	NC
C9	P_AD15	P_AD15	P_AD15	T10	V_{CC}	V_{CC}	V_{CC}
C11	P_C/$\overline{BE1}$	P_C/$\overline{BE1}$	P_C/$\overline{BE1}$	T12	GND	GND	GND
C13	NC	NC	NC	T14	GND	GND	GND
C15	S_AD11	S_AD11	S_AD11	T16	V_{CC}	V_{CC}	V_{CC}
C17	S_AD12	S_AD12	S_AD12	T18	NC	NC	NC

Table 5: Pin Assignments (cont'd)

Pin #	i960Sx	i960Jx	i960Cx/Hx	Pin #	i960Sx	i960Jx	i960Cx/Hx
C19	S_AD13	S_AD13	S_AD13	T20	NC	NC	NC
C21	S_AD14	S_AD14	S_AD14	T22	NC	NC	NC
C23	S_AD15	S_AD15	S_AD15	T24	NC	NC	NC
C25	S_C/$\overline{BE1}$	S_C/$\overline{BE1}$	S_C/$\overline{BE1}$	U1	$\overline{S\_LINT}$	$\overline{S\_LINT}$	$\overline{S\_LINT}$
D2	P_PAR	P_PAR	P_PAR	U3	$\overline{BE0}$	$\overline{BE0}$	$\overline{BE0}$
D4	$\overline{P\_SERR}$	$\overline{P\_SERR}$	$\overline{P\_SERR}$	U5	NC	NC	NC
D6	$\overline{P\_PERR}$	$\overline{P\_PERR}$	$\overline{P\_PERR}$	U7	NC	NC	NC
D8	$\overline{P\_STOP}$	$\overline{P\_STOP}$	$\overline{P\_STOP}$	U9	NC	NC	NC
D10	$\overline{P\_DEVSEL}$	$\overline{P\_DEVSEL}$	$\overline{P\_DEVSEL}$	U11	V_{CC}	V_{CC}	V_{CC}
D12	$\overline{P\_TRDY}$	$\overline{P\_TRDY}$	$\overline{P\_TRDY}$	U13	V_{CC}	V_{CC}	V_{CC}
D14	S_PAR	S_PAR	S_PAR	U15	V_{CC}	V_{CC}	V_{CC}
D16	$\overline{S\_SERR}$	$\overline{S\_SERR}$	$\overline{S\_SERR}$	U17	NC	NC	NC
D18	$\overline{S\_PERR}$	$\overline{S\_PERR}$	$\overline{S\_PERR}$	U19	NC	NC	NC
D20	$\overline{S\_STOP}$	$\overline{S\_STOP}$	$\overline{S\_STOP}$	U21	NC	NC	NC
D22	$\overline{S\_DEVSEL}$	$\overline{S\_DEVSEL}$	$\overline{S\_DEVSEL}$	U23	NC	NC	NC
D24	$\overline{S\_TRDY}$	$\overline{S\_TRDY}$	$\overline{S\_TRDY}$	U25	NC	NC	NC
E1	$\overline{P\_IRDY}$	$\overline{P\_IRDY}$	$\overline{P\_IRDY}$	V2	$\overline{P\_LRST}$	$\overline{P\_LRST}$	$\overline{P\_LRST}$
E3	$\overline{P\_FRAME}$	$\overline{P\_FRAME}$	$\overline{P\_FRAME}$	V4	LCLK	LCLK	LCLK
E5	P_C/$\overline{BE2}$	P_C/$\overline{BE2}$	P_C/$\overline{BE2}$	V6	NC	NC	NC
E7	P_AD16	P_AD16	P_AD16	V8	NC	NC	NC
E9	P_AD17	P_AD17	P_AD17	V10	NC	NC	NC
E11	P_AD18	P_AD18	P_AD18	V12	NC	NC	NC
E13	NC	NC	NC	V14	NC	NC	NC
E15	$\overline{S\_IRDY}$	$\overline{S\_IRDY}$	$\overline{S\_IRDY}$	V16	NC	NC	NC
E17	$\overline{S\_FRAME}$	$\overline{S\_FRAME}$	$\overline{S\_FRAME}$	V18	NC	NC	NC
E19	S_C/$\overline{BE2}$	S_C/$\overline{BE2}$	S_C/$\overline{BE2}$	V20	NC	NC	NC
E21	S_AD16	S_AD16	S_AD16	V22	NC	NC	NC
E23	S_AD17	S_AD17	S_AD17	V24	NC	NC	NC
E25	S_AD18	S_AD18	S_AD18	W1	P_SDA	P_SDA	P_SDA
F2	P_AD19	P_AD19	P_AD19	W3	$\overline{BLAST}$	$\overline{BLAST}$	$\overline{BLAST}$
F4	P_AD20	P_AD20	P_AD20	W5	P_HOLDA	P_HOLDA	P_HOLDA
F6	P_AD21	P_AD21	P_AD21	W7	LA29	LAD29	LD29
F8	P_AD22	P_AD22	P_AD22	W9	LA5	LA5	LA5
F10	P_AD23	P_AD23	P_AD23	W11	LA23	LAD23	LD23
F12	P_IDSEL	P_IDSEL	P_IDSEL	W13	reserved	reserved	LA11

Table 5: Pin Assignments (cont'd)

Pin #	i960Sx	i960Jx	i960Cx/Hx	Pin #	i960Sx	i960Jx	i960Cx/Hx
F14	S_AD19	S_AD19	S_AD19	W15	LA16	LAD16	LD16
F16	S_AD20	S_AD20	S_AD20	W17	reserved	reserved	LA18
F18	S_AD21	S_AD21	S_AD21	W19	LAD9	LAD9	LD9
F20	S_AD22	S_AD22	S_AD22	W21	LAD7	LAD7	LD7
F22	S_AD23	S_AD23	S_AD23	W23	reserved	reserved	LA28
F24	S_IDSEL	S_IDSEL	S_IDSEL	W25	LD0	LAD0	LD0
G1	P_C/$\overline{BE3}$	P_C/$\overline{BE3}$	P_C/$\overline{BE3}$	Y2	$\overline{S\_LRST}$	$\overline{S\_LRST}$	$\overline{S\_LRST}$
G3	P_AD24	P_AD24	P_AD24	Y4	reserved	$\overline{BE3}$	$\overline{BE3}$
G5	P_AD25	P_AD25	P_AD25	Y6	'0'	$\overline{BTERM}$	$\overline{BTERM}$
G7	P_AD26	P_AD26	P_AD26	Y8	LA3	LA3	LA3
G9	P_AD27	P_AD27	P_AD27	Y10	LA24	LAD24	LD24
G11	P_AD28	P_AD28	P_AD28	Y12	reserved	reserved	LA9
G13	NC	NC	NC	Y14	LA18	LAD18	LD18
G15	S_C/$\overline{BE3}$	S_C/$\overline{BE3}$	S_C/$\overline{BE3}$	Y16	reserved	reserved	LA16
G17	S_AD24	S_AD24	S_AD24	Y18	LAD11	LAD11	LD11
G19	S_AD25	S_AD25	S_AD25	Y20	reserved	reserved	LA23
G21	S_AD26	S_AD26	S_AD26	Y22	reserved	reserved	LA26
G23	S_AD27	S_AD27	S_AD27	Y24	LAD2	LAD2	LD2
G25	S_AD28	S_AD28	S_AD28	AA1	P_SCL/ $\overline{LPERR}$	P_SCL/ $\overline{LPERR}$	P_SCL/ $\overline{LPERR}$
H2	P_AD29	P_AD29	P_AD29	AA3	W/$\overline{R}$	W/$\overline{R}$	W/$\overline{R}$
H4	P_AD30	P_AD30	P_AD30	AA5	S_HOLD	S_HOLD	S_HOLD
H6	P_AD31	P_AD31	P_AD31	AA7	LA30	LAD30	LD30
H8	$\overline{P\_REQ}$	$\overline{P\_REQ}$	$\overline{P\_REQ}$	AA9	LA26	LAD26	LD26
H10	$\overline{P\_GNT}$	$\overline{P\_GNT}$	$\overline{P\_GNT}$	AA11	reserved	reserved	LA7
H12	P_PCLK	P_PCLK	P_PCLK	AA13	LA20	LAD20	LD20
H14	S_AD29	S_AD29	S_AD29	AA15	reserved	reserved	LA14
H16	S_AD30	S_AD30	S_AD30	AA17	LAD13	LAD13	LD13
H18	S_AD31	S_AD31	S_AD31	AA19	reserved	reserved	LA21
H20	$\overline{S\_REQ}$	$\overline{S\_REQ}$	$\overline{S\_REQ}$	AA21	reserved	reserved	LA24
H22	$\overline{S\_GNT}$	$\overline{S\_GNT}$	$\overline{S\_GNT}$	AA23	LAD4	LAD4	LD4
H24	S_PCLK	S_PCLK	S_PCLK	AA25	reserved	reserved	LA31
J1	$\overline{P\_PRST}$	$\overline{P\_PRST}$	$\overline{P\_PRST}$	AB2	'0'	'0'	'1'
J3	$\overline{P\_INTD}$	$\overline{P\_INTD}$	$\overline{P\_INTD}$	AB4	reserved	$\overline{BE2}$	$\overline{BE2}$
J5	$\overline{P\_INTC}$	$\overline{P\_INTC}$	$\overline{P\_INTC}$	AB6	$\overline{READY}$	$\overline{READY}$	$\overline{READY}$

Table 5: Pin Assignments (cont'd)

Pin #	i960Sx	i960Jx	i960Cx/Hx	Pin #	i960Sx	i960Jx	i960Cx/Hx
J7	$\overline{\text{P\_INTB}}$	$\overline{\text{P\_INTB}}$	$\overline{\text{P\_INTB}}$	AB8	LA28	LAD28	LD28
J9	$\overline{\text{P\_INTA}}$	$\overline{\text{P\_INTA}}$	$\overline{\text{P\_INTA}}$	AB10	reserved	reserved	LA6
J11	V_{CC}	V_{CC}	V_{CC}	AB12	LA22	LAD22	LD22
J13	V_{CC}	V_{CC}	V_{CC}	AB14	reserved	reserved	LA12
J15	V_{CC}	V_{CC}	V_{CC}	AB16	LAD15	LAD15	LD15
J17	$\overline{\text{S\_PRST}}$	$\overline{\text{S\_PRST}}$	$\overline{\text{S\_PRST}}$	AB18	reserved	reserved	LA19
J19	$\overline{\text{S\_INTD}}$	$\overline{\text{S\_INTD}}$	$\overline{\text{S\_INTD}}$	AB20	LAD8	LAD8	LD8
J21	$\overline{\text{S\_INTC}}$	$\overline{\text{S\_INTC}}$	$\overline{\text{S\_INTC}}$	AB22	LAD6	LAD6	LD6
J23	$\overline{\text{S\_INTB}}$	$\overline{\text{S\_INTB}}$	$\overline{\text{S\_INTB}}$	AB24	reserved	reserved	LA29
J25	$\overline{\text{S\_INTA}}$	$\overline{\text{S\_INTA}}$	$\overline{\text{S\_INTA}}$	AC1	S_SDA	S_SDA	S_SDA
K2	NC	NC	NC	AC3	P_RDIR	P_RDIR	P_RDIR
K4	NC	NC	NC	AC5	S_HOLDA	S_HOLDA	S_HOLDA
K6	NC	NC	NC	AC7	LA31	LAD31	LD31
K8	NC	NC	NC	AC9	LA4	LA4	LA4
K10	V_{CC}	V_{CC}	V_{CC}	AC11	LPAR2	LPAR2	LPAR2
K12	GND	GND	GND	AC13	reserved	reserved	LA10
K14	GND	GND	GND	AC15	LA17	LAD17	LD17
K16	V_{CC}	V_{CC}	V_{CC}	AC17	reserved	reserved	LA17
K18	NC	NC	NC	AC19	LAD10	LAD10	LD10
K20	NC	NC	NC	AC21	LPAR0	LPAR0	LPAR0
K22	NC	NC	NC	AC23	reserved	reserved	LA27
K24	NC	NC	NC	AC25	LAD1	LAD1	LD1
L1	NC	NC	NC	AD2	$\overline{\text{P\_LINT}}$	$\overline{\text{P\_LINT}}$	$\overline{\text{P\_LINT}}$
L3	NC	NC	NC	AD4	$\overline{\text{BE1}}$	$\overline{\text{BE1}}$	$\overline{\text{BE1}}$
L5	NC	NC	NC	AD6	P_HOLD	P_HOLD	P_HOLD
L7	NC	NC	NC	AD8	LA2	LA2	LA2
L9	V_{CC}	V_{CC}	V_{CC}	AD10	LA25	LAD25	LD25
L11	GND	GND	GND	AD12	reserved	reserved	LA8
L13	GND	GND	GND	AD14	LA19	LAD19	LD19
L15	GND	GND	GND	AD16	reserved	reserved	LA15
L17	V_{CC}	V_{CC}	V_{CC}	AD18	LAD12	LAD12	LD12
L19	NC	NC	NC	AD20	reserved	reserved	LA22
L21	NC	NC	NC	AD22	reserved	reserved	LA25
L23	NC	NC	NC	AD24	LAD3	LAD3	LD3

Table 5: Pin Assignments (cont'd)

Pin #	i960Sx	i960Jx	i960Cx/Hx	Pin #	i960Sx	i960Jx	i960Cx/Hx
L25	NC	NC	NC	AE1	S_SCL/ $\overline{\text{LPERR}}$	S_SCL/ $\overline{\text{LPERR}}$	S_SCL/ $\overline{\text{LPERR}}$
M2	NC	NC	NC	AE3	S_RDIR	S_RDIR	S_RDIR
M4	NC	NC	NC	AE5	$\overline{\text{ADS}}$	$\overline{\text{ADS}}$	$\overline{\text{ADS}}$
M6	NC	NC	NC	AE7	ALE	ALE	'1'
M8	NC	NC	NC	AE9	LA27	LAD27	LD27
M10	GND	GND	GND	AE11	LPAR3	LPAR3	LPAR3
M12	GND	GND	GND	AE13	LA21	LAD21	LD21
M14	GND	GND	GND	AE15	reserved	reserved	LA13
M16	GND	GND	GND	AE17	LAD14	LAD14	LD14
M18	NC	NC	NC	AE19	reserved	reserved	LA20
M20	NC	NC	NC	AE21	LPAR1	LPAR1	LPAR1
M22	NC	NC	NC	AE23	LAD5	LAD5	LD5
M24	NC	NC	NC	AE25	reserved	reserved	LA30
N1	NC	NC	NC				
N3	NC	NC	NC				
N5	NC	NC	NC				
N7	NC	NC	NC				
N9	V_{CC}	V_{CC}	V_{CC}				
N11	GND	GND	GND				
N13	GND	GND	GND				
N15	GND	GND	GND				
N17	V_{CC}	V_{CC}	V_{CC}				
N19	NC	NC	NC				
N21	NC	NC	NC				
N23	NC	NC	NC				
N25	NC	NC	NC				

Figure 1: V96DPC 313-pin BGA Pinout (i960Sx Configuration)

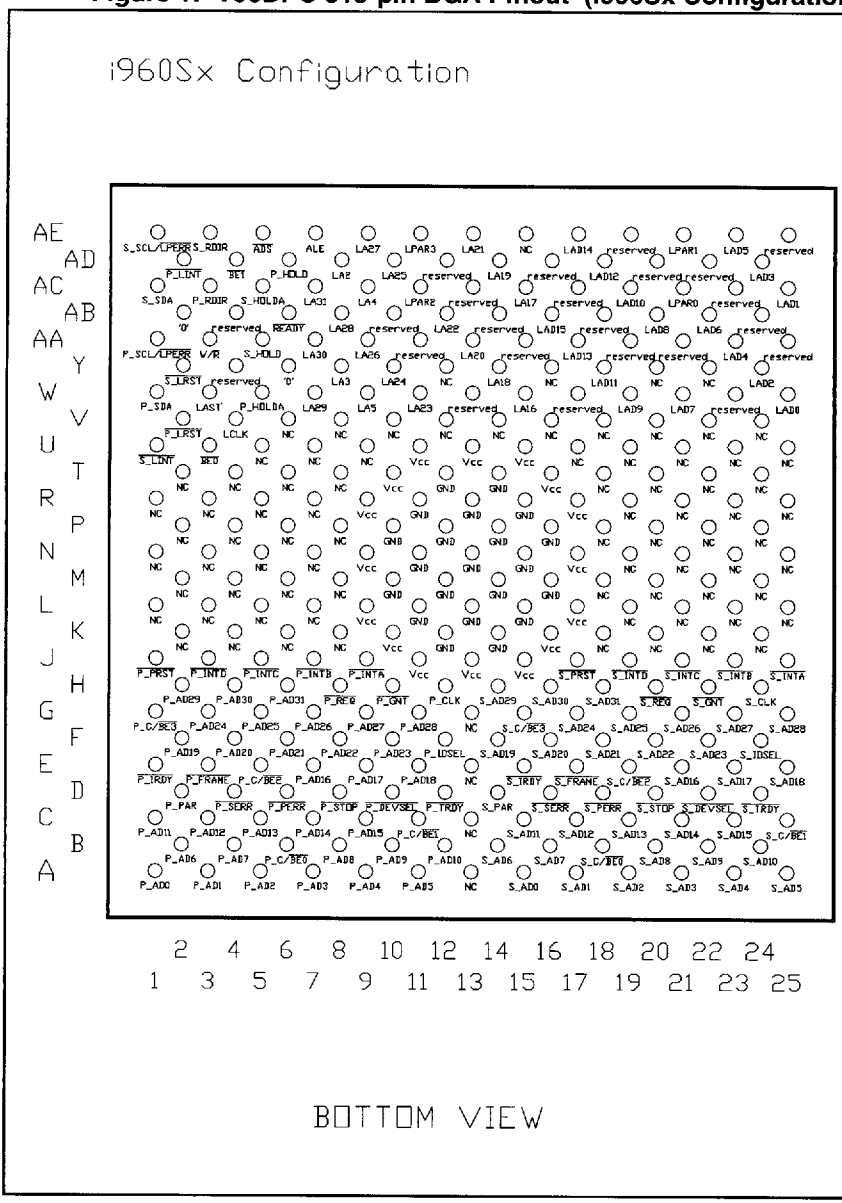


Figure 2: V96DPC 313-pin BGA Pinout (i960Jx Configuration)

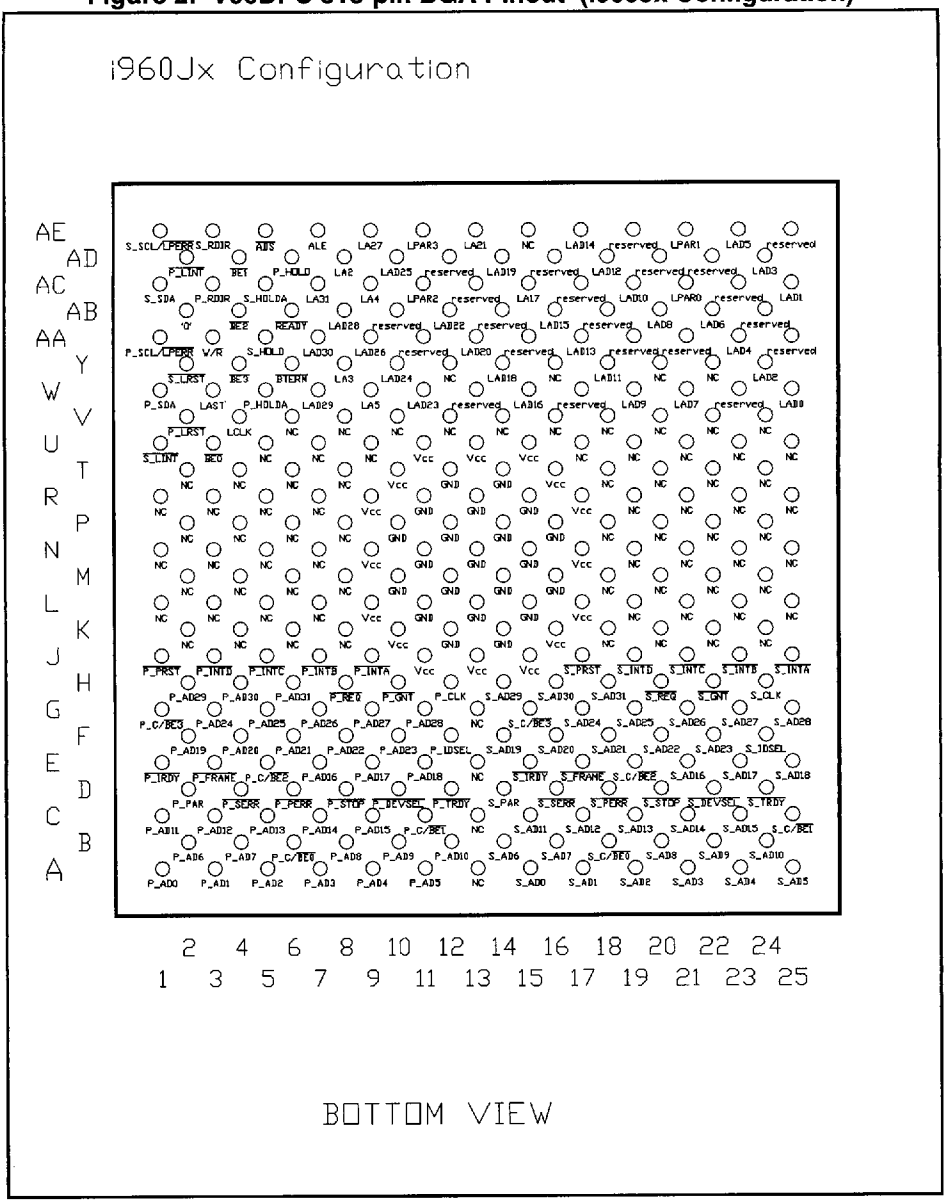


Figure 3: V96DPC 313-pin BGA Pinout (i960Cx/Hx Configuration)

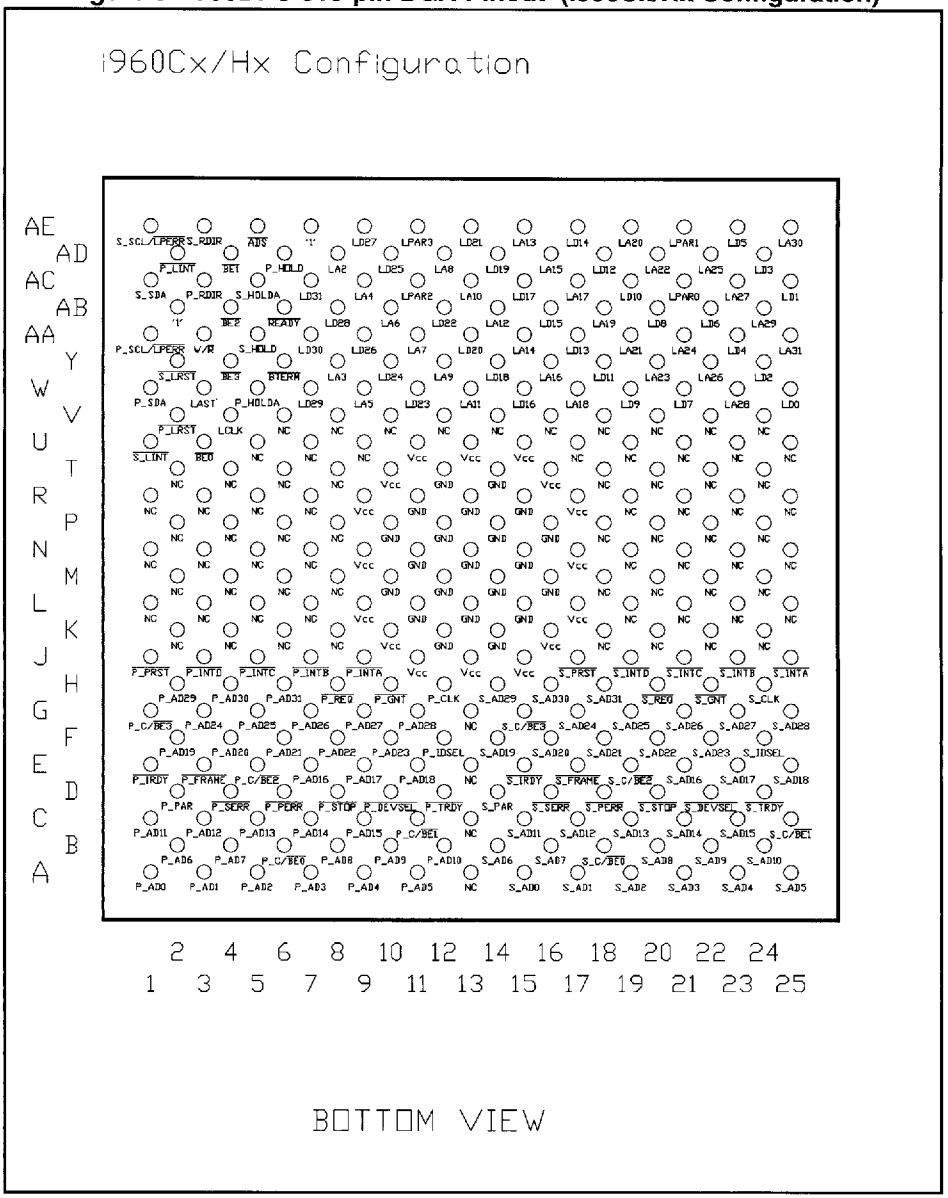
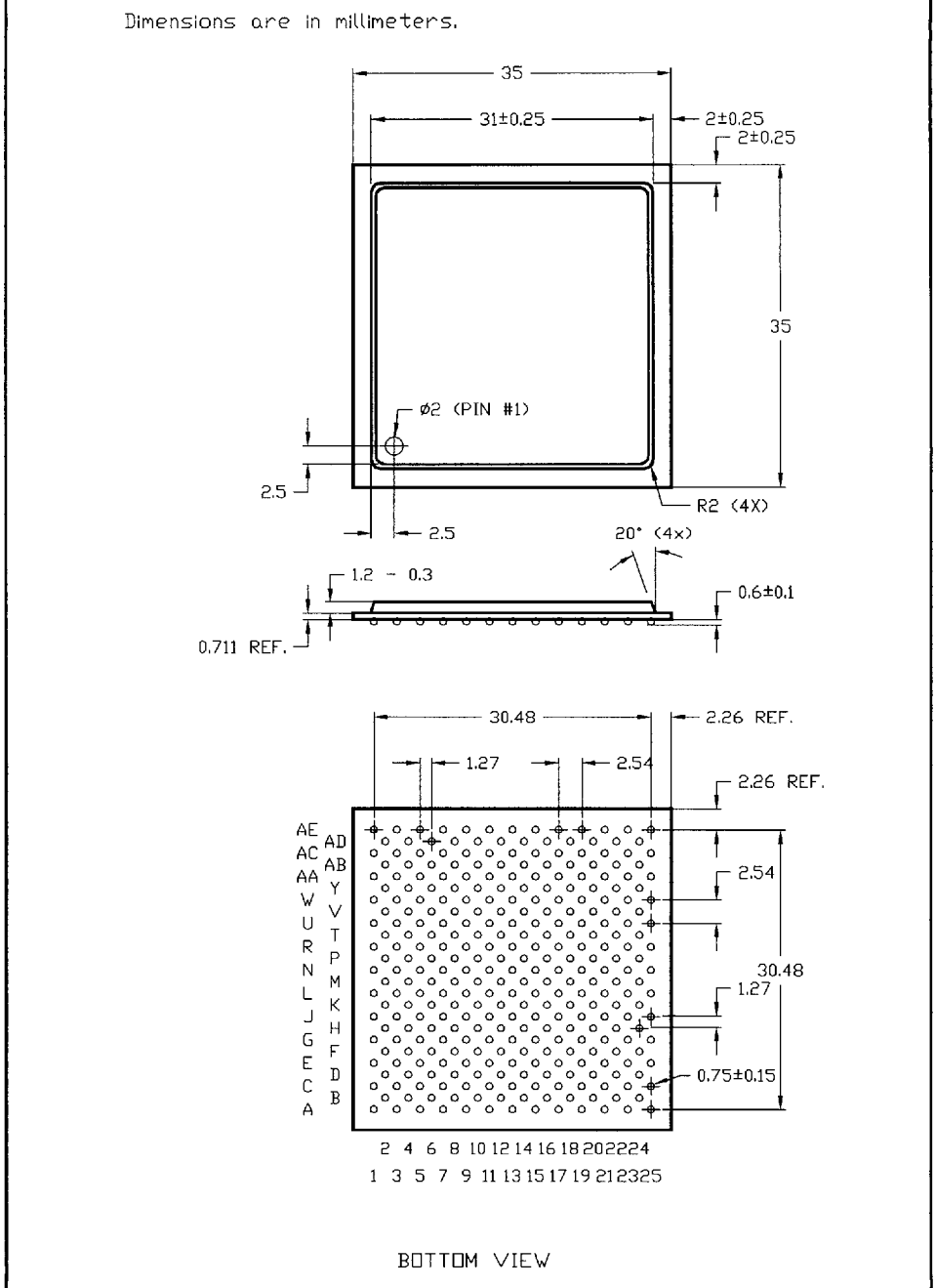


Figure 4: 313-pin BGA mechanical details



3.0 DC Specifications

The DC specifications for the PCI bus signals match exactly those given in the PCI Specification, Rev. 2.1, Section 4.2.1.1. For more information on the PCI DC specifications, see the PCI Specification.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	-0.3 to +7	V
V_{IN}	DC input voltage	-0.3 to V_{CC}+0.3	V
I_{IN}	DC input current	± 10	mA
T_{STG}	Storage temperature range	-40 to +125	°C

Table 7: Guaranteed Operating Conditions

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	4.75 to 5.25	V
T_A	Ambient temperature range	0 to 70	°C

3.1 PCI Bus DC Specifications

Table 8: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{IH}	Input high voltage		2.0	V_{CC}+0.5	V	
V_{IL}	Input low voltage		-0.5	0.8	V	
I_{IH}	Input high leakage current	V_{IN} = 2.7V		70	µA	1
I_{IL}	Input low leakage current	V_{IN} = 0.5V		-70	µA	1
V_{OH}	Output high voltage	I_{OUT} = -2mA	2.4		V	
V_{OL}	Output low voltage	I_{OUT} = 3mA, 6mA		0.55	V	2
C_{IN}	Input pin capacitance			10	pF	3
C_{CLK}	PCLK pin capacitance		5	12	pF	
C_{IDSEL}	IDSEL pin capacitance			8	pF	4
L_{PIN}	Pin inductance			20	nH	

Notes:
1. Input leakage currents include high impedance output leakage for all bi-directional buffers with tri-state outputs.
2. Signals without pullup resistors have greater than 3mA low output current. Signals requiring pull resistors have greater than 6mA output current. The latter include $\overline{\text{P\_FRAME}}$, $\overline{\text{S\_FRAME}}$, $\overline{\text{P\_TRDY}}$, $\overline{\text{S\_TRDY}}$, $\overline{\text{P\_IRDY}}$, $\overline{\text{S\_IRDY}}$, $\overline{\text{P\_STOP}}$, $\overline{\text{S\_STOP}}$, $\overline{\text{P\_SERR}}$, $\overline{\text{S\_SERR}}$, $\overline{\text{P\_PERR}}$, $\overline{\text{S\_PERR}}$.
3. Absolute maximum pin capacitance for a PCI unit is 10pF (except for P_PCLK and S_PCLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to P_AD[xx] and S_AD[xx].

3.2 Local Bus DC Specifications

Table 9: Local Bus Signals DC Operating Specifications

Symbol	Description	Conditions	Min	Max	Units
V_{IL}	Low level input voltage	V_{CC} = 4.75V		0.8	V
V_{IH}	High level input voltage	V_{CC} = 5.25V	2.0		V
I_{IL}	Low level input current	V_{IN}=GND, V_{CC}=5.25V	-10		µA
I_{IH}	High level input current	V_{IN} = V_{CC} = 5.25V		10	µA
V_{OL4}	Low level output voltage for 4 mA outputs and I/O pins	I_{OL} = -4 mA		0.4	V
V_{OH4}	High level output voltage for 4 mA outputs and I/O pins	I_{OH} = 4 mA	2.4		V
I_{OZL}	Low level float input leakage	V_{IN} = GND	-10		µA
I_{OZH}	High level float input leakage	V_{IN} = V_{CC}		10	µA
I_{CC} (max)	Maximum supply current	V_{CC} = 5.25V P_PCLK = P_PCLK = S_PCLK = S_LCLK = 33MHz		300	mA
I_{CC} (typ)	Typical supply current	V_{CC} = 5.0V P_PCLK = P_PCLK = S_PCLK = S_LCLK = 33MHz		240	mA
C_{IO}	Input and output capacitance			10	pF

4.0 AC Specifications

The AC specifications for the PCI bus signals match exactly those given in the PCI Specification, Rev. 2.1, Section 4.2.1.2. For more information on the PCI AC specifications, including the V/I curves for 5V signalling, see section 4.2.1.2 of Rev 2.1 PCI Specification.

4.1 PCI Bus Timings

Table 10: PCI Bus Signals AC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
$I_{OH(AC)}$	Switching current high	$0V<V_{OUT}\leq 1.4V$	-44		mA	1
		$1.4V<V_{OUT}<2.4V$	$-44+(V_{OUT}-1.4)/0.024$	Equation A	mA	1, 2, 3
	(Test point)	$V_{OUT}=3.1V$		-142	mA	3
$I_{OL(AC)}$	Switching current low	$V_{OUT}\geq 2.2V$	95		mA	1
		$2.2V>V_{OUT}>0.55$	$V_{OUT}/0.023$	Equation B	mA	1, 3
	(Test point)	$V_{OUT}=0.71$		206	mA	3
I_{CL}	Low clamp current	$-5<V_{IN}\leq -1$	$-25+(V_{IN}+1)/0.015$		mA	
t_R	Unloaded output rise time	0.4V to 2.4V	1	5	V/ns	4
t_F	Unloaded output fall time	2.4V to 0.4V	1	5	V/ns	4

Notes:
1. Refer to the V/I curves in Section 4.2.1 of the PCI Specification. This specification does not apply to P_PCLK, S_CLK, $\overline{\text{P\_PRST}}$ and $\overline{\text{S\_PRST}}$ which are system outputs. "Switching Current High" specifications are not relevant to open drain outputs such as $\overline{\text{P\_SERR}}$, $\overline{\text{S\_SERR}}$, $\overline{\text{P\_INT[A:D]}}$ and $\overline{\text{S\_INT[A:D]}}$.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as it does in the pull-down curve). This difference is intended to allow for an optional N-channel pullup.
3. Maximum current requirements are met as drivers pull beyond the first step voltage (AC drive point). Equations defining these maximums (A and B) are provided with the respective V/I curves given in the PCI Spec. The equation defined maxima is met by design.
4. The minimum slew rate (slowest signal edge) is met by the PCI drivers. The maximum slew rate (fastest signal edge) is a guideline. Motherboard designers must bear in mind that rise and fall times faster than this maximum guideline could occur, and should ensure that signal integrity modeling accounts for this.

Equation A: $I_{OH} = 11.9 \cdot (V_{OUT} - 5.25V) \cdot (V_{OUT} + 2.45V)$ for $V_{CC} > V_{OUT} > 3.1V$

Equation B: $I_{OL} = 78.5 \cdot V_{OUT}(4.4V - V_{OUT})$ for $0V < V_{OUT} < 0.71V$

4.2 Local Bus Timings

Table 11: i960 Local Bus AC Test Conditions

Symbol	Parameter	Limits	Units
V_{CC}	Supply voltage	4.75 to 5.25	V
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 12: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Derating
4mA	0.058 ns/pF for loads > 50pF

Figure 5: Clock and Synchronous Signals

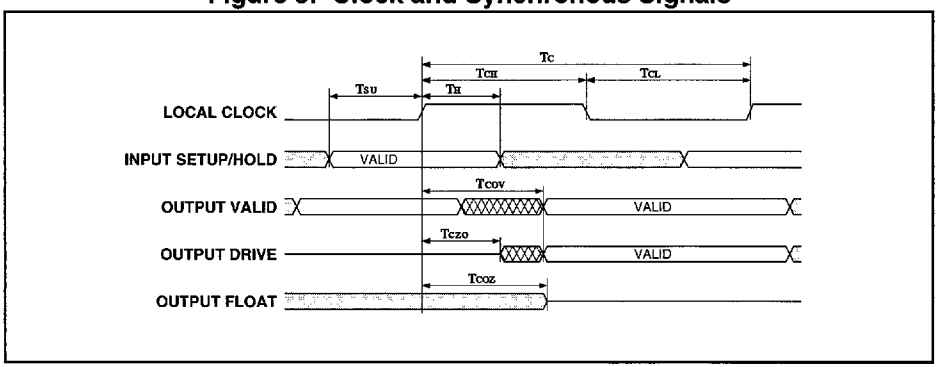


Figure 6: ALE Signal

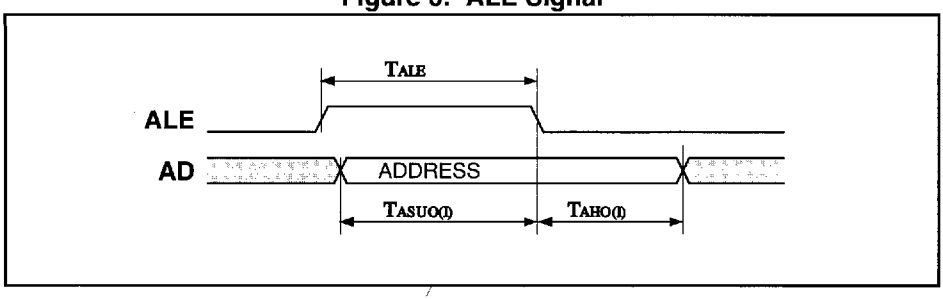


Table 13: Local Bus Timing Parameters for Vcc = 5 Volts +/- 5%

				33MHz		40MHz		
#	Symbol	Description	Notes	Min	Max	Min	Max	Units
1	T_C	LCLK period		30		25		ns
2	T_{CH}	LCLK high time	1	12		11		ns
3	T_{CL}	LCLK low time	1	12		11		ns
4	T_{SU}	Synchronous input setup	2	11		10		ns
4a	T_{SU}	Synchronous input setup ($\overline{BLAST}$)		13		11		ns
5	T_H	Synchronous input hold			3		3	ns
6	T_{COV}	LCLK to output valid delay	3	3	14	3	13	ns
7a	T_{COV}	LCLK to output valid delay (address, data, byte enable, parity)		4	19	4	17	ns
8	T_{CZO}	LCLK to output driving delay		5	18	4	16	ns
9	T_{COZ}	LCLK to high impedance delay	4	5	18		16	ns
10	T_{RST}	Reset period when $\overline{P\_LRST}$ or $\overline{S_LRST}$used as input		$16 \cdot T_C$		$16 \cdot T_C$		ns

Notes:
1. Measured at 1.5V.
2. All local bus signals except those in 4a.
3. All local bus signals except those in 7a.
4. $\overline{READY}$, $\overline{BLAST}$, $\overline{ADS}$ are driven to high impedance at the falling edge of LCLK.

Table 14: PCI Bus Timing Parameters for Vcc = 5 Volts +/- 5%

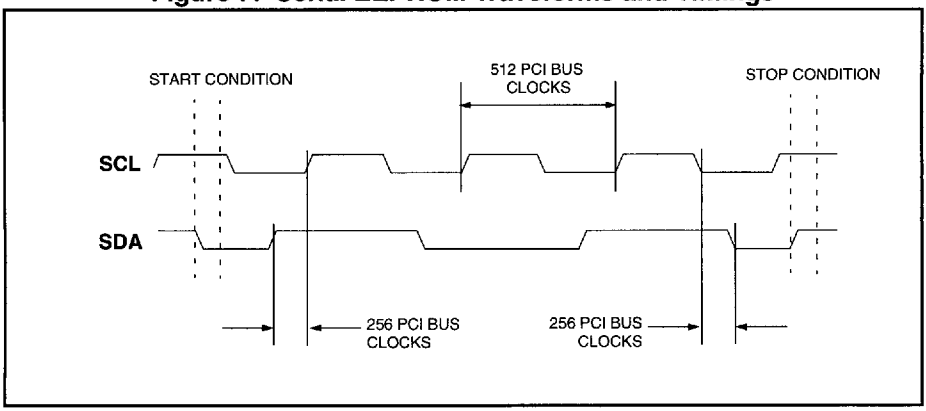
#	Symbol	Description	Notes	Min	Max	Units
1	T_C	P_PCLK or S_PCLK period		30		ns
2	T_{SU}	Synchronous input setup to P_PCLK or S_PCLK	1	7		ns
2a	T_{SU}	Synchronous input setup to P_PCLK ($\overline{P\_GNT}$) or S_PCLK ($\overline{S\_GNT}$)		10		ns
3	T_H	Synchronous input hold from P_PCLK or S_PCLK		0		ns
4	T_{COV}	P_PCLK or S_PCLK to output valid delay	2	3	11	ns
4a	T_{COV}	P_PCLK or S_PCLK to output valid delay ($\overline{P\_REQ}$ or $\overline{S\_REQ}$)		4	12	ns
5	T_{CZO}	P_PCLK or S_PCLK to output driving delay		4	11	ns
6	T_{COZ}	P_PCLK or S_PCLK to high impedance delay		5	18	ns
7	T_{RST}	Reset period when $\overline{P\_PRST}$ or $\overline{S_PRST}$used as input		$16 \cdot T_C$		

Notes:
1. All PCI bus signals except those in 2a.
2. All PCI bus signals except those in 4a.

4.3 Serial EEPROM Port TImings

The clock for the serial EEPROM interface is derived by dividing the PCI bus clock. The waveforms generated are shown in Figure 7.

Figure 7: Serial EEPROM Waveforms and Timings



5.0 Revision History

Table 15: Revision History

Revision Number	Date	Comments and Changes
2.1	10/96	Data Book revision.
2.0	08/96	First release without NDA.
1.0	05/96	Alpha release.

SEMICONDUCTOR
THE EMBEDDED CHIPSET COMPANY

USA:
2348G Walsh Ave.
Santa Clara CA 95051
Phone: (408)988-1050 Fax: (408)988-2601
Toll Free: (800)488-8410 (Canada and U.S. only)
World Wide Web: http://www.vcubed.com

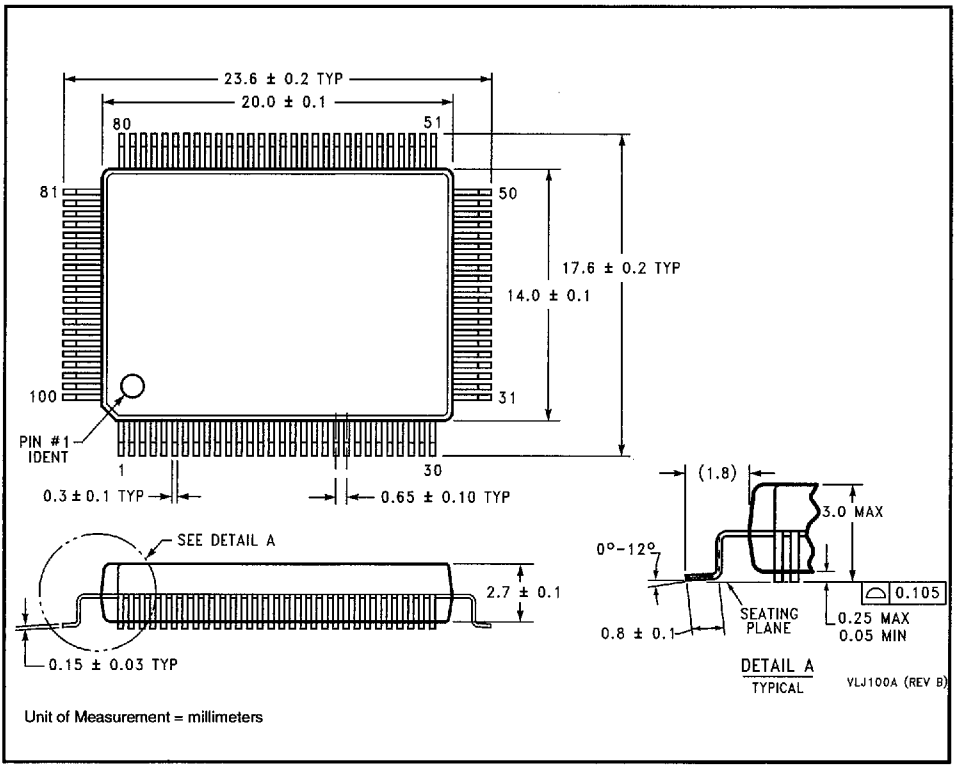
Package Specifications

Package outlines are listed in ascending pin count order. For information on device ordering codes, see *Ordering Information* in this data book. Package outline dimensions are shown in each diagram.

Package Selection Guide

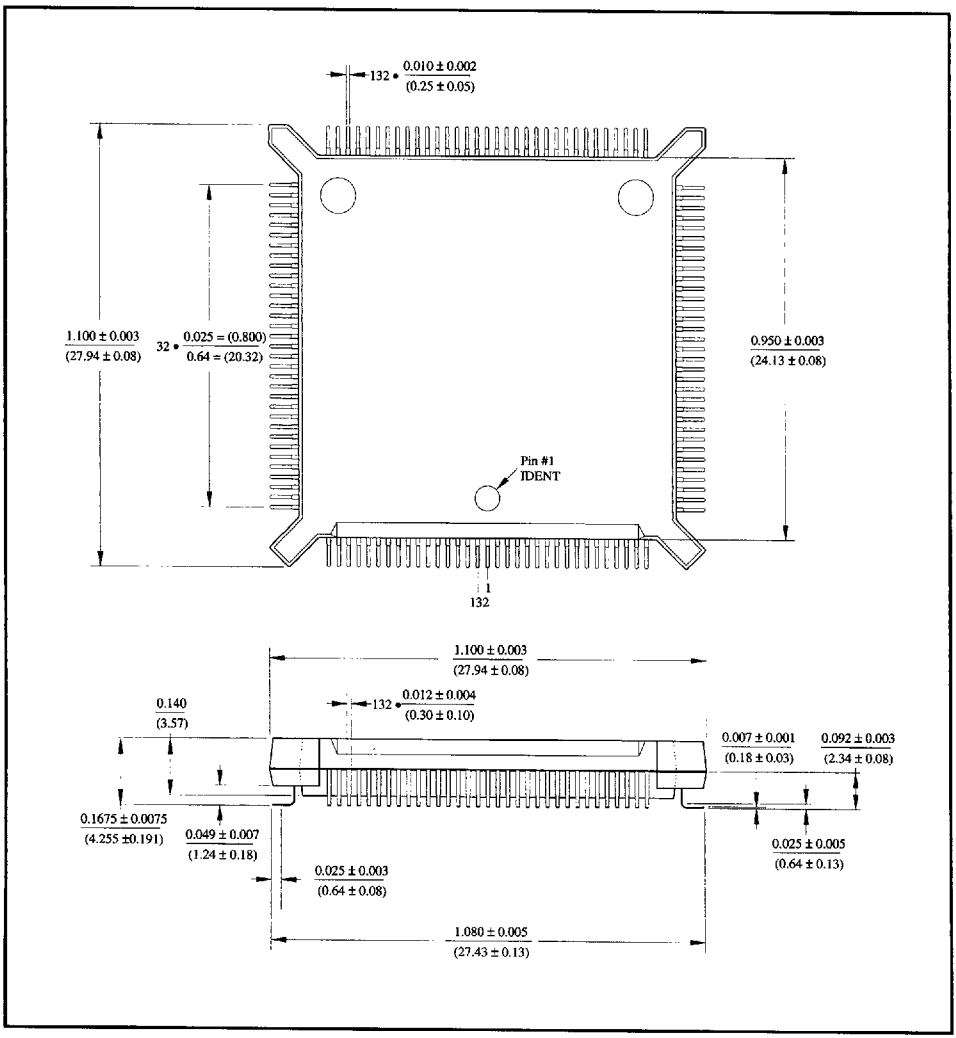
DEVICE	PQFP	BGA
V960PBC V961PBC V962PBC V292PBC	160	
V96DPC		313
V96BMC V292BMC	132	
V96SSC	100	

100-pin EIAJ PQFP (Plastic Quad Flat Pack) Mechanical Details



Products: V96SSC

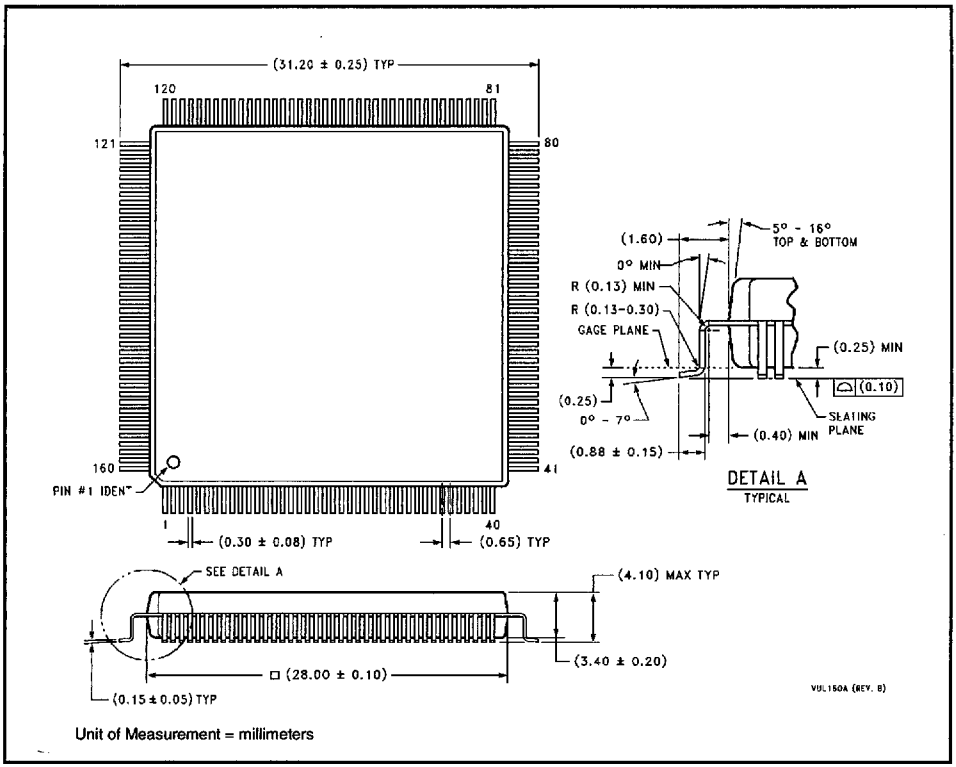
132-pin PQFP (Plastic Quad Flat Pack) Mechanical Details



Products: V96BMC, V292BMC

Note: Controlling measurement is in inches. Millimeter measurement, shown in parentheses, are for reference only.

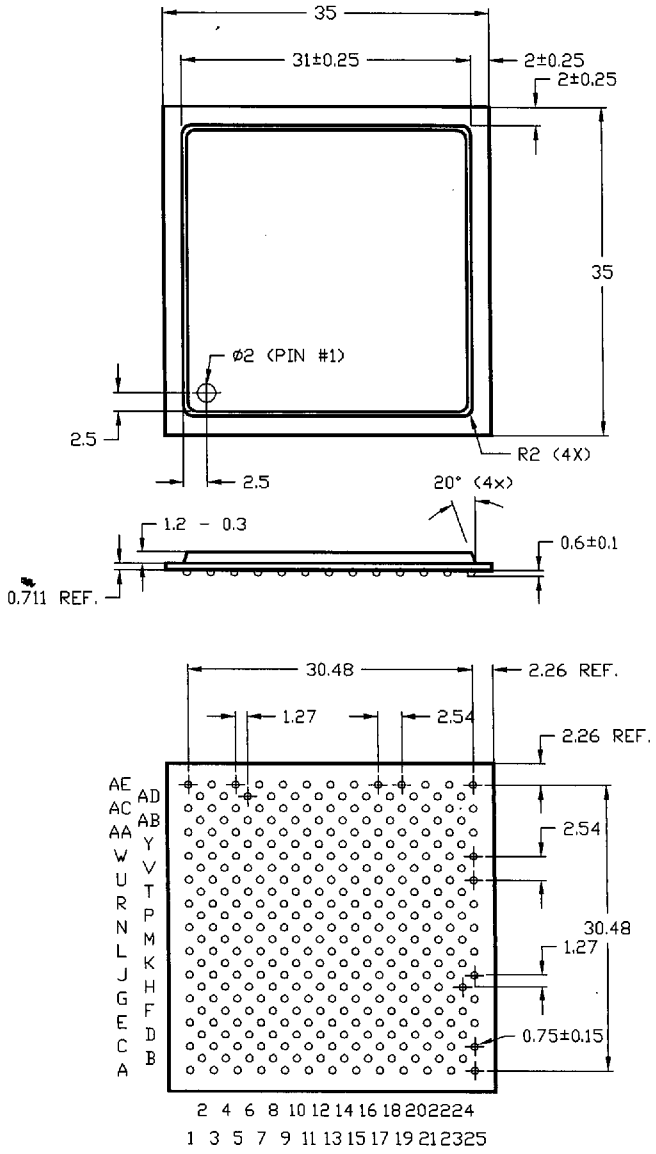
160-pin EIAJ PQFP (Plastic Quad Flat Pack) Mechanical Details



Products: V960PBC, V961PBC, V962PBC, V292PBC

313-pin BGA (Ball Grid Array) Mechanical Details

Dimensions are in millimeters.



Products: V96DPC