T-79-07-10

VTC Incorporated

# VA708

## HIGH-SPEED, FAST-SETTLING, HIGH OUTPUT CURRENT OPERATIONAL AMPLIFIER, $A_{CL} \geq 3$

### FEATURES

- Fast Settling Time: ±0.1% in 150ns
- High Slew Rate: 90V/µs
- Large Gain Bandwidth: 100MHz
- Full Power Bandwidth: 4.8 MHz at 6V p-p
- Ease of Use: Internally Compensated for $A_{CL} \geq 3$ with 50°-60° Phase Margin
- Large Output Current: ±50mA
- Low Supply Voltage Operation: ±4V
- Wide Input Voltage Range: Within 1.5V of V+ and 0.5V of V-
- Short Circuit Protection
- Available in Commercial Versions

### DESCRIPTION

The VA708 is a high-speed general purpose monolithic operational amplifier useful for signal frequencies extending into the video range. The same processing innovations which permit the high speed also allow very high output currents capable of driving large capacitive loads at high speeds.

The high open-loop voltage gain of 10k V/V and high slew rate of 90V/µs make the VA708 ideal for analog amplification and processing of high-speed signals.

The large gain bandwidth of 100MHz and 90V/µs slew rate results in ±0.1% settling times of150ns, which makes the amplifier ideal for fast data conversion systems.

The high output current capability of ±50mA allows the amplifier to drive terminated transmission lines of 50Ω with amplitudes of 5V peak-to-peak.

Along with the high speed and output drive capability, a 35nA offset current and trimmable offset voltage make the VA708 usable for signal conditioning applications where accuracy must be maintained.

### ABSOLUTE MAXIMUM RATINGS

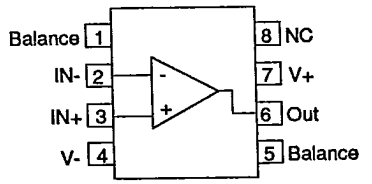
| | |
|---|---|
| Supply Voltages | ±6V |
| Differential Input Voltage | ±9V |
| Common Mode Input Voltage | $\|V_S\|$ -0.5V |
| Power Dissipation (Note 1) | 450mW |
| Output Short Circuit Current Duration (Note 2) | Indefinite |
| Operating Temperature Range: | |
| Commercial (708 J, K) | 0° to 70°C |
| Storage Temperature Range | -65° to +150°C |
| Lead Temperature (Soldering to 60 Sec.) | 300°C |

*Note 1: Power derating above $T_A$ = 70°C to be based on a maximum junction temperature of 150°C and the following thermal resistance factors in the chart below.*

*Note 2: Continuous short circuit protection is allowed to the following case and ambient temperatures:*

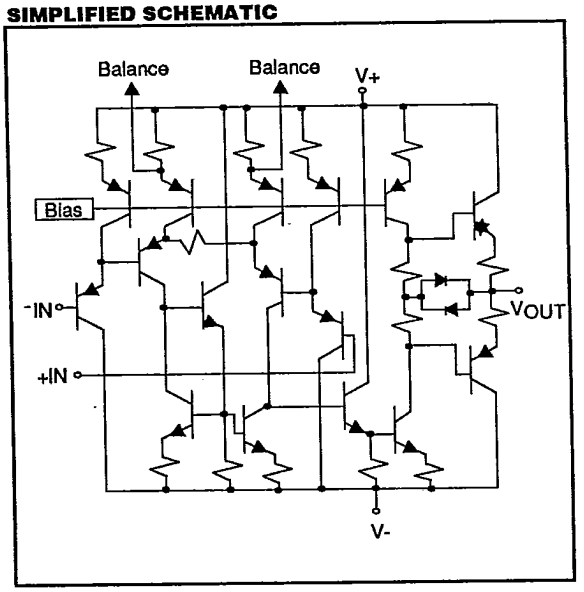
### CONNECTION DIAGRAM

8-Lead Dual In-Line/SOIC Package




*Top View*

### SIMPLIFIED SCHEMATIC




### PACKAGE TYPES AVAILABLE

- 8-Pin Plastic DIP
- 8-Pin CERDIP
- 8-Pin SOIC

| PKGE. | $\theta_{JC}$ (°C/W) | $\theta_{JA}$ (°C/W) | $T_C$ (°C) | $T_A$ (°C) |
|---|---|---|---|---|
| DIP | 75 | 180 | 110 | 70 |
| SOIC | 115 | 180 | 95 | 70 |

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**ELECTRICAL CHARACTERISTICS** ($V_S$= ±5V, $T_A$ = 25° C unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | VA708J | | | VA708K | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Input Offset Voltage | $V_{OS}$ | | | 5 | 12 | | 3 | 6 | mV |
| $T_{Min}$ to $T_{Max}$ | | 0°≤$T_A$≤70°C | | 8 | 16 | | 5 | 10 | |
| Average Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | 0°≤$T_A$≤70°C | | 20 | | | 20 | | µV/°C |
| Input Bias Current | $I_B$ | | | 650 | 1100 | | 650 | 1100 | nA |
| Input Offset Current | $I_{OS}$ | | | 35 | 120 | | 35 | 120 | nA |
| $T_{Min}$ to $T_{Max}$ | | 0°≤$T_A$≤70°C | | 70 | 200 | | 70 | 200 | |
| Input Common Mode Range | $V_{CM}$ | | +3<br>-4 | +3.5<br>-4.5 | | +3<br>-4 | +3.5<br>-4.5 | | V |
| Differential Input Resistance | $R_{IND}$ | (Note 1) | 3 | 10 | | 3 | 10 | | MΩ |
| Common Mode Input Resistance | $R_{INC}$ | (Note 1) | 4 | 8 | | 4 | 8 | | MΩ |
| Differential Input Capacitance | $C_{IND}$ | (Note 1) | | 2 | | | | | pF |
| Common Mode Input Capacitance | $C_{INC}$ | (Note 1) | | 3 | | | 3 | | pF |
| Input Voltage Noise | $e_N$ | BW=10Hz to 100KHz | | 12 | | | 12 | | µVRMS |
| Open Loop Voltage Gain | $A_V$ | $V_{OUT}$ =±3V<br>$R_L$=2kΩ | 2 | 5 | | 5 | 10 | | V/mV |
| Output Voltage Swing | $V_{OUT}$ | $R_L$=2kΩ | ±3.5 | | | ±3.5 | | | V |
| | | $R_L$=51Ω | ±2.0 | ±2.4 | | ±2.5 | ±2.7 | | |
| Power Supply Current | $I_S$ | | | 7 | 10 | | 7 | 10 | mA |
| Common Mode Rejection Ratio | CMRR | $V_{CM}$ =±2V | 60 | 70 | | 60 | 70 | | dB |
| Power Supply Rejection Ratio | PSRR | $\Delta V_{PS}$ =±0.5V | 60 | 66 | | 60 | 66 | | dB |
| Slew Rate | SR | 10-90%of Leading Edge (Figure 1) | 60 | 90 | | 60 | 90 | | V/µs |
| Settling Time | $t_S$ | To ±0.1%(±4mV) of Final Value (Figure 1) (Note 1) | | 150 | 200 | | 150 | 200 | ns |
| Gain Bandwidth Product | GBW | | | 100 | | | 100 | | MHz |
| Small Signal Rise/Fall Time | $t_r$ /$t_f$ | $e_O$ = ±50mV 10-90% (Figure 1) | | 7 | | | 7 | | ns |
| Full Power Bandwidth | $BW_{FP}$ | $R_L$= 2kΩ<br>$C_L$= 50pF<br>$V_{OUT}$= 6Vp-p | | 4.8 | | | 4.8 | | MHz |

*Notes: 1. Not tested, guaranteed by design.*

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## DIE INFORMATION

### WAFER TEST LIMITS

$V_S$= ±5V, $T_A$= 25° C unless otherwise stated

| PARAMETER | SYM | CONDITIONS | VA708XS LIMIT | UNITS |
|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | 6 | mV Max |
| Input Bias Current | $I_B$ | | 1100 | nA Max |
| Input Offset Current | $I_{OS}$ | | 120 | nA Max |
| Input Common Mode Range | $V_{CM}$ | | +3<br>-4 | V Min |
| Open Loop Voltage Gain | $A_V$ | $V_{OUT}$=±3V<br>$R_L$ = 2k | 5 | V/mV Min |
| Output Voltage Swing | $V_{OUT}$ | $R_L$ = 2KΩ | ±3.5 | V Min |
| | | $R_L$ = 51 Ω | ±2.5 | |
| Power Supply Current | $I_S$ | | 10 | mA Max |
| Common Mode Rejection Ratio | CMRR | $V_{CM}$ = ±2V | 60 | dB Min |
| Power Supply Rejection Ratio | PSRR | $\Delta V_{PS}$ = ±0.5V | 60 | dB Min |
| Slew Rate | SR | 10-90% of Leading Edge (Figure 1a,b) | 60 | V/µs Min |

### TYPICAL ELECTRICAL CHARACTERISTICS

$V_S$= ±5V, $T_A$= 25° C unless otherwise stated

| PARAMETER | SYM | CONDITIONS | VA708XS TYPICAL | UNITS |
|---|---|---|---|---|
| Input Offset Voltage $T_{Min}$ to $T_{Max}$ | $V_{OS}$ | | 6 | mV |
| Input Offset Current $T_{Min}$ to $T_{Max}$ | $I_{OS}$ | | 70 | nA |
| Settling Time | $t_S$ | To ±0.1% of Final Value (Figure 1a,b) | 150 | ns |
| Gain Bandwidth Product | GBW | | 100 | MHz |
| Small Signal Rise/Fall Time | $t_r$ /$t_f$ | $e_O$ = ±50mV 10-90% (Figure 1c) | 7 | ns |
| Full Power Bandwidth | $BW_{FP}$ | $R_L$ = 2kΩ<br>$C_L$ = 50pf<br>$V_{OUT}$= 6V p-p | 4.8 | MHz |

## DICE POLICY

**Electrical Characteristics**

Each die is electrically tested to the commercial or military grade DC parameters to guard band limits at 25°C to guarantee operation over the full temperature range.

**Quality Assurance**

All dice are 100% visually inspected to the requirement of MIL-STD-883C, Method 2010.2, Condition 3.

All dice are glass passivated with only the bonding pads exposed to provide scratch protection.

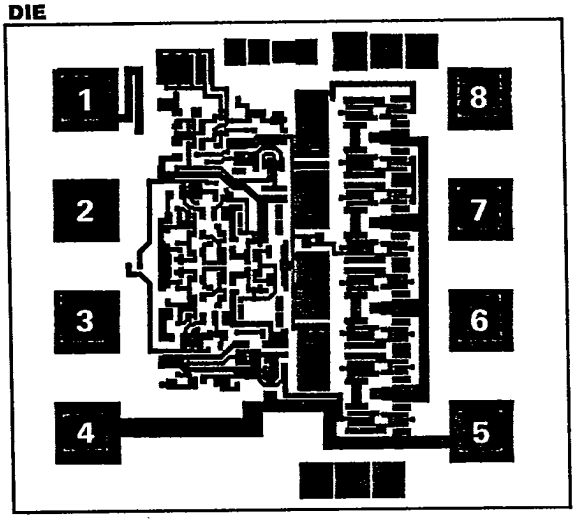
All dice are provided with gold backing.

**Shipping Packages/Order Information**

All dice are packaged in die crates with individual compartments which prevent damage to the die during shipping. The individual cavity size of the die crate is such that maximum rotation of the die within the cavity is < 45°.

Minimum order for dice is 100, supplied only in multiples of 100.

## DIE




Die size = 0.035 x 0.035 inch (1225 sq. mils)
0.89 x 0.89 mm (0.79 sq. mm)
Shipped in die crates.

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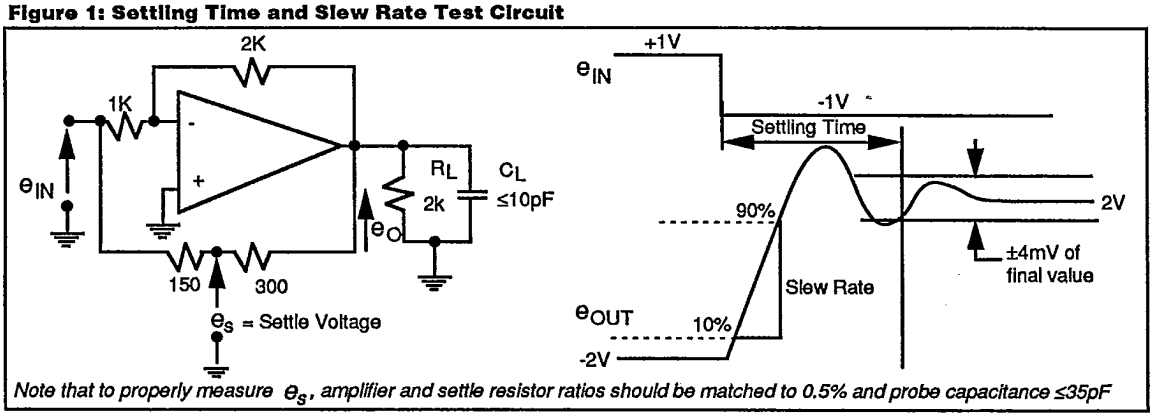
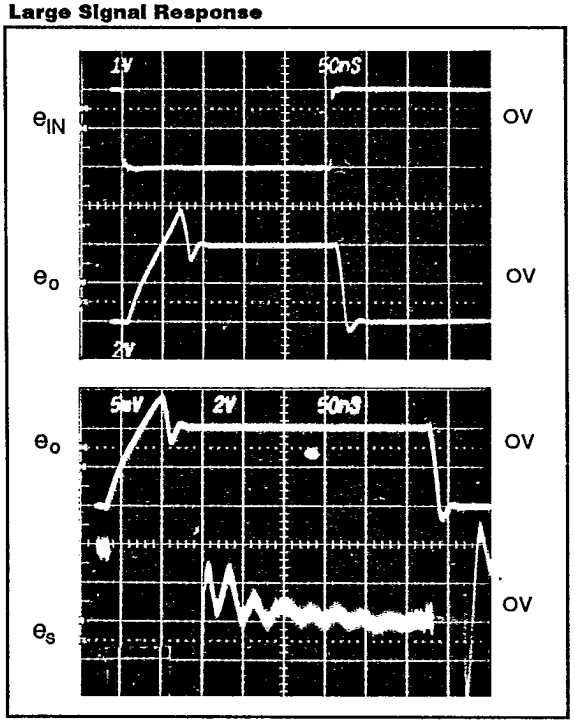
**Figure 1: Settling Time and Slew Rate Test Circuit**

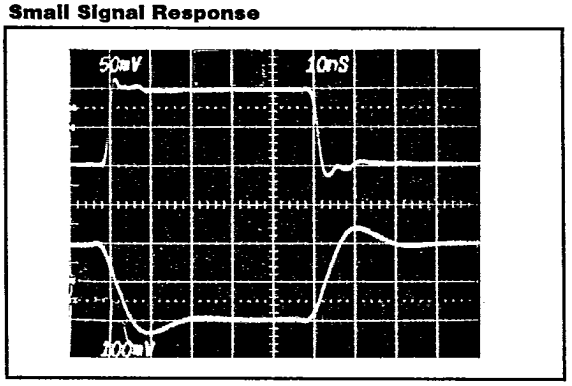



*Note that to properly measure $e_S$, amplifier and settle resistor ratios should be matched to 0.5% and probe capacitance ≤35pF*

**Large Signal Response**




**Small Signal Response**



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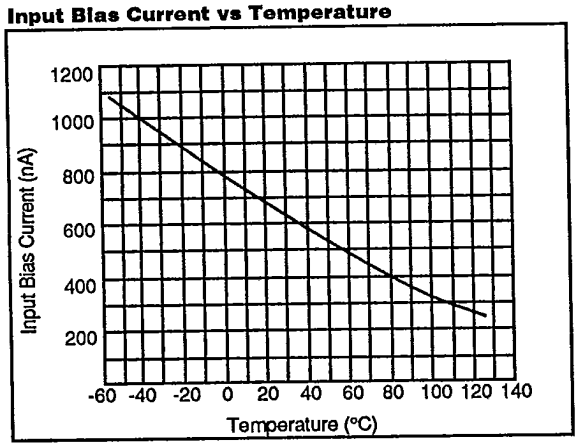
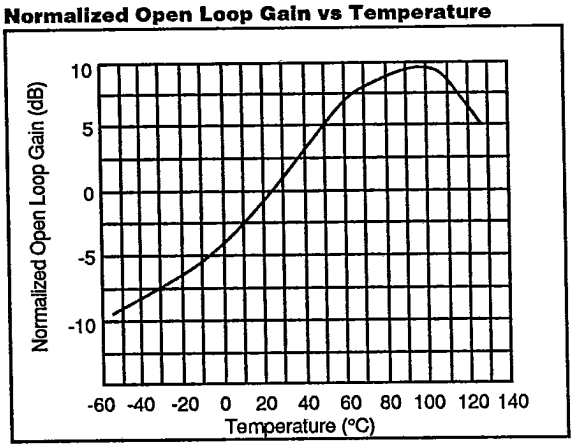
**TYPICAL PERFORMANCE CHARACTERISTICS** ($V_S$= ±5V, $T_A$= 25° C unless otherwise stated)

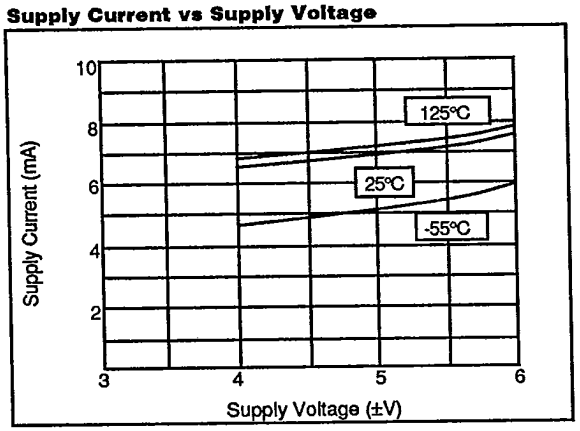
**Input Bias Current vs Temperature**



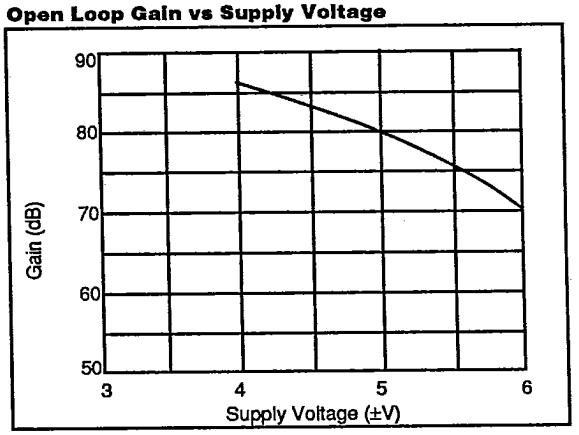

**Normalized Open Loop Gain vs Temperature**



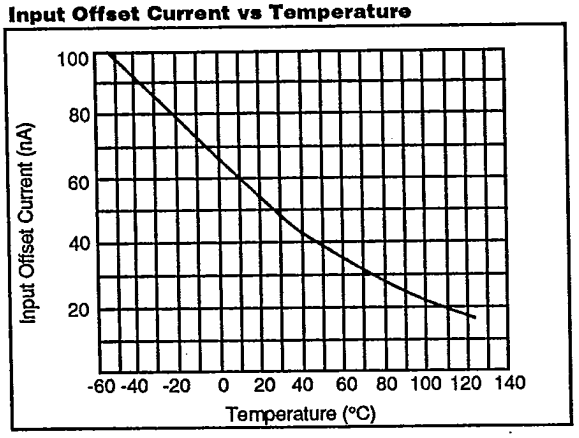

**Supply Current vs Supply Voltage**




**Open Loop Gain vs Supply Voltage**

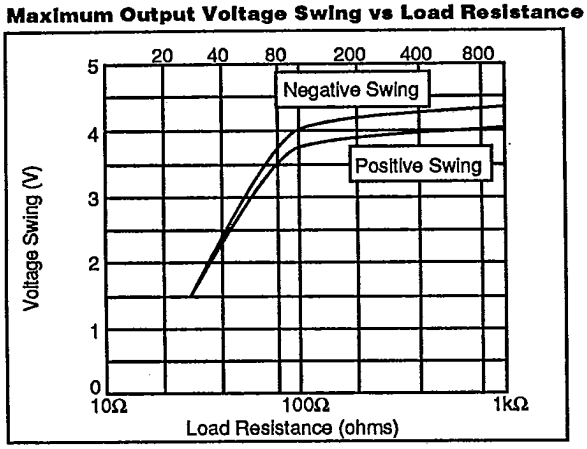



**Input Offset Current vs Temperature**

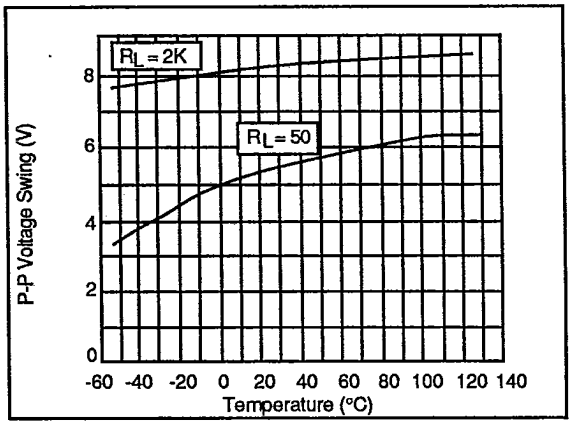


**TYPICAL PERFORMANCE CHARACTERISTICS** ($V_S$= ±5V, $T_A$ = 25° C unless otherwise stated)

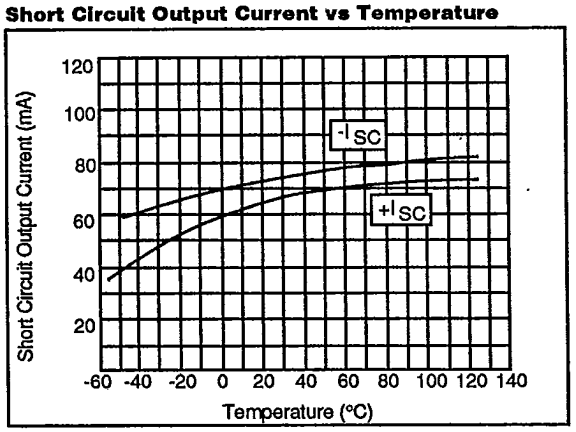
**Maximum Output Voltage Swing vs Load Resistance**



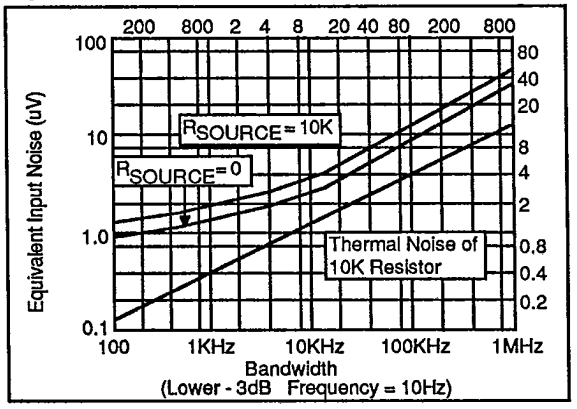

**Maximum Output Voltage Swing vs Temperature**




**Short Circuit Output Current vs Temperature**




**Equivalent Input Noise vs Bandwidth**



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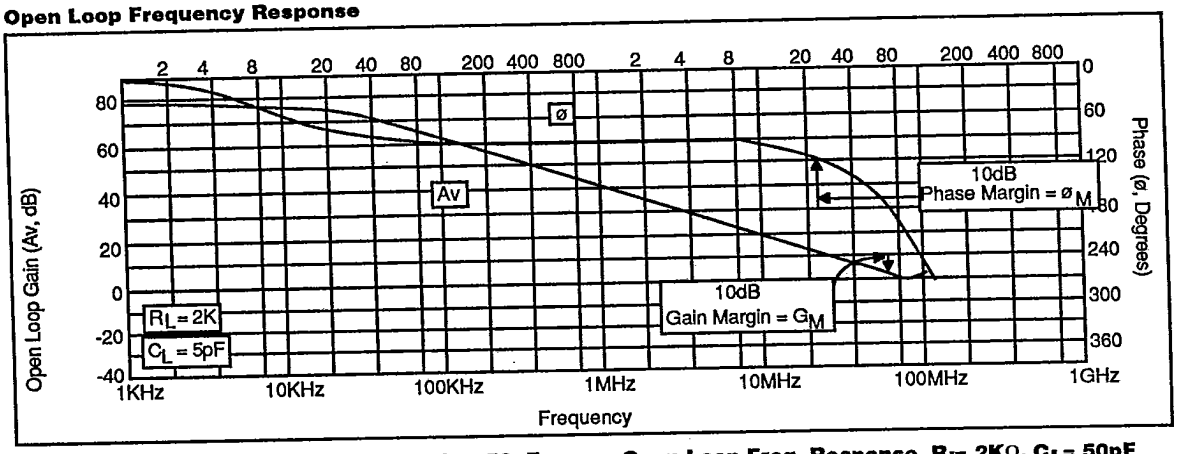
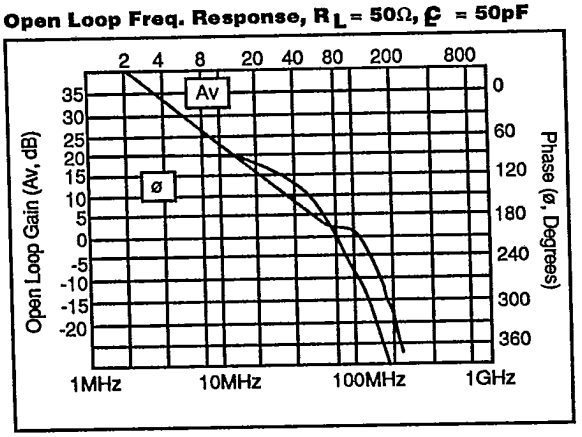
**TYPICAL PERFORMANCE CHARACTERISTICS** ($V_S$= ±5V, $T_A$= 25° C unless otherwise stated)

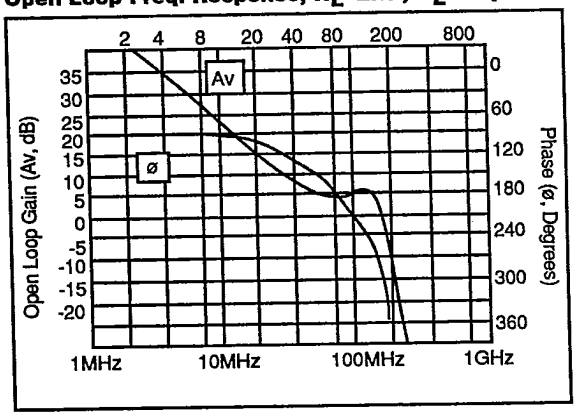
**Open Loop Frequency Response**



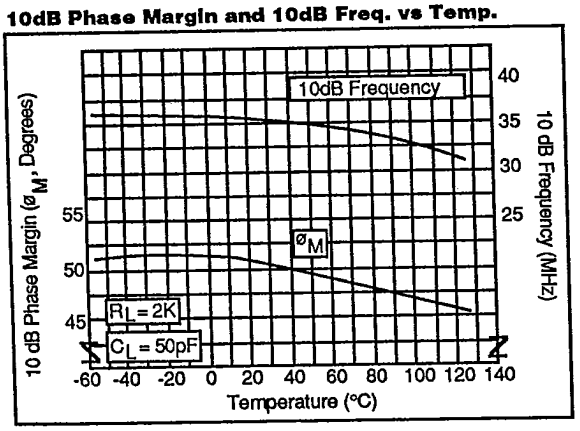

**Open Loop Freq. Response, $R_L$ = 50Ω, $C_L$ = 50pF**



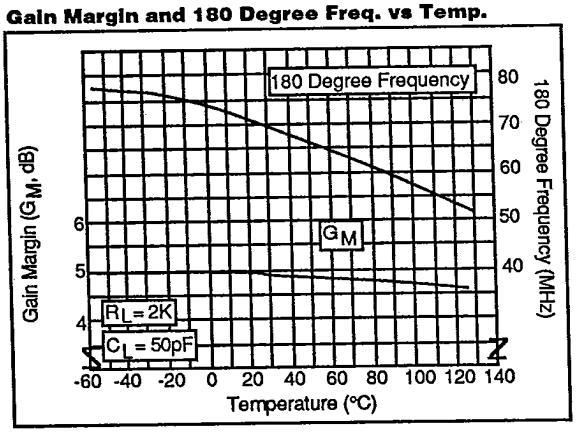

**Open Loop Freq. Response, $R_L$= 2KΩ, $C_L$= 50pF**




**10dB Phase Margin and 10dB Freq. vs Temp.**




**Gain Margin and 180 Degree Freq. vs Temp.**



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## APPLICATION INFORMATION

### AC Characteristics

The 35MHz 10dB crossover point of the VA708 is achieved without feed forward compensation, a technique which can produce long tails in the recovery characteristics. The single pole rolloff follows the classic 20dB/decade slope to frequencies approaching 50MHz. The 10dB (3.2 V/V) phase margin of 50°, even with a capacitive load of 50pF, gives stable and predictable performance down to non-inverting gain configurations of approximately 3 V/V (inverting gains of -2V/V). At frequencies beyond 50MHz, the 20dB/decade slope is disturbed by an output stage zero, the damping factor of which is dependent upon the $R_L$, $C_L$ load combination. This results in loss of gain margin (gain at loop phase = 360°) at frequencies of 70 to 100MHz which at a gain margin of 5dB ($R_L$ = 2K, $C_L$ = 50pF) results in a peak in the gain of 3 amplifier configurations as shown in Figures 3 and 4.

Figure 3 shows a blow up of the open loop characteristics in the 10MHz to 200MHz frequency range, as well as the corresponding closed loop characteristics for a gain of 3 non-inverting amplifier at similar load conditions. It should be noted that the open loop characteristic does not show the additional phase shift covered by the input capacitance pole — this is why the closed loop peaking at 30 to 40MHz is greater than what would be expected from the 50 to 60 degrees of phase margin indicated by the open loop characteristics. Corresponding small signal step response characteristics show well-behaved pulse waveforms with 16-33% overshoot.

The input capacitive pole can be neutralized by adding a feedback capacitor to $R_2$. The value of capacitance is selected according to $R_1 C_{IN} = R_2 C_{FB}$, where $C_{IN}$ is the sum of the common mode and differential input capacitance ≈ 5pF. For $R_2 = 2R_1$, $C_{FB} = C_{IN}/2 \approx 2.5$pF.

Figure 4 shows the results of this feedback capacitor addition. Neutralizing the input capacitance demonstrates the peaking that can result from the loss of gain margin at 70 to 100MHz. As the load time constant ($R_L C_L$) increases the peaking gets progressively worse ≈ 6dB at $R_L$ = 2K, $C_L$ = 50pF. The step response waveforms are as expected with a very strong 88MHz ring being exhibited at $R_L$ = 2K, $C_L$ = 50pF and no overshoot at $R_L$ = 50Ω, $C_L$ = 5pF.

### Layout Considerations

As with any high-speed wideband amplifier, certain layout considerations are necessary to ensure stable operation. All connections to the amplifier should be kept as short as possible, and the power supplies bypassed with 0.1µF capacitors to signal ground. It is suggested that a ground plane be considered as the best method for ensuring stability because it minimizes stray inductance and unwanted coupling in the ground signal paths.

To minimize capacitive effects, resistor values should be kept as small as possible, consistent with the application.

### Offset Voltage Nulling

The configuration of Figure 5 will give a typical $V_{OS}$ nulling range of ±15mV. If a smaller adjustment range is desired, resistor values R1 = R2 can be increased accordingly. For example, at R1 = 3.6kΩ, the adjustment range is ±5mV. Since pins 1 and 5 are not part of the signal path, AC characteristics are left undisturbed.

**Figure 5: Vos Nulling Method**

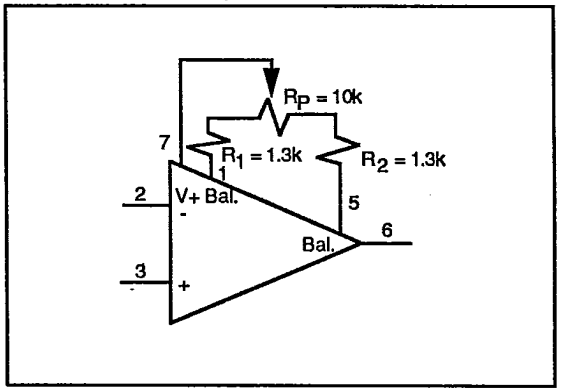

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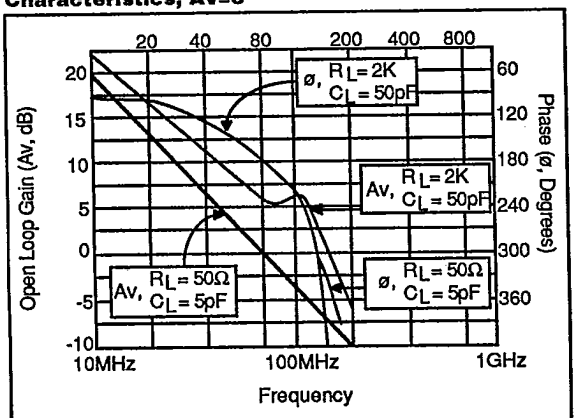
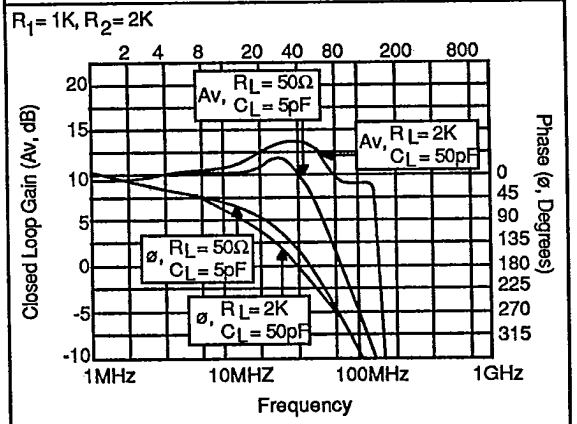
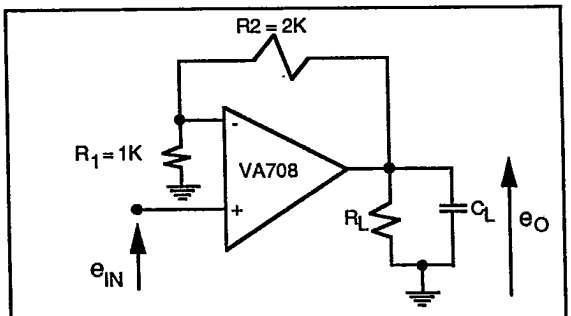
**Figure 3: Frequency and Time Domain Response Characteristics, Av=3**



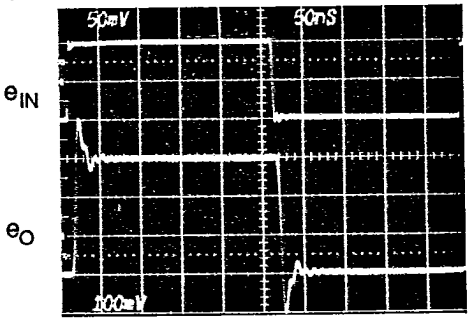

**Open Loop Frequency Response**



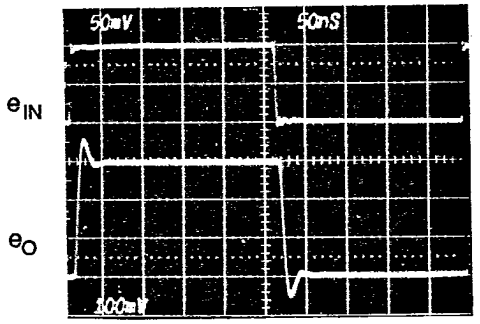

**Closed Loop Frequency Response**




$e_o / e_{IN} = (1 + R2/R1) = 3$ V/V



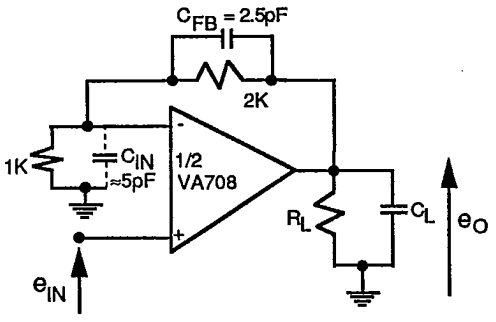

$R_L = 2k\Omega$
$C_L = 50pF$

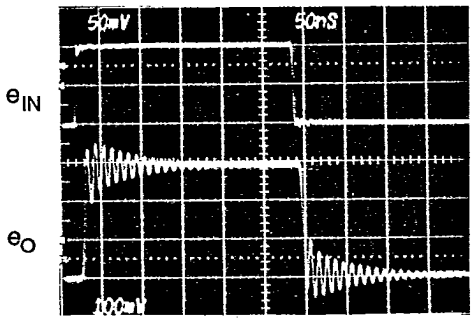



$R_L = 50\Omega$
$C_L = 5pF$

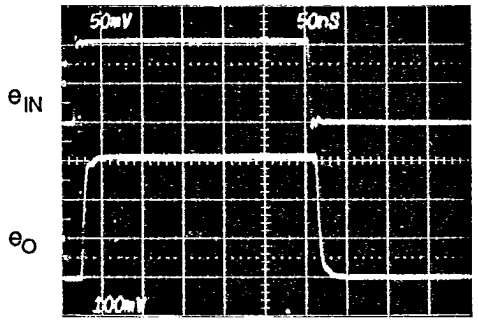
**Small Signal Step Response**

**Figure 4: Response Characteristics with Input Pole Cancellation, Av=3**



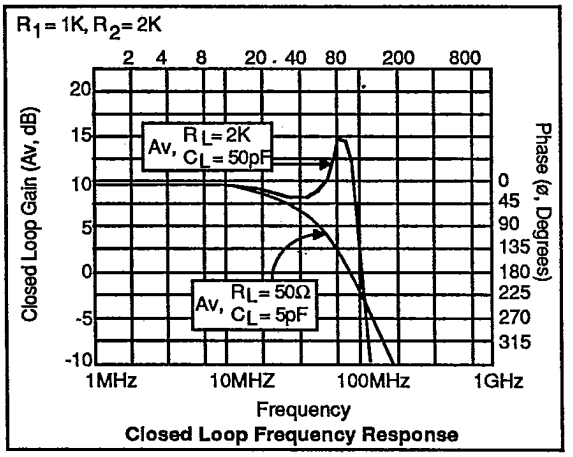




$R_L$ = 2kΩ
$C_L$ = 50pF




$R_L$ = 50Ω
$C_L$ = 5pF

**Small Signal Step Response**




**Closed Loop Frequency Response**