Central™
Semiconductor Corp.

PROCESS CP704

Small Signal Transistors

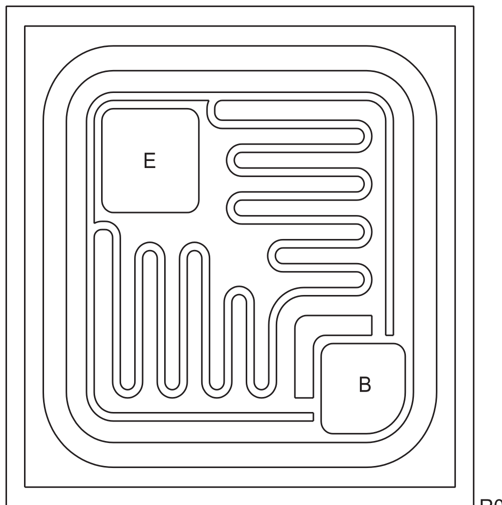
PNP - High Current Transistor Chip

www.DataSheet4U.com

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	22 x 22 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	3.7 X 3.7 MILS
Emitter Bonding Pad Area	4.2 X 4.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER
23,450

PRINCIPAL DEVICE TYPES
MPSA55
MPSA56

145 Adams Avenue
Hauppauge, NY 11788 USA
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Fax: (631) 435-1824
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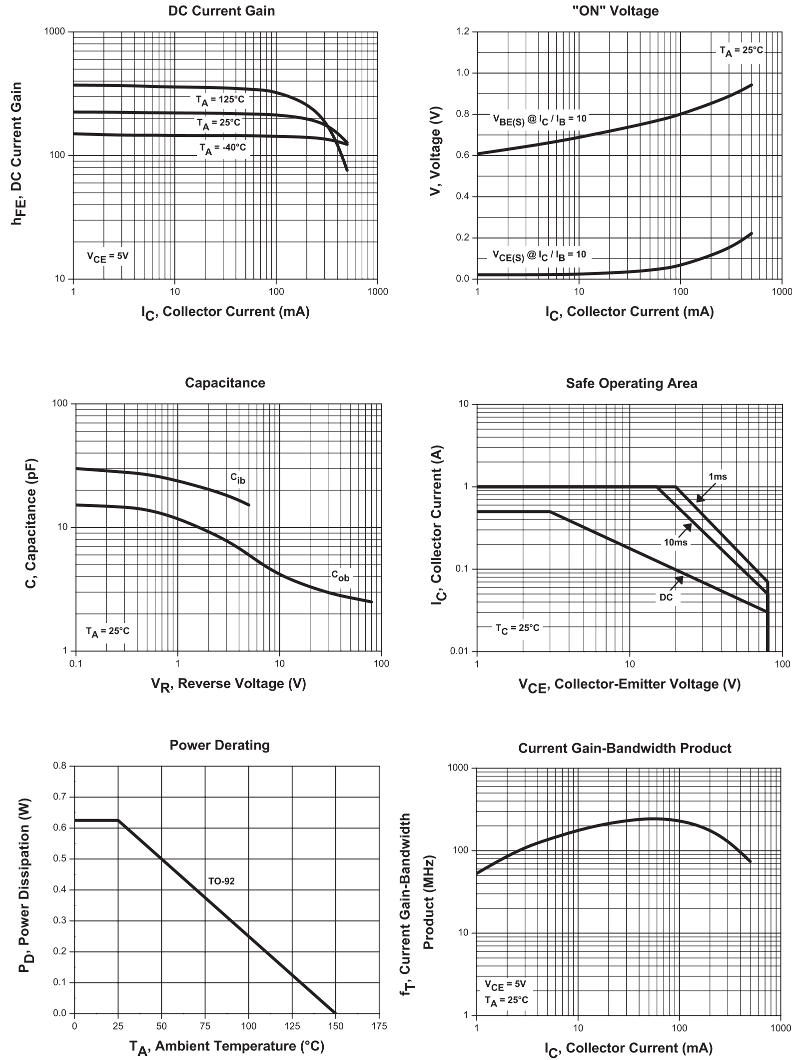
PROCESS CP704
Typical Electrical Characteristics



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