Addendum

HC908JL8AD/D
Rev. 0, 5/2002

Addendum to
MC68HC908JL8
Technical Data

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This addendum provides update and additional information to the *MC68HC908JL8 Technical Data*, Rev. 2 (Motorola document number MC68HC908JL8/D)

MC68HC08JL8
MC68HC08JK8

The MC68HC08JL8 is the ROM part equivalent to the MC68HC908JL8. The entire MC68HC908JL8 data book apply to this ROM device, with exceptions outlined in this addendum.

Table 1. Summary of MC68HC08JL8 and MC68HC908JL8 Differences

	MC68HC08JL8	MC68HC908JL8
Memory ($DC00–$FBFF)	8,192 bytes ROM	8,192 bytes FLASH
User vectors ($FFDC–$FFFF)	36 bytes ROM	36 bytes FLASH
Registers at $FE08 and $FFCF	Not used; locations are reserved.	FLASH related registers. $FE08 — FLCR $FFCF — FLBPR
Mask option register ($FFD0)	Defined by mask; read only.	Read/write FLASH register.
Monitor ROM ($FC00–$FDFF and $FE10–$FFCE)	$FC00–$FDFF: Not used. $FE10–$FFCE: Used for testing purposes only.	Used for testing and FLASH programming/erasing.
Available Packages	20-pin PDIP (MC68HC08JK8) 20-pin SOIC (MC68HC08JK8) 28-pin PDIP 28-pin SOIC 32-pin SDIP 32-pin LQFP	20-pin PDIP (MC68HC908JK8) 20-pin SOIC (MC68HC908JK8) 28-pin PDIP 28-pin SOIC 32-pin SDIP 32-pin LQFP

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MCU Block Diagram

Figure 1 shows the block diagram of the MC68HC08JL8.

Memory Map

The MC68HC08JL8 has 8,192 bytes of user ROM from $DC00 to $FBFF, and 36 bytes of user ROM vectors from $FFDC to $FFFF. On the MC68HC908JL8, these memory locations are FLASH memory.

Figure 2 shows the memory map of the MC68HC08JL8.

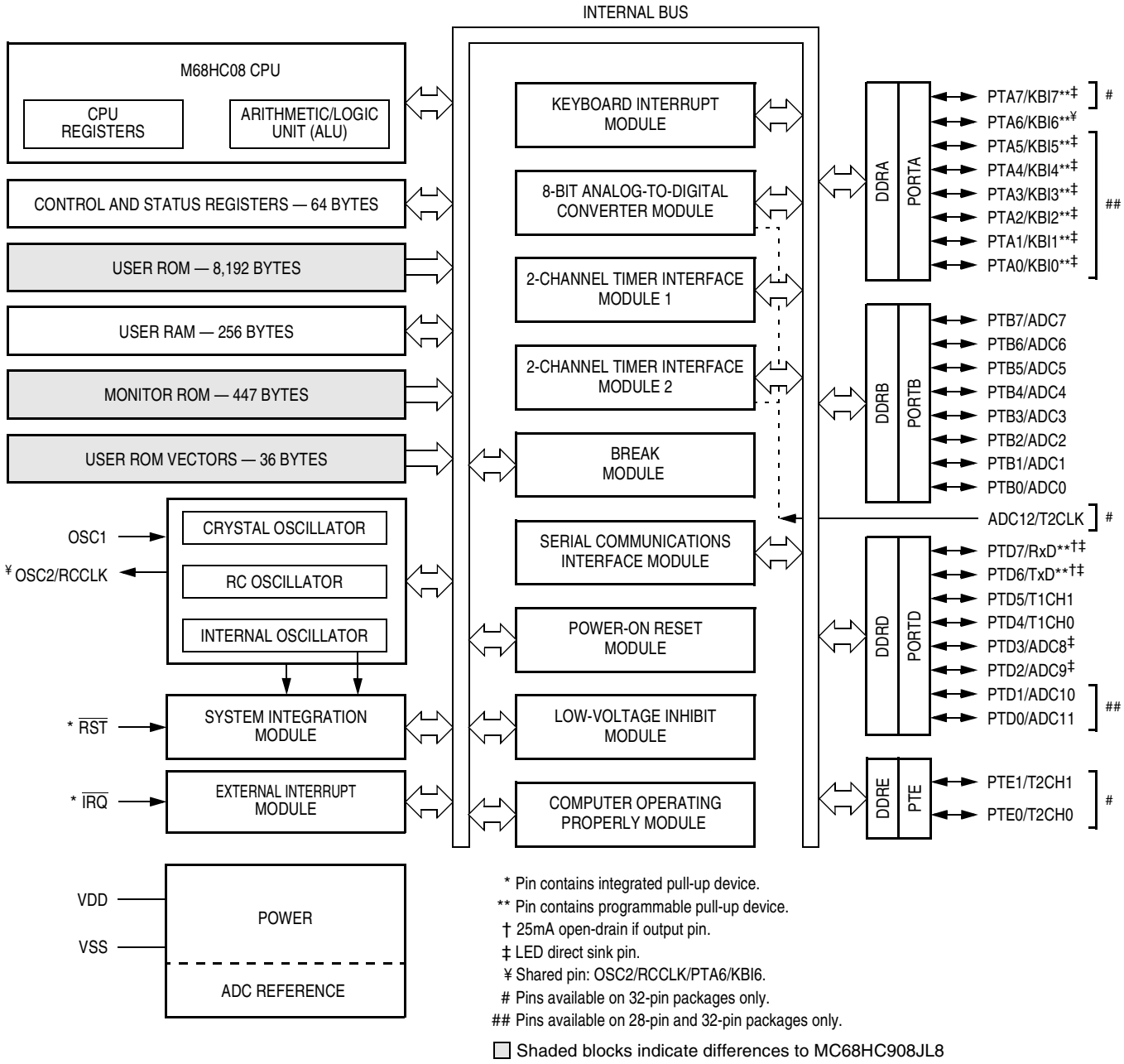

Figure 1. MC68HC08JL8 Block Diagram

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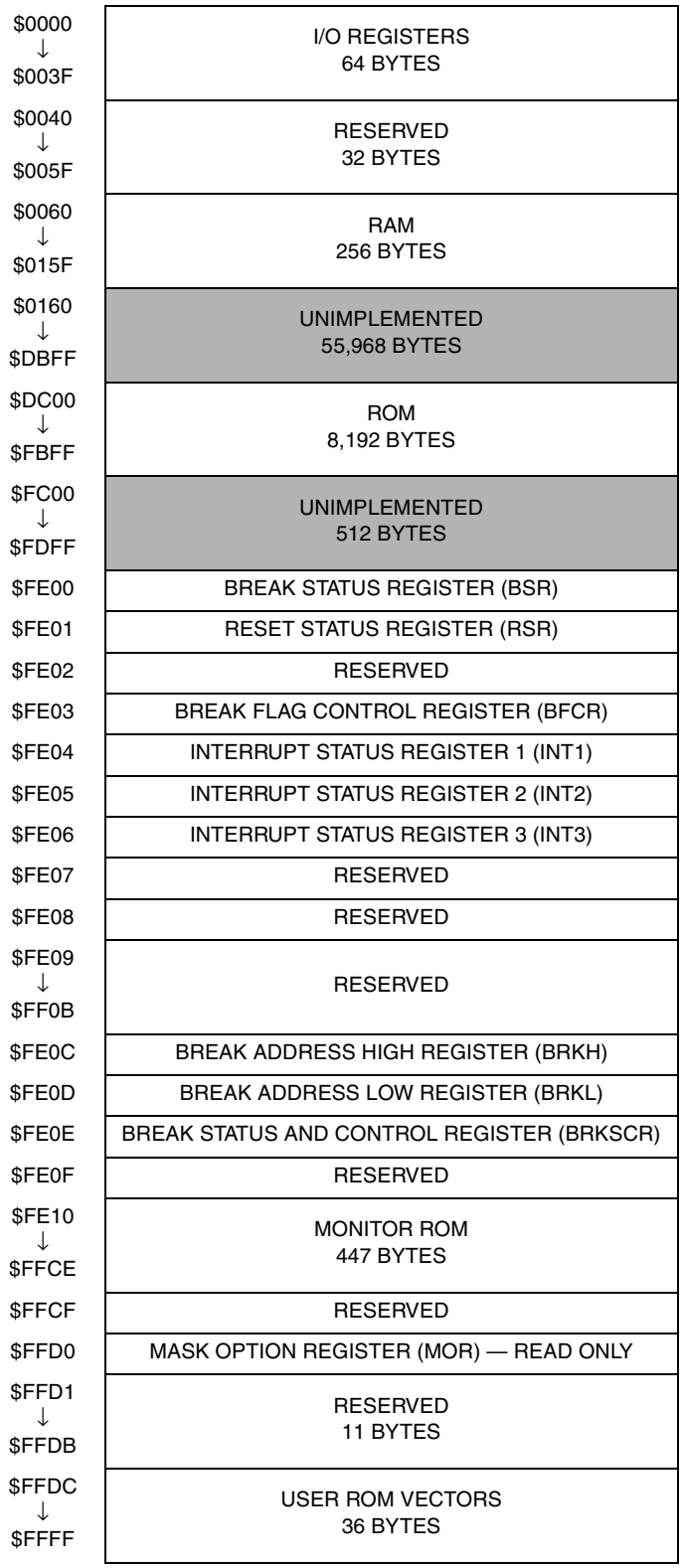

Figure 2. MC68HC08JL8 Memory Map

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Reserved Registers

The two registers at $FE08 and $FFCF are reserved locations on the MC68HC08JL8.

On the MC68HC908JL8, these two locations are the FLASH control register and the FLASH block protect register respectively.

Mask Option Register

The mask option register at $FFD0 is read only. The value is defined by mask option (hard-wired connections) specified at the time as the ROM code submission.

On the MC68HC908JL8, the MOR is implemented as a FLASH, which can be programmed, erased, and read.

Monitor ROM

The monitor program (monitor ROM: $FE10–$FFCE) on the MC68HC08JL8 is for device testing only. $FC00–$FDFF are unused.

Electrical Specifications

Electrical specifications for the MC68HC908JL8 apply to the MC68HC08JL8, except for the parameters indicated below.

DC Electrical Characteristics

Table 2. DC Electrical Characteristics (5V)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
V_{DD} supply current, f_{OP} = 8MHz RC oscillator option	I_{DD}	Values same as, and characterized from MC68HC908JL8, but not tested.			
Low-voltage inhibit, trip falling voltage	V_{TRIPF}	3.55 (3.60)[3]	4.02 (4.25)	4.48 (4.48)	V
Low-voltage inhibit, trip rising voltage	V_{TRIPR}	3.66 (3.75)	4.13 (4.40)	4.59 (4.63)	V

1. V_{DD} = 4.5 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. The numbers in parenthesis are MC68HC908JL8 values.

Table 3. DC Electrical Characteristics (3V)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
V_{DD} supply current, f_{OP} = 4MHz RC oscillator option	I_{DD}	Values same as, and characterized from MC68HC908JL8, but not tested.			
Low-voltage inhibit, trip voltage (No hysteresis implemented for 3V LVI)	V_{LVI3}	2.1 (2.18)[3]	2.4 (2.49)	2.69 (2.68)	V

1. V_{DD} = 2.7 to 3.3 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. The numbers in parenthesis are MC68HC908JL8 values.

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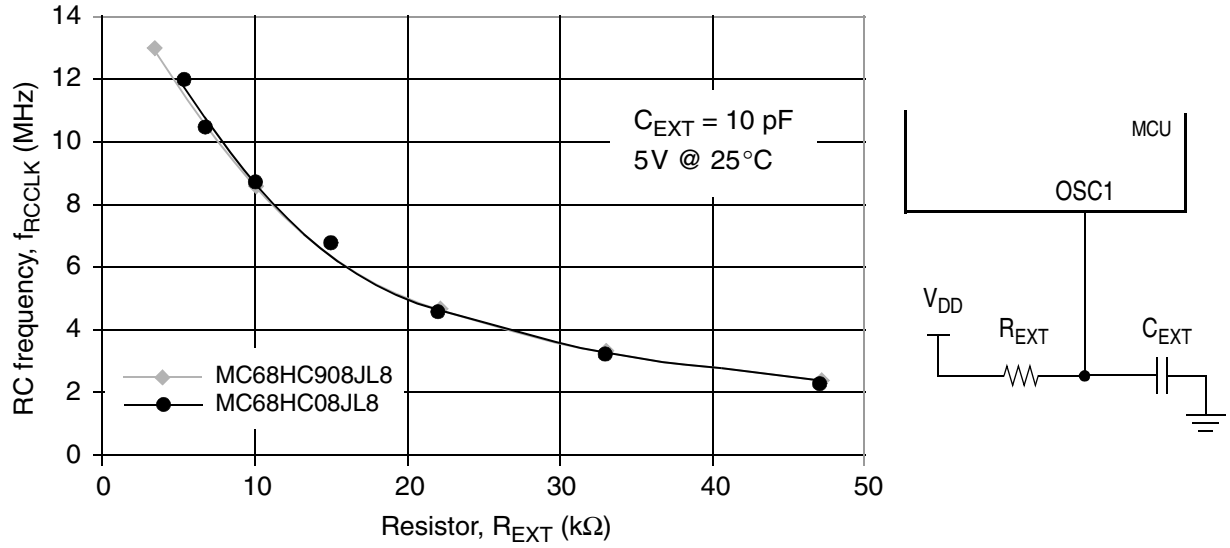

Figure 3. RC vs. Frequency (5V @25°C)

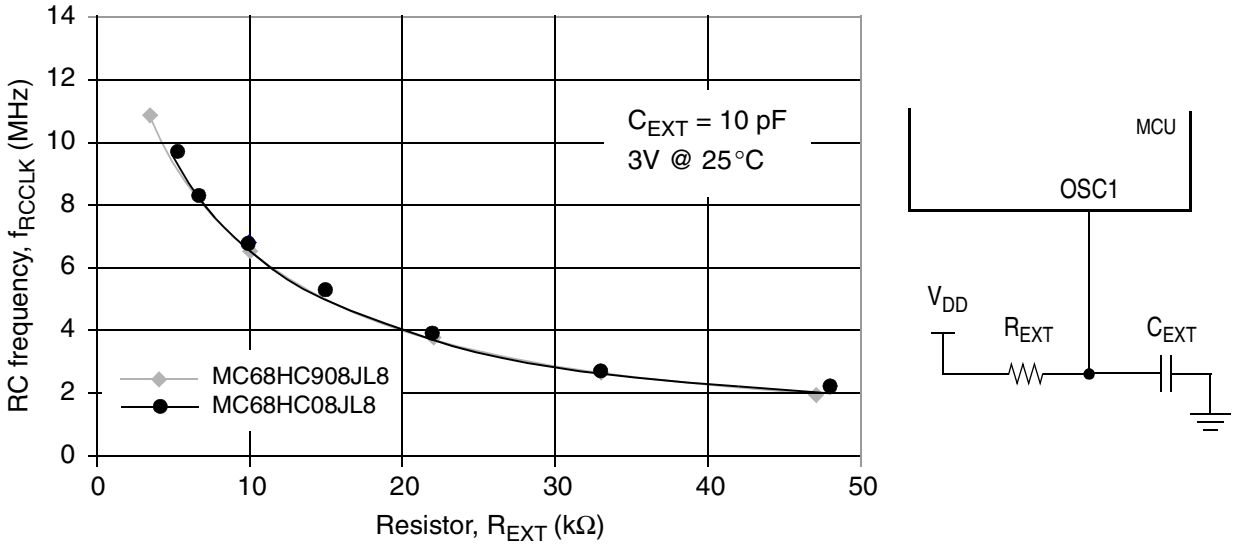

Figure 4. RC vs. Frequency (3V @25°C)

Memory Characteristics

Table 4. Memory Characteristics

Characteristic	Symbol	Min	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	V

Notes:
Since MC68HC08JL8 is a ROM device, FLASH memory electrical characteristics do not apply.

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MC68HC08JL8 Order Numbers

These part numbers are generic numbers only. To place an order, ROM code must be submitted to the ROM Processing Center (RPC).

Table 5. MC68HC08JL8 Order Numbers

MC Order Number	Operating Temperature Range	Package
MC68HC08JK8CP	−40 °C to +85 °C	20-pin PDIP
MC68HC08JK8MP	−40 °C to +125 °C	
MC68HC08JK8CDW	−40 °C to +85 °C	20-pin SOIC
MC68HC08JK8MDW	−40 °C to +125 °C	
MC68HC08JL8CP	−40 °C to +85 °C	28-pin PDIP
MC68HC08JL8MP	−40 °C to +125 °C	
MC68HC08JL8CDW	−40 °C to +85 °C	28-pin SOIC
MC68HC08JL8MDW	−40 °C to +125 °C	
MC68HC08JL8CSP	−40 °C to +85 °C	32-pin SDIP
MC68HC08JL8MSP	−40 °C to +125 °C	
MC68HC08JL8CFA	−40 °C to +85 °C	32-pin LQFP
MC68HC08JL8MFA	−40 °C to +125 °C	

NOTE: Temperature grade "M" is available for V_{DD} = 5V only.

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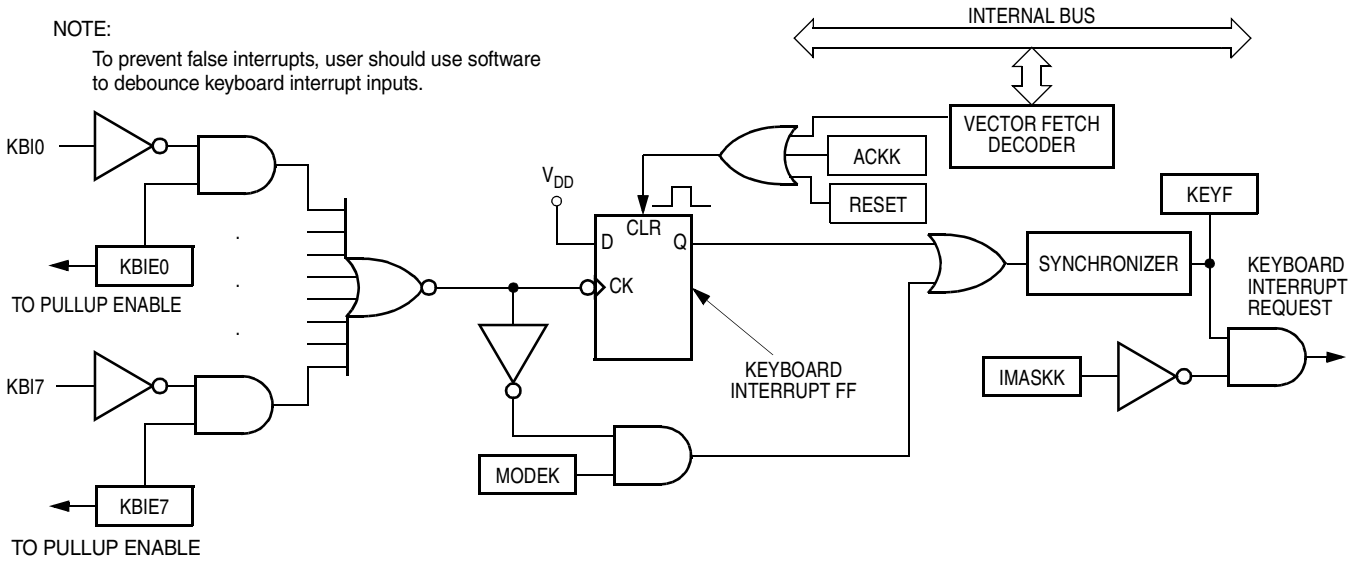
AMENDMENTS TO MC68HC908JL8/D, REV. 2

Keyboard Interrupt

Page 243, ***Figure 15-2. Keyboard Interrupt Block Diagram*** — Replace with the following block diagram:



Computer Operating Properly (COP)

Page 254, ***16.8.2 Stop Mode*** — Replace the two paragraphs:

From: Stop mode turns off the ICLK input to the COP if the STOP_ICLKDIS bit is set in configuration register 2 (CONFIG2). Service the COP immediately before entering or after exiting stop mode to ensure a full COP timeout period after entering or exiting stop mode.

After reset, the STOP_ICLKDIS bit is clear by default and ICLK is enabled during stop mode.

To: Stop mode turns off the ICLK input to the COP and clears the COP prescaler. Service the COP immediately before entering or after exiting stop mode to ensure a full COP timeout period after entering or exiting stop mode.

To prevent inadvertently turning off the COP with a STOP instruction, a configuration option is available that disables the STOP instruction. When the STOP bit in the configuration register has the STOP instruction is disabled, execution of a STOP instruction results in an illegal opcode reset.

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