Integrated Circuit Systems, Inc.

ICS9250-13

Frequency Generator & Integrated Buffers for PENTIUM/Pro™

General Description

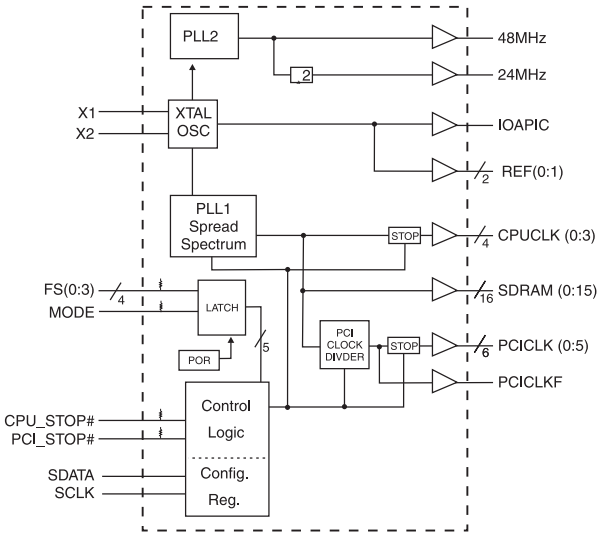
The **ICS9250-13** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro or Cyrix. Eight different reference frequency multiplying factors are externally selectable with smooth frequency transitions.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9250-13** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Features

- 3.3V outputs: SDRAM, PCI, REF, 48/24MHz
- 2.5V or 3.3V outputs: CPU
- 20 ohm CPU clock output impedance
- 20 ohm PCI clock output impedance
- Skew from CPU (earlier) to PCI clock - 1 to 4 ns, center 2.6 ns.
- No external load cap for C_L=18pF crystals
- ±250 ps CPU, PCI clock skew
- 400ps (cycle to cycle) CPU jitter
- Smooth frequency switch, with selections from 50 to 83.3 MHz CPU.
- I^2C interface for programming
- 2ms power up clock stable time
- Clock duty cycle 45-55%.
- 56 pin 300 mil SSOP package
- 3.3V operation, 5V tolerant input.

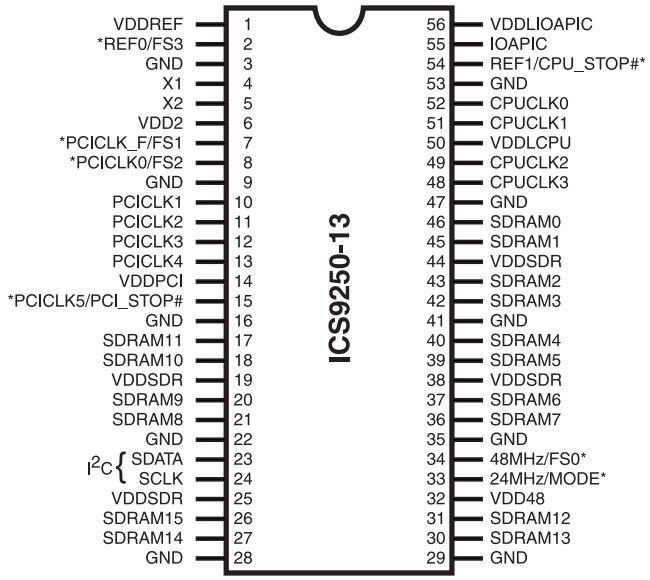
Block Diagram



Recomended Application:

- 440LX/EX type chipset Motherboard single chip clock solution.

Pin Configuration



56-Pin SSOP

* Internal Pull-up Resistor of 120K to VDD on indicated inputs

Power Groups

VDDREF = REF (0:1), X1, X2
VDDPCI = PCICLK_F, PCICLK(0:5)
VDDSDR = SDRAM (0:11), supply for PLL core,
VDD48 = 24MHz, 48MHz
VDDLIOAPIC = IOAPIC
VDDL2CPU = CPUCLK (0:3)

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I^2C is a trademark of Philips Corporation

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	Ref (0:1), XTAL power supply, nominal 3.3V
2	REF0	OUT	14.318 MHz reference clock.
	FS3[1, 2]	IN	Frequency select pin. Latched Input
3,9,16,22,28, 29, 35, 41, 47, 53	GND	PWR	Ground
4	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
5	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
6,14	VDDPCI	PWR	Supply for PCICLK_F and PCICLK (0:5), nominal 3.3V
7	PCICLK_F	OUT	Free running PCI clock
	FS1[1, 2]	IN	Frequency select pin. Latched Input
8	PCICLK0	OUT	PCI clock output.
	FS2[1, 2]	IN	Frequency select pin. Latched Input
10, 11, 12, 13	PCICLK(1:4)	OUT	PCI clock outputs.
15	PCICLK5	OUT	PCI clock output. (In desktop mode, MODE=1)
	PCI_STOP#[1]	IN	Halts PCICLK(0:5) clocks at logic 0 level, when input low (In mobile mode, MODE=0)
17, 18, 20, 21, 26, 27, 30, 31, 36, 37, 39, 40, 42, 43, 45, 46	SDRAM (0:15)	OUT	SDRAM clock outputs.
19, 25, 38, 44	VDDSDR	PWR	Supply for SDRAM (0:15), PLL Core and 24MHz clocks, nominal 3.3V.
23	SDATA	IN	Data input for I^2C serial input.
24	SCLK	IN	Clock input of I^2C input
32	VDD48	PWR	Supply for 48MHz clocks 3.3V nominal
33	24MHz	OUT	24MHz output clock
	MODE[1, 2]	IN	Pin 15, pin 54 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input.
34	48MHz	OUT	48MHz output clock
	FS0[1, 2]	IN	Frequency select pin. Latched Input
48, 49, 51, 52	CPUCLK(0:3)	OUT	CPU clock outputs, powered by VDDL2. Low if CPU_STOP#=Low
50	VDDLCPU	PWR	Supply for CPU (0:3), either 2.5V or 3.3V nominal
54	REF1	OUT	14.318 MHz reference clock, (in Desktop Mode, MODE=1) This REF output is the STRONGER buffer for ISA BUS loads.
	CPU_STOP#[1]	IN	Halts CPUCLK (0:3) clocks at logic 0 level, when input low (in Mobile Mode, MODE=0)
55	IOAPIC	OUT	IOAPIC clock output. 14.318 MHz Powered by VDDL1.
56	VDDLIOAPIC	PWR	Supply for IOAPIC, either 2.5 or 3.3V nominal

Notes:

1: Internal Pull-up Resistor of 240K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

Mode Pin - Power Management Input Control

MODE, Pin 25 (Latched Input)	Pin 46	Pin 15
0	CPU_STOP# (INPUT)	PCI_STOP# (INPUT)
1	REF1 (OUTPUT)	PCICLK5 (OUTPUT)

Power Management Functionality

CPU_STOP#	PCI_STOP#	CPUCLK Outputs	PCICLK (0:5)	PCICLK_F, REF, 24/48MHz and SDRAM	Crystal OSC	VCO
0	1	Stopped Low	Running	Running	Running	Running
1	1	Running	Running	Running	Running	Running
1	0	Running	Stopped Low	Running	Running	Running

CPU 3.3#_2.5V Buffer selector for CPUCLK and IOAPIC drivers.

CPU3.3#_2.5 Input level (Latched Data)	Buffer Selected for operation at:
1	2.5V VDD
0	3.3V VDD

Functionality

V_{DD}1,2,3 = 3.3V±5%, V_{DDL}1,2 = 2.5V±5% or 3.3±5%, TA=0 to 70°C
Crystal (X1, X2) = 14.31818MHz

FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	PCICLK (MHz)	REF, IOAPIC (MHz)
0	0	0	0	90.00	90.00	45.00	14.318
0	0	0	1	89.01	89.01	44.51	14.318
0	0	1	0	88.00	88.00	44.00	14.318
0	0	1	1	86.99	86.99	43.50	14.318
0	1	0	0	85.91	85.91	42.95	14.318
0	1	0	1	85.01	85.01	42.51	14.318
0	1	1	0	84.00	84.00	42.00	14.318
0	1	1	1	82.00	82.00	41.00	14.318
1	0	0	0	81.01	81.01	40.00	14.318
1	0	0	1	80.00	80.00	41.65	14.318
1	0	1	0	83.31	83.31	34.24	14.318
1	0	1	1	68.49	68.49	34.24	14.318
1	1	0	0	78.00	78.00	39.00	14.318
1	1	0	1	75.00	75.00	37.50	14.318
1	1	1	0	71.99	71.99	35.99	14.318
1	1	1	1	66.82	66.82	33.41	14.318

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controler (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description				PWD
Bit 7	0 - ±0.25% Spread Spectrum Modulation 1 - ±0.6% Spread Spectrum Modulation				1
Bit (2,6:4)	Bit (2,6:4)	CPUCLK (MHz)	SDRAM (MHz)	PCICLK (MHz)	XXX Note 1
	0000	90.00	90.00	45.00	
	0001	89.01	89.01	44.51	
	0010	88.00	88.00	44.00	
	0011	86.99	86.99	43.50	
	0100	85.91	85.91	42.95	
	0101	85.01	85.01	42.51	
	0110	84.00	84.00	42.00	
	0111	82.00	82.00	41.00	
	1000	81.01	81.01	40.51	
	1001	80.00	80.00	40.00	
	1010	83.31	83.31	41.65	
	1011	68.49	68.49	34.24	
	1100	78.00	78.00	39.00	
	1101	75.00	75.00	37.50	
	1110	71.99	71.99	35.99	
	1111	66.82	66.82	33.41	
Bit 3	0-Frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 2,6:4				0
Bit 1	0 - Normal operation 1 - Spread Spectrum Enabled				1
Bit 0	0 - Running 1 - Tristate all outputs				0

Note 1. Default at Power-up will be for latched logic inputs to define frequenc,. Bits 2, 6:4 are default to 0000.

Byte 1: Control Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	X	FS2#
Bit 4	-	X	FS0#
Bit 3	48	1	CPUCLK3 (Act/Inact)
Bit 2	49	1	CPUCLK2 (Act/Inact)
Bit 1	51	1	CPUCLK1 (Act/Inact)
Bit 0	52	1	CPUCLK0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 2: Control Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	X	FS3#
Bit 6	7	1	PCICLK_F (Act/Inact)
Bit 5	15	1	PCICLK5 (Act/Inact)
Bit 4	13	1	PCICLK4 (Act/Inact)
Bit 3	12	1	PCICLK3 (Act/Inact)
Bit 2	11	1	PCICLK2 (Act/Inact)
Bit 1	10	1	PCICLK1 (Act/Inact)
Bit 0	8	1	PCICLK0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 3: Control Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	36	1	SDRAM7 (Act/Inact)
Bit 6	37	1	SDRAM6 (Act/Inact)
Bit 5	39	1	SDRAM5 (Act/Inact)
Bit 4	40	1	SDRAM4 (Act/Inact)
Bit 3	42	1	SDRAM3 (Act/Inact)
Bit 2	43	1	SDRAM2 (Act/Inact)
Bit 1	45	1	SDRAM1 (Act/Inact)
Bit 0	46	1	SDRAM0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 4: Control Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	26	1	SDRAM15 (Act/Inact)
Bit 6	27	1	SDRAM14 (Act/Inact)
Bit 5	30	1	SDRAM13 (Act/Inact)
Bit 4	31	1	SDRAM12 (Act/Inact)
Bit 3	17	1	SDRAM11 (Act/Inact)
Bit 2	18	1	SDRAM10 (Act/Inact)
Bit 1	20	1	SDRAM9 (Act/Inact)
Bit 0	21	1	SDRAM8 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

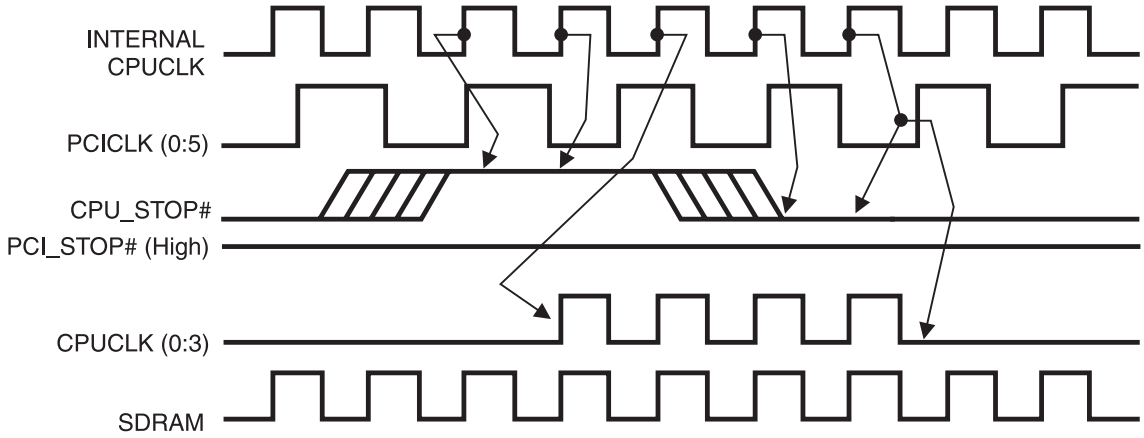
Byte 5: Control Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	55	1	IOAPIC (Act/Inact)
Bit 3	-	X	FS1#
Bit 2	-	1	(Reserved)
Bit 1	54	1	REF1 (Act/Inact)
Bit 0	2	1	REF0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS9250-13**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.

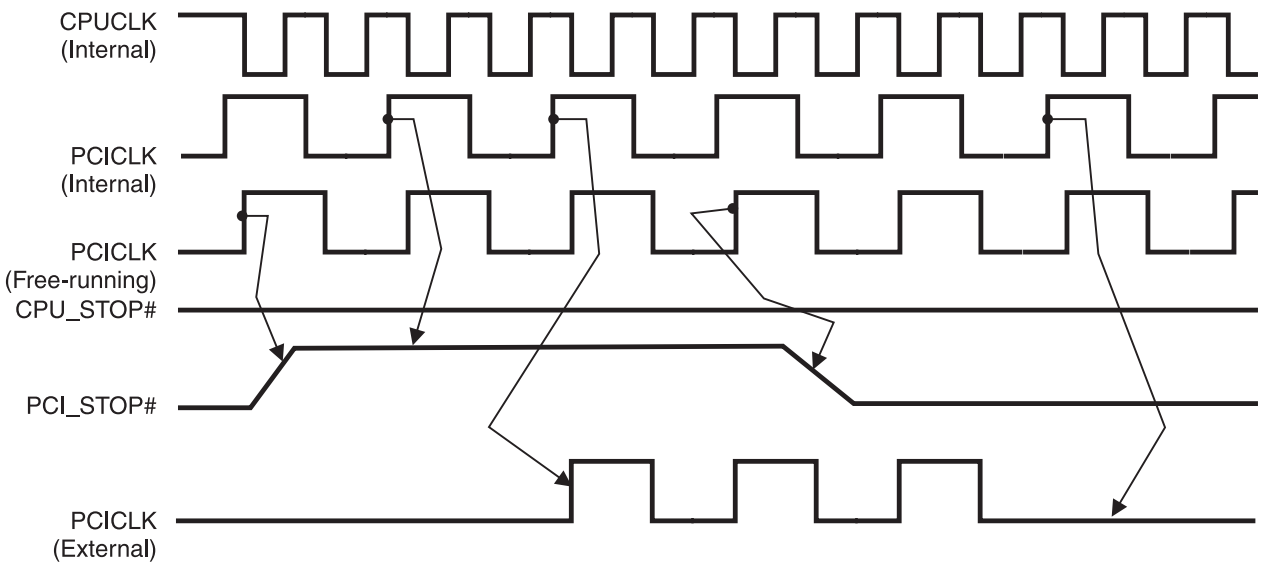


Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9250-13.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9250-13**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9250-13** internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

Shared Pin Operation - Input/Output Pins

Pins 2, 7, 8, 25, and 26 on the **ICS9250-13** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

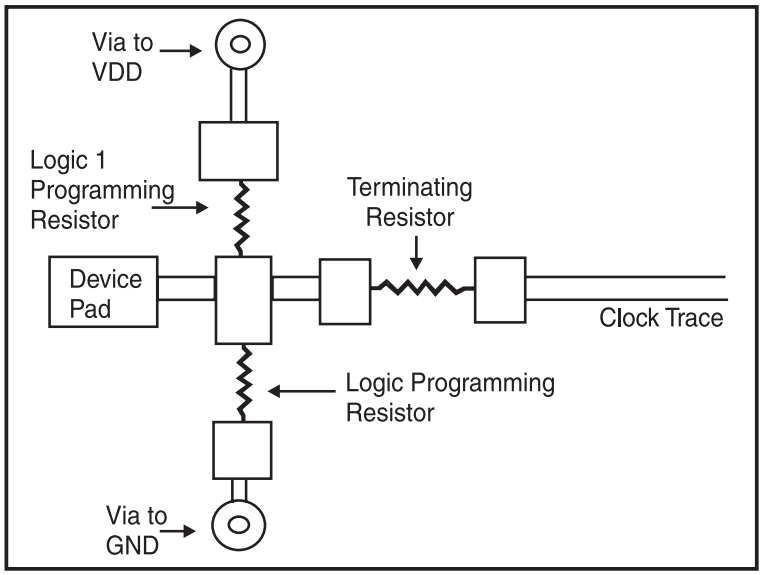


Fig. 1

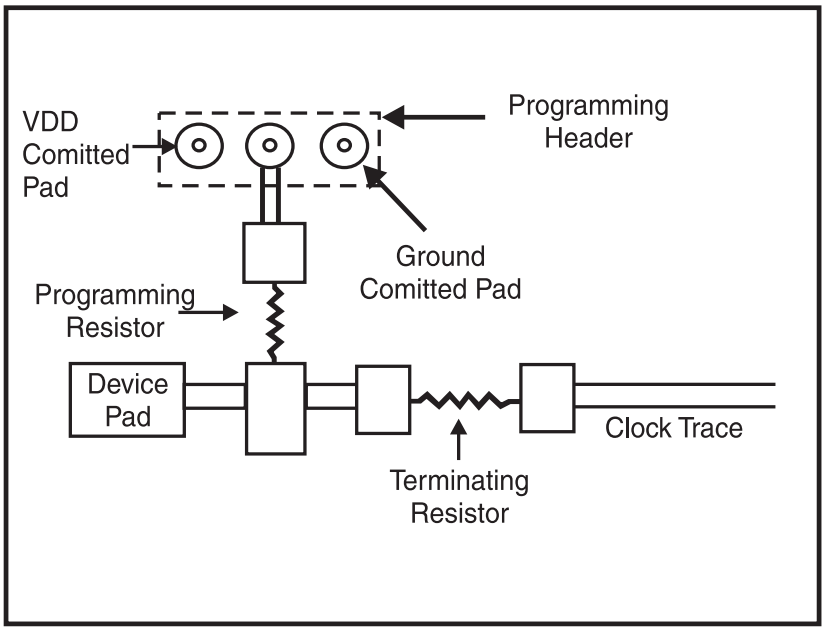

VDD
Comitted
Pad
Programming
Header
Ground
Comitted Pad
Programming
Resistor
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2a

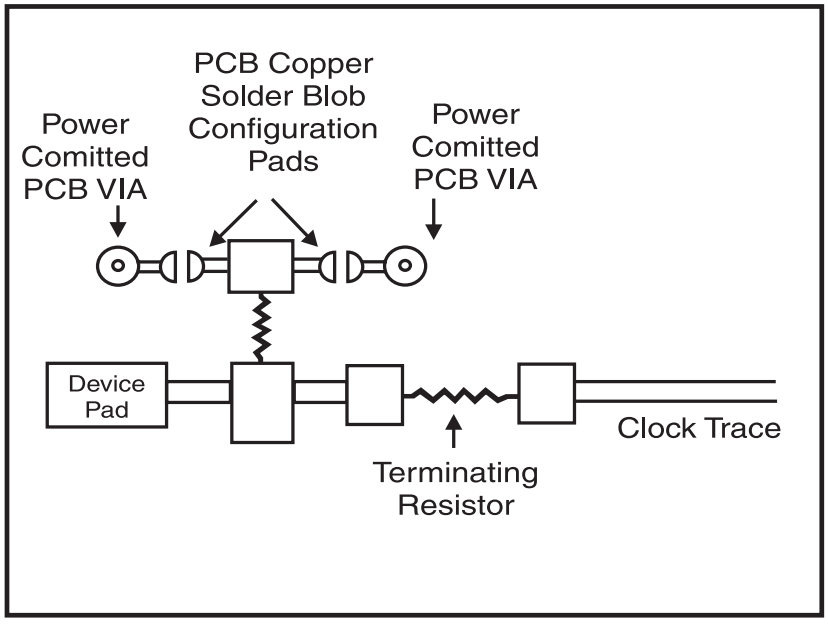

PCB Copper
Solder Blob
Configuration
Pads
Power
Comitted
PCB VIA
Power
Comitted
PCB VIA
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2b

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5% VDDL = 2.5V ± 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD2.5OP}$	C_L = 0 pF; Select @ 66MHz			160	mA
Input Frequency	F_i	V_{DD} = 3.3 V	12	14.32	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{Trans}	To 1st crossing of target Freq.		1.3	2	ms
Settling Time[1]	T_s			0.3		
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.		< 2	2	ms
Skew[1]	$T_{CPU-PCI2}$	V_T = 1.5 V	1	2.15	4	ns
	$T_{CPU-SDRAM2}$	V_T = 1.5 V		70	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP}$	C_L = 0 pF; Select @ 66.8 MHz			20	mA
Skew[1]	$T_{CPU-PCI2}$	V_T=1.5 V; VTL=1.25 V	1	2.15	4	ns
	$T_{CPU-SDRAM2}$	VT=1.5 V;VTL=1.25 V		70	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -25 mA	2.4	2.85		V
Output Low Voltage	V_{OL3}	I_{OL} = 20 mA		0.35	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V		-60	-40	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	35	45		mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.6	2.4	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.8	2.2	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	46	52	56	%
Skew[1]	T_{sk1}	V_T = 1.5 V		325	500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -8.0 mA	2	2.4		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.32	0.4	V
Output High Current	I_{OH2B}	V_{OH} =1.7 V		-37	-16	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	26		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.3	1.9	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.5	1.9	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	50	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		78	175	ps
Jitter, Cycle-to-cycle	$tj_{cyc-cyc2B}$[1]	V_T = 1.25 V, Normal or Spread mode		170	350	ps
Jitter, One Sigma	$t_{j1\sigma 2B}$[1]	V_T = 1.25 V		45	150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250	120	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -28 mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.17	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-60	-40	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	41	45		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.4	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		280	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1a}$	VT = 1.5 V, Normal or Spread mode		230	400	ps
Jitter, One Sigma[1]	$t_{j1\sigma1a}$	V_T = 1.5 V		75	150	ps
Jitter, Absolute[1]	t_{jabs1a}	V_T = 1.5 V	-250	160	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH4B}	I_{OH} = -8.0 mA	2	2.3		V
Output Low Voltage	V_{OL4B}	I_{OL} = 12 mA		0.3	0.4	V
Output High Current	I_{OH4B}	V_{OH} =1.7 V		-26	-15	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	19	27		mA
Rise Time	t_{r4B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.3	2.2	ns
Fall Time	t_{f4B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.35	2	ns
Duty Cycle	d_{t4B}[1]	V_T = 1.25 V	45	52	55	%
Jitter, One Sigma	$t_{j1\sigma4B}$[1]	V_T = 1.25 V		235	350	ps
Jitter, Absolute	t_{jabs4B}[1]	V_T = 1.25 V	-800	510	800	ps

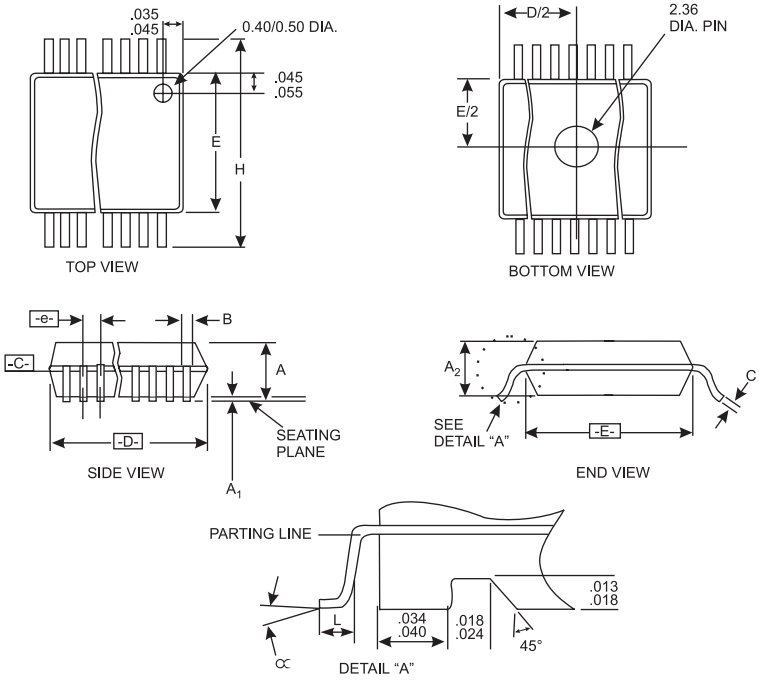
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 24 MHz, 48 MHz

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 10 mA		0.3	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-30	-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	23		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.95	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.1	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	51	55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V		170	400	ps
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V	-800	400	800	ps

[1]Guaranteed by design, not 100% tested in production.



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AD	.720	.725	.730	56
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	.006	.0085					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

SSOP Package

Ordering Information

ICS9250yF-13

Example:

ICS XXXX y F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Revision Designator

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device