



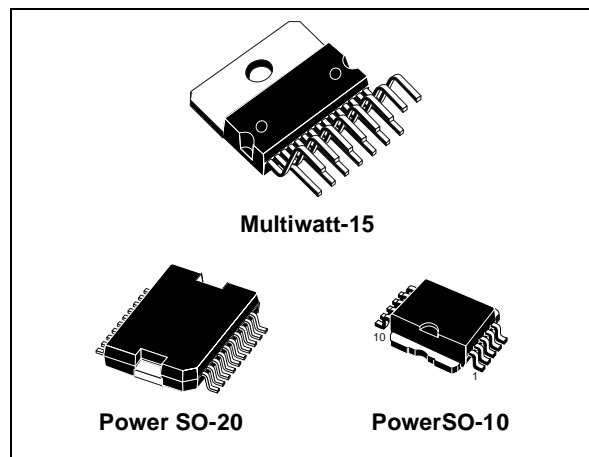
LNBP SUPPLY AND CONTROL VOLTAGE REGULATOR (PARALLEL INTERFACE)

- COMPLETE INTERFACE FOR TWO LNBS
REMOTE SUPPLY AND CONTROL
- LNB SELECTION AND STAND-BY
FUNCTION
- BUILT-IN TONE OSCILLATOR FACTORY
TRIMMED AT 22KHz
- FAST OSCILLATOR START-UP FACILITATES
DiSEqC™ ENCODING
- TWO SUPPLY INPUTS FOR LOWEST
DISSIPATION
- BYPASS FUNCTION FOR SLAVE
OPERATION
- LNB SHORT CIRCUIT PROTECTION AND
DIAGNOSTIC
- AUXILIARY MODULATION INPUT EXTENDS
FLEXIBILITY
- CABLE LENGTH COMPENSATION
- INTERNAL OVER TEMPERATURE
PROTECTION
- BACKWARD CURRENT PROTECTION

DESCRIPTION

Intended for analog and digital satellite receivers, the LNBP is a monolithic linear voltage regulator, assembled in Multiwatt-15, PowerSO-20 and PowerSO-10, specifically designed to provide the powering voltages and the interfacing signals to the LNB downconverter situated in the antenna via the coaxial cable. Since most satellite receivers have two antenna ports, the output voltage of the regulator is available at one of two logic-selectable output pins (LNBA, LNBB). When the IC is powered and put in Stand-by (EN pin LOW), both regulator outputs are disabled to allow the antenna downconverters to be supplied/controlled by others satellite receivers sharing the same coaxial lines. In this occurrence the device will limit at 3 mA (max) the backward current that could flow from LNBA and LNBB output pins to GND.

For slave operation in single dish, dual receiver systems, the bypass function is implemented by an electronic switch between the Master Input pin (MI) and the LNBA pin, thus leaving all LNB powering and control functions to the Master Receiver. This electronic switch is closed when the device is powered and EN pin is LOW.



The regulator outputs can be logic controlled to be 13 or 18 V (typ.) by mean of the VSEL pin for remote controlling of LNBS. Additionally, it is possible to increment by 1V (typ.) the selected voltage value to compensate the excess voltage drop along the coaxial cable (LLC pin HIGH).

In order to reduce the power dissipation of the device when the lowest output voltage is selected, the regulator has two Supply Input pins V_{CC1} and V_{CC2} . They must be powered respectively at 16V (min) and 23V (min), and an internal switch automatically will select the suitable supply pin according to the selected output voltage. If adequate heatsink is provided and higher power losses are acceptable, both supply pins can be powered by the same 23V source without affecting any other circuit performance.

The ENT (Tone Enable) pin activates the internal oscillator so that the DC output is modulated by a ± 0.3 V, 22KHz (typ.) square wave. This internal oscillator is factory trimmed within a tolerance of ± 2 KHz, thus no further adjustments neither external components are required.

A burst coding of the 22KHz tone can be accomplished thanks to the fast response of the ENT input and the prompt oscillator start-up. This helps designers who want to implement the DiSEqC™ protocols (*).

In order to improve design flexibility and to allow implementation of newcoming LNB remote control standards, an analogic modulation

input pin is available (EXTM). An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. When external modulation is not used, the relevant pin can be left open.

Two pins are dedicated to the overcurrent protection/monitoring: CEXT and OLF. The overcurrent protection circuit works dynamically: as soon as an overload is detected in either LNB output, the output is shut-down for a time t_{off} determined by the capacitor connected between CEXT and GND. Simultaneously the OLF pin, that is an open collector diagnostic output flag, from HIGH IMPEDANCE state goes LOW.

After the time has elapsed, the output is resumed for a time $t_{on}=1/15t_{off}$ (typ.) and OLF goes in HIGH

IMPEDANCE. If the overload is still present, the protection circuit will cycle again through t_{off} and t_{on} until the overload is removed. Typical $t_{on}+t_{off}$ value is 1200ms when a 4.7 μ F external capacitor is used.

This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start up even with highly capacitive loads on LNB outputs.

The device is packaged in Multiwatt15 for thru-holes mounting and in PowerSO-20 for surface mounting. When a limited functionality in a smaller package matches design needs, a range of cost-effective PowerSO-10 solutions is also offered. All versions have built-in thermal protection against overheating damage.

(*): External components are needed to comply to level 2.x and above (bidirectional) DiSEqC™ bus hardware requirements. DiSEqC™ is a trademark or EUTELSAT.

Table 1: Ordering Codes

TYPE	Multiwatt-15	PowerSO-20	PowerSO-10
LNBP10			LNBP10SP-TR (*)
LNBP11			LNBP11SP-TR (*)
LNBP12			LNBP12SP-TR (*)
LNBP13			LNBP13SP-TR (*)
LNBP14			LNBP14SP-TR (*)
LNBP15			LNBP15SP-TR (*)
LNBP16			LNBP16SP-TR (*)
LNBP20	LNBP20CR	LNBP20PD-TR	

(*) Available on request

Figure 1: Pin Configuration (top view)

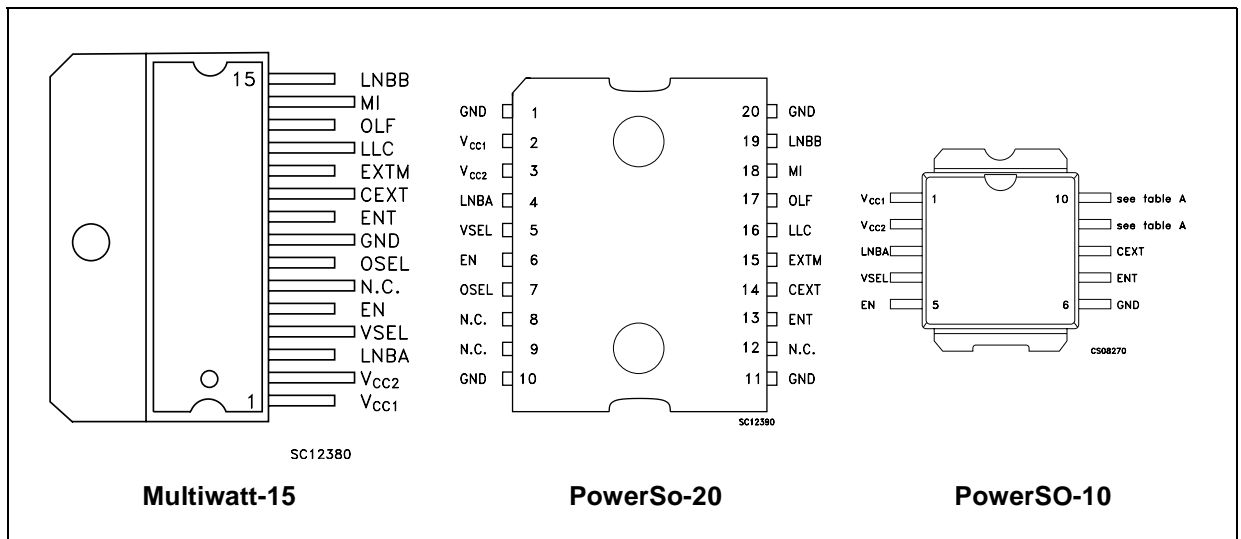


Table 2: Pin Description

SYMBOL	NAME	FUNCTION	PIN NUMBER vs SALES TYPE (LNBP)								
			20CR	20PD	10SP	11SP	12SP	13SP	14SP	15SP	16SP
V _{CC1}	Supply Input 1	15V to 25V supply. It is automatically selected when V _{OUT} = 13 or 14V	1	2	1	1	1		1	1	1
V _{CC2}	Supply Input 2	22V to 25V supply. It is automatically selected when V _{OUT} = 18 or 19V	2	3	2	2	2	2	2	2	2
LNBA	Output Port	See truth table voltage and port selection. In stand-by mode this port is powered by the MI pin via the internal Bypass Switch	3	4	3	3	3	3	3	3	3
V _{SEL}	Output Voltage Selection: 13 or 18V (typ)	Logic control input: see truth table	4	5	4	4	4	4	4	4	4
EN	Port Enable	Logic control input: see truth table	5	6	5	5	5	5	5	5	5
OSEL	Port Selection	Logic control input: see truth table	7	7	9	NA	NA	NA	NA	NA	NA
GND	Ground	Circuit Ground. It is internally connected to the die frame	8	1 10 11 20	6	6	6	6	6	6	6
ENT	22KHz Tone Enable	Logic control input: see truth table	9	13	7	7	7	7	7	7	7
CEXT	External Capacitor	Timing Capacitor used by the Dynamic Overload protection. Typical application is 4.7μF for a 1200ms cycle	10	14	8	8	8	8	8	8	8
EXTM	External Modulator	External Modulation Input. Needs DC decoupling to the AC source. if not used, can be left open.	11	15	NA	NA	NA	9	NA	9	9
LLC	Line Length Compens. (1V typ)	Logic control input: see truth table	12	16	NA	NA	9	NA	9	NA	10
OLF	Over Load Flag	Logic output (open collector). Normally in HIGH IMPEDANCE, goes LOW when current or thermal overload occurs	13	17	NA	9	NA	NA	10	10	NA
MI	Master Input	In stand-by mode, the voltage on MI is routed to LNBA pin. Can be left open if bypass function is not needed	14	18	NA	10	10	10	NA	NA	NA
LNBB	Output Port	See truth tables for voltage and port selection	15	19	10	NA	NA	NA	NA	NA	NA

NOTE: the limited pin availability of the PowerSO-10 package leads to drop some functions.

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage (V_{CC1} , V_{CC2} , MI)	28	V
I_O	Output Current (LNBA, LNBB)	Internally Limited	mA
V_I	Logic Input Voltage (ENT, EN OSEL, VSEL, LLC)	-0.5 to 7	V
I_{SW}	Bypass Switch Current	900	mA
P_D	Power Dissipation at $T_{case} < 85^\circ\text{C}$	14	W
T_{stg}	Storage Temperature Range	-40 to +150	$^\circ\text{C}$
T_{op}	Operating Junction Temperature Range	-40 to +125	$^\circ\text{C}$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4: Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal Resistance Junction-case	2	$^\circ\text{C}/\text{W}$

Table 5: Logic Controls Truth Table

CONTROL I/O	PIN NAME	L	H
OUT	OLF	$I_{OUT} > I_{OMAX}$ or $T_j > 150^\circ\text{C}$	$I_{OUT} < I_{OMAX}$
IN	ENT	22KHz tone OFF	22KHz tone ON
IN	EN	See Table Below	See Table Below
IN	OSEL	See Table Below	See Table Below
IN	VSEL	See Table Below	See Table Below
IN	LLC	See Table Below	See Table Below

EN	OSEL	VSEL	LLCO	V_{LNBA}	V_{LNBB}
L	X	X	X	$V_{MI} - 0.4\text{V}$ (typ.)	Disabled
H	L	L	L	13V (typ.)	Disabled
H	L	H	L	18V (typ.)	Disabled
H	L	L	H	14V (typ.)	Disabled
H	L	H	H	19V (typ.)	Disabled
H	H	L	L	Disabled	13V (typ.)
H	H	H	L	Disabled	18V (typ.)
H	H	L	H	Disabled	14V (typ.)
H	H	H	H	Disabled	19V (typ.)

NOTE: All logic input pins have internal pull-down resistor (typ. = 250K Ω)

Figure 2: Block Diagram

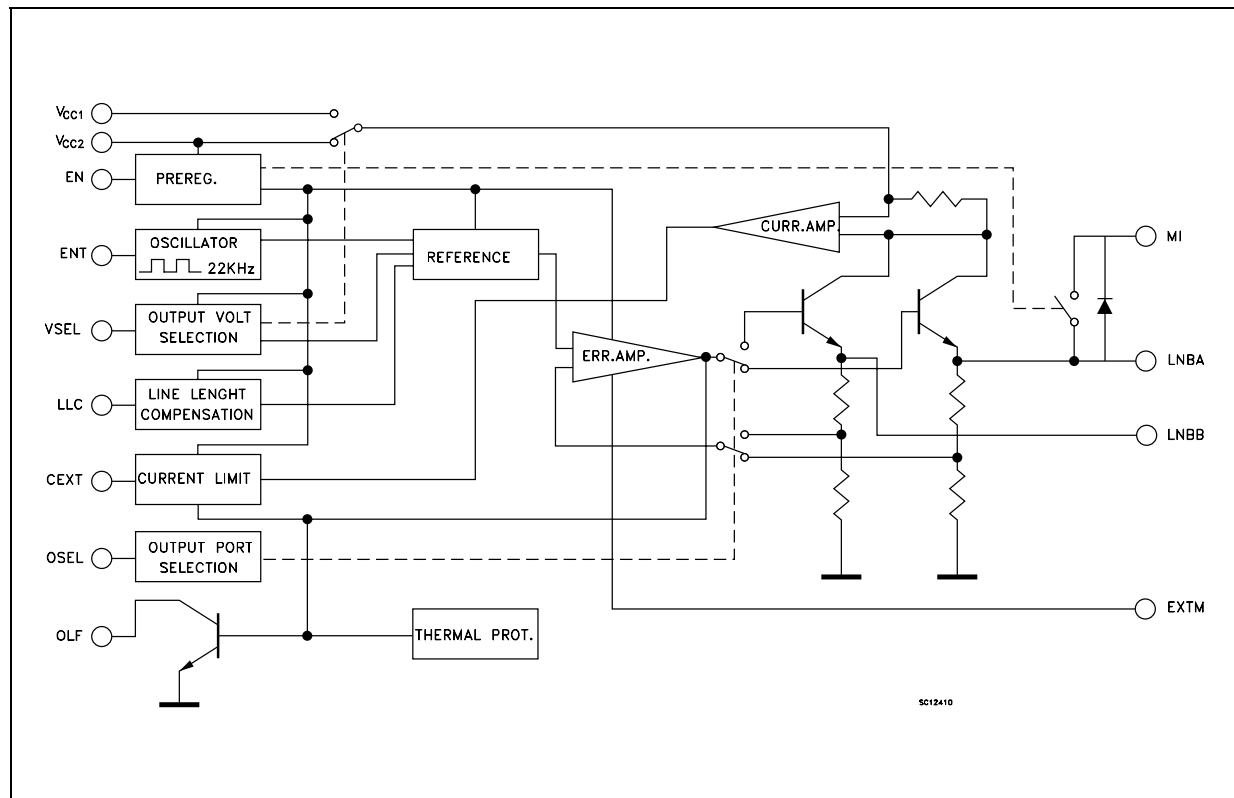


Table 6: Electrical Characteristics For LNBP Series ($T_J = 0$ to 85°C , $C_I = 0.22\mu\text{F}$, $C_O = 0.1\mu\text{F}$, $\text{EN}=\text{H}$, $\text{ENT}=\text{L}$, $\text{LLC}=\text{L}$, $V_{\text{IN}1}=16\text{V}$, $V_{\text{IN}2}=23\text{V}$ $I_{\text{OUT}}=50\text{mA}$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{IN}1}$	$V_{\text{CC}1}$ Supply Voltage	$I_O = 500\text{ mA}$, $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{L}$	15		25	V
		$I_O = 500\text{ mA}$, $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{H}$	16		25	V
$V_{\text{IN}2}$	$V_{\text{CC}2}$ Supply Voltage	$I_O = 500\text{ mA}$, $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{L}$	22		25	V
		$I_O = 500\text{ mA}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{H}$	23		25	V
$V_{\text{O}1}$	Output Voltage	$I_O = 500\text{ mA}$, $\text{VSEL}=\text{H}$, $\text{LLC}=\text{L}$	17.3	18	18.7	V
		$I_O = 500\text{ mA}$, $\text{VSEL}=\text{H}$, $\text{LLC}=\text{H}$		19		V
$V_{\text{O}2}$	Output Voltage	$I_O = 500\text{ mA}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{L}$	12.5	13	13.5	V
		$I_O = 500\text{ mA}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{H}$		14		V
ΔV_O	Line Regulation	$V_{\text{IN}1}=15$ to 18V $V_{\text{OUT}}=13\text{V}$		4	40	mV
		$V_{\text{IN}2}=22$ to 25V $V_{\text{OUT}}=18\text{V}$		4	40	mV
ΔV_O	Load Regulation	$V_{\text{IN}1}=V_{\text{IN}2}=22\text{V}$ $V_{\text{OUT}}=13$ or 18V $I_O = 50$ to 500mA		80	180	mV
SVR	Supply Voltage Rejection	$V_{\text{IN}1} = V_{\text{IN}2} = 23 \pm 0.5V_{\text{ac}}$ $f_{\text{ac}} = 120\text{ Hz}$,		45		dB
I_{MAX}	Output Current Limiting		500	650	800	mA
t_{OFF}	Dynamic Overload protection OFF Time	Output Shorted $C_{\text{EXT}} = 4.7\mu\text{F}$		1100		ms
t_{ON}	Dynamic Overload protection ON Time	Output Shorted $C_{\text{EXT}} = 4.7\mu\text{F}$		$t_{\text{OFF}}/15$		ms
f_{TONE}	Tone Frequency	$\text{ENT}=\text{H}$	20	22	24	KHz
A_{TONE}	Tone Amplitude	$\text{ENT}=\text{H}$	0.55	0.72	0.9	Vpp
D_{TONE}	Tone Duty Cycle	$\text{ENT}=\text{H}$	40	50	60	%
t_r, t_f	Tone Rise and Fall Time	$\text{ENT}=\text{H}$	5	10	15	μs
G_{EXTM}	External Modulation Gain	$\Delta V_{\text{OUT}}/\Delta V_{\text{EXTM}}$, $f = 10\text{Hz}$ to 40KHz		5		
V_{EXTM}	External Modulation Input Voltage	AC Coupling			400	mVpp
Z_{EXTM}	External Modulation Impedance	$f = 10\text{Hz}$ to 40KHz		400		Ω
V_{SW}	Bypass Switch Voltage Drop (MI to LNBA)	$\text{EN}=\text{L}$, $I_{\text{SW}}=300\text{mA}$, $V_{\text{CC}2}-V_{\text{MI}}=4\text{V}$		0.35	0.6	V
V_{OL}	Overload Flag Pin Logic LOW	$I_{\text{OL}}=8\text{mA}$		0.28	0.5	V
I_{OZ}	Overload Flag Pin OFF State Leakage Current	$V_{\text{OH}} = 6\text{V}$			10	μA
V_{IL}	Control Input Pin Logic LOW				0.8	V
V_{IH}	Control Input Pin Logic HIGH		2.5			V
I_{IH}	Control Pins Input Current	$V_{\text{IH}} = 5\text{V}$		20		μA
I_{CC}	Supply Current	Output Disabled ($\text{EN}=\text{L}$)		0.3	1	mA
		$\text{ENT}=\text{H}$, $I_{\text{OUT}}=50\text{mA}$		3.1	6	mA
I_{OBK}	Output Backward Current	$\text{EN}=\text{L}$ $V_{\text{LNBA}} = V_{\text{LNBB}} = 18\text{V}$ $V_{\text{IN}1} = V_{\text{IN}2} = 22\text{V}$ or floating		0.2	3	mA
T_{SHDN}	Temperature Shutdown Threshold			150		$^\circ\text{C}$

TYPICAL CHARACTERISTICS (unless otherwise specified $T_j = 25^\circ\text{C}$)

Figure 3: Output Voltage vs Output Current

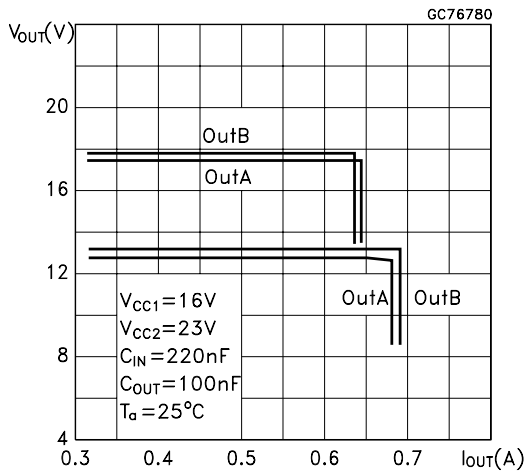


Figure 4: Tone Duty Cycle vs Temperature

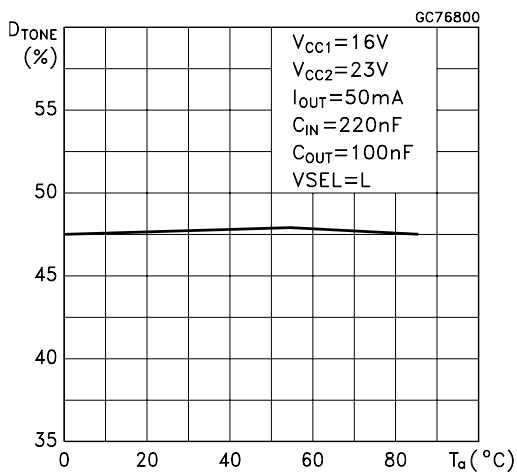


Figure 5: Tone Fall Time vs Temperature

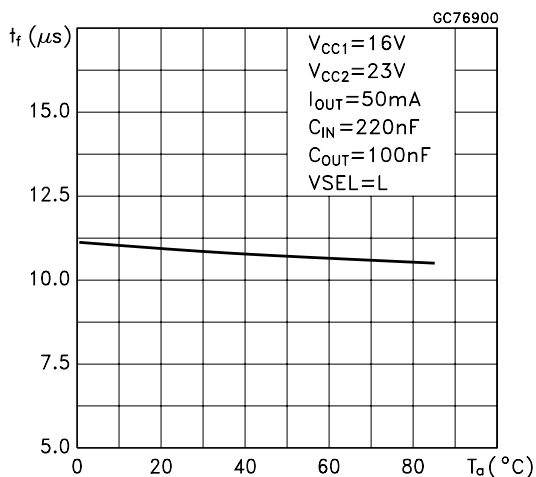


Figure 6: Tone Frequency vs Temperature

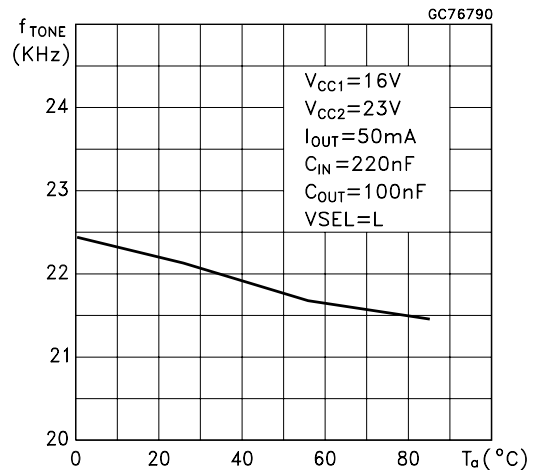


Figure 7: Tone Rise Time vs Temperature

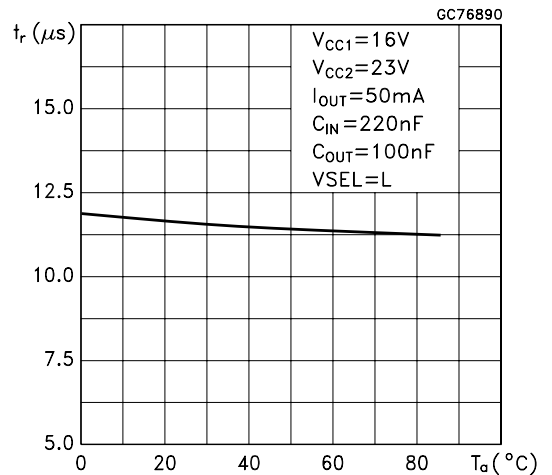


Figure 8: Tone Amplitude vs Temperature

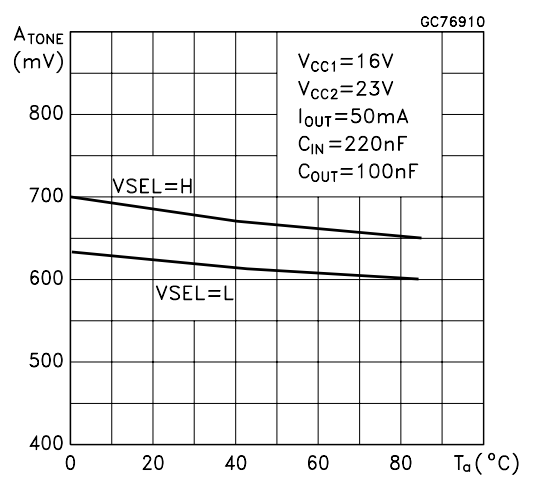


Figure 9: S.V.R. vs Frequency

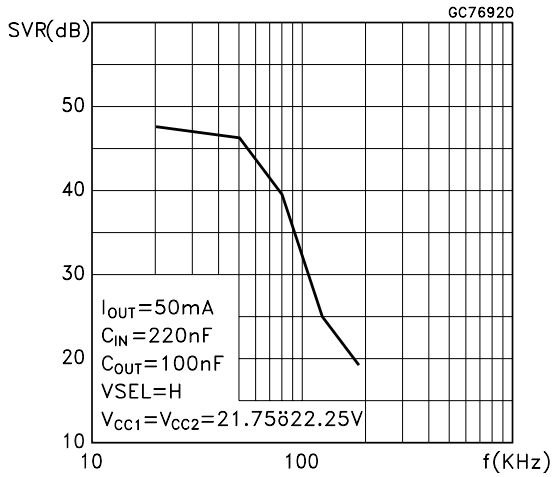


Figure 10: External Modulation vs Temperature

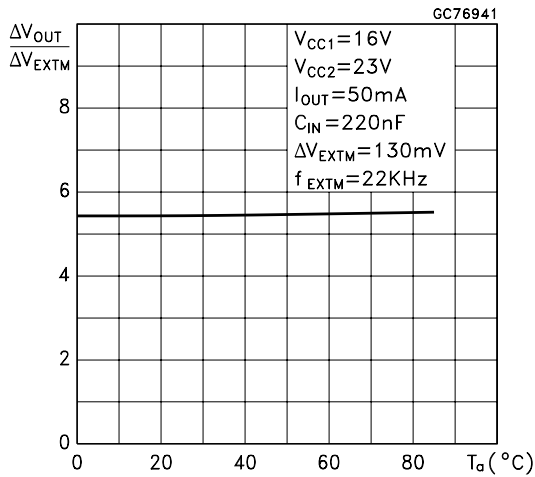


Figure 11: Bypass Switch Drop vs Output Current

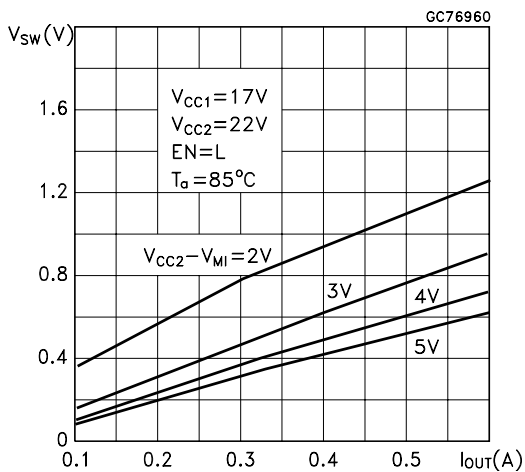


Figure 12: LNBA External Modulation gain vs Frequency

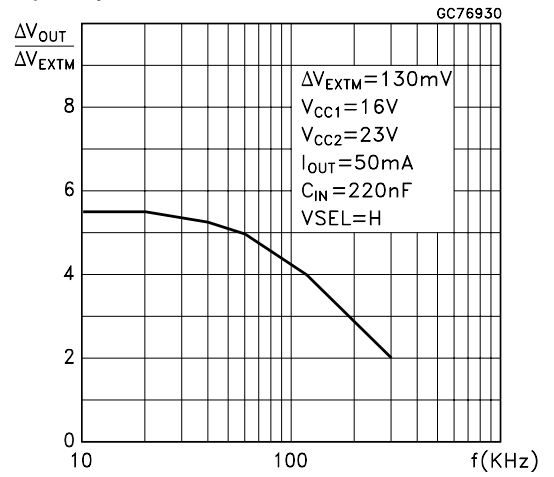


Figure 13: Bypass switch Drop vs Output Current

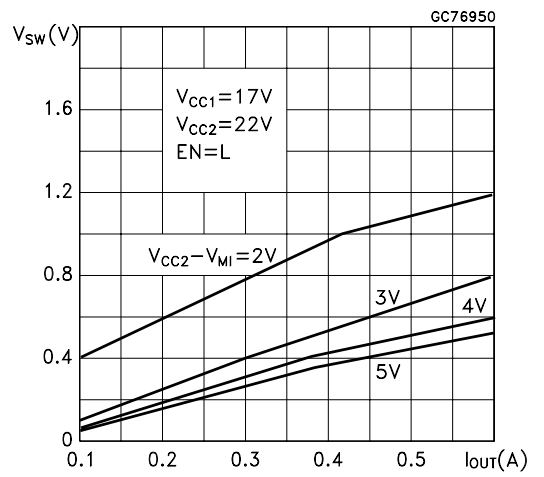


Figure 14: Overload Flag pin Logic LOW vs Flag Current

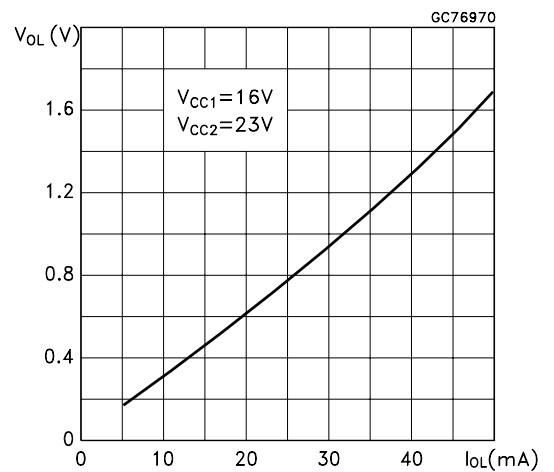


Figure 15: Supply Voltage vs Temperature

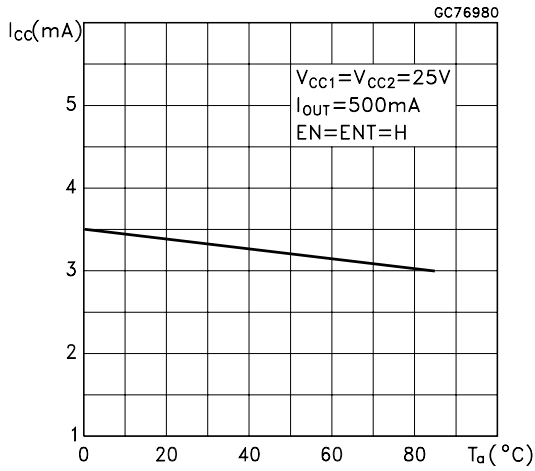


Figure 18: Tone Enable

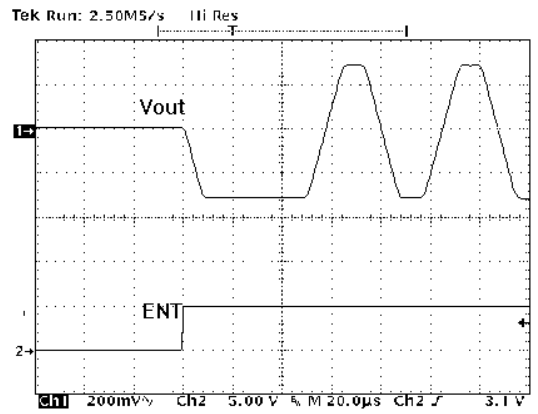


Figure 16: Supply Current vs Temperature

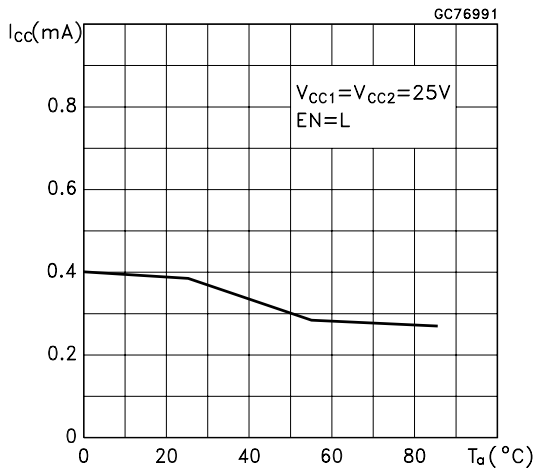


Figure 19: Tone Disable

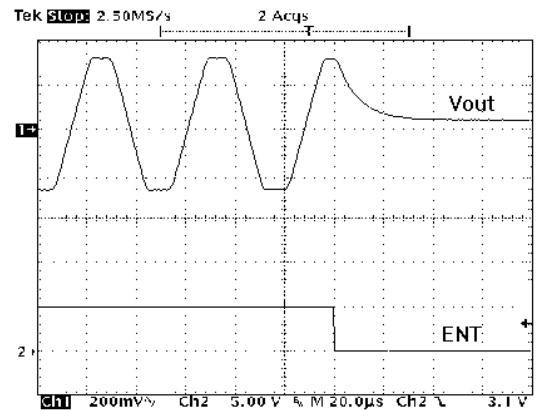


Figure 17: Dynamic Overload protection (I_{SC} vs Time)

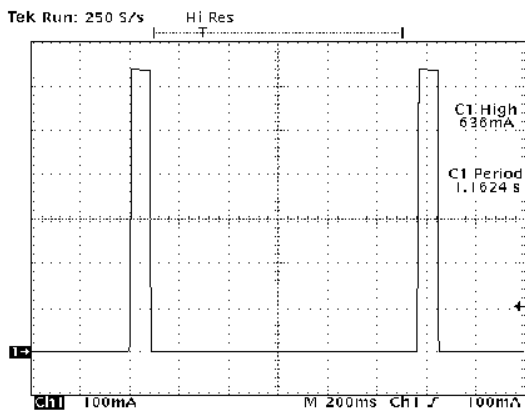


Figure 20: 22KHz Tone

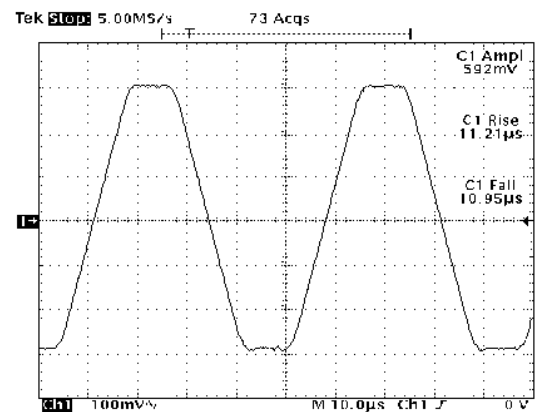


Figure 21: Enable Time

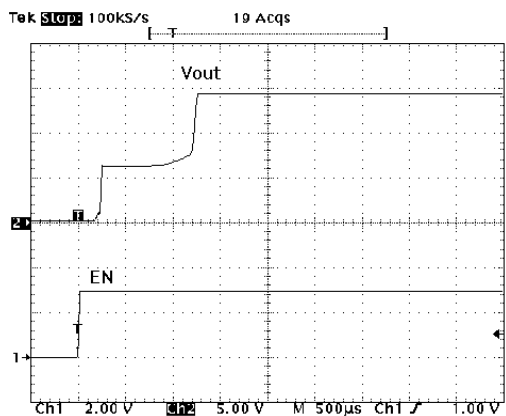


Figure 23: 18V to 13V Change

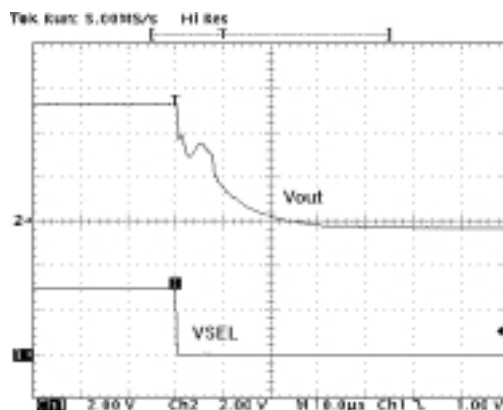


Figure 22: Disable Time

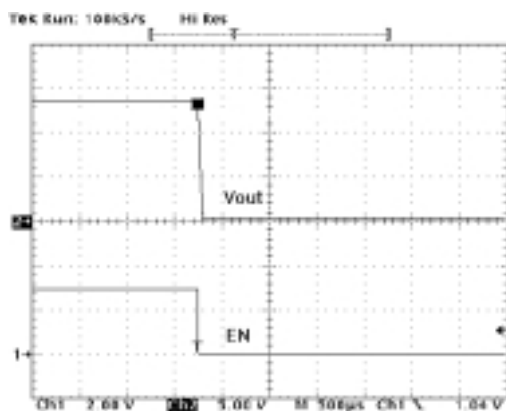


Figure 24: 18V to 13V Change

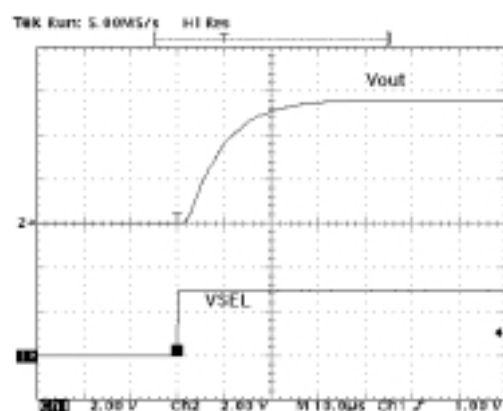


Figure 27: Using Serial Bus To Save MPU I/os

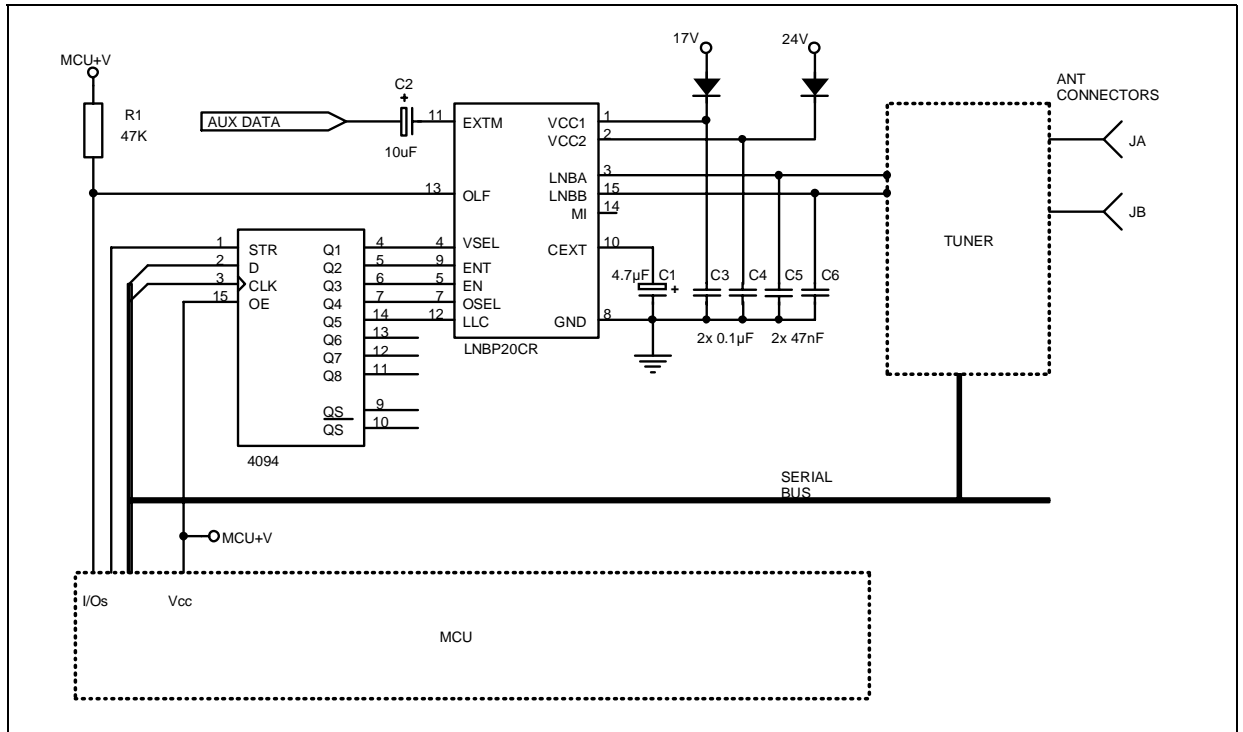


Figure 28: Two Antenna Ports Receiver - Low Cost Solution

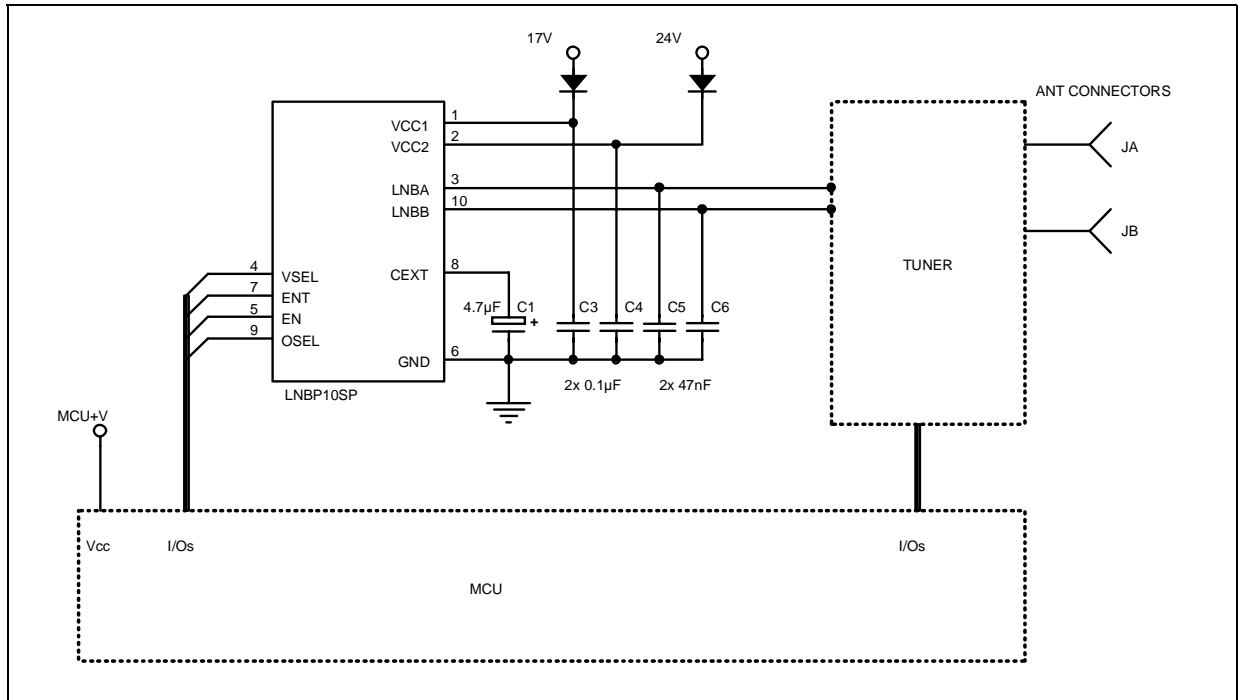


Figure 29: Connecting Together V_{CC1} And V_{CC2}

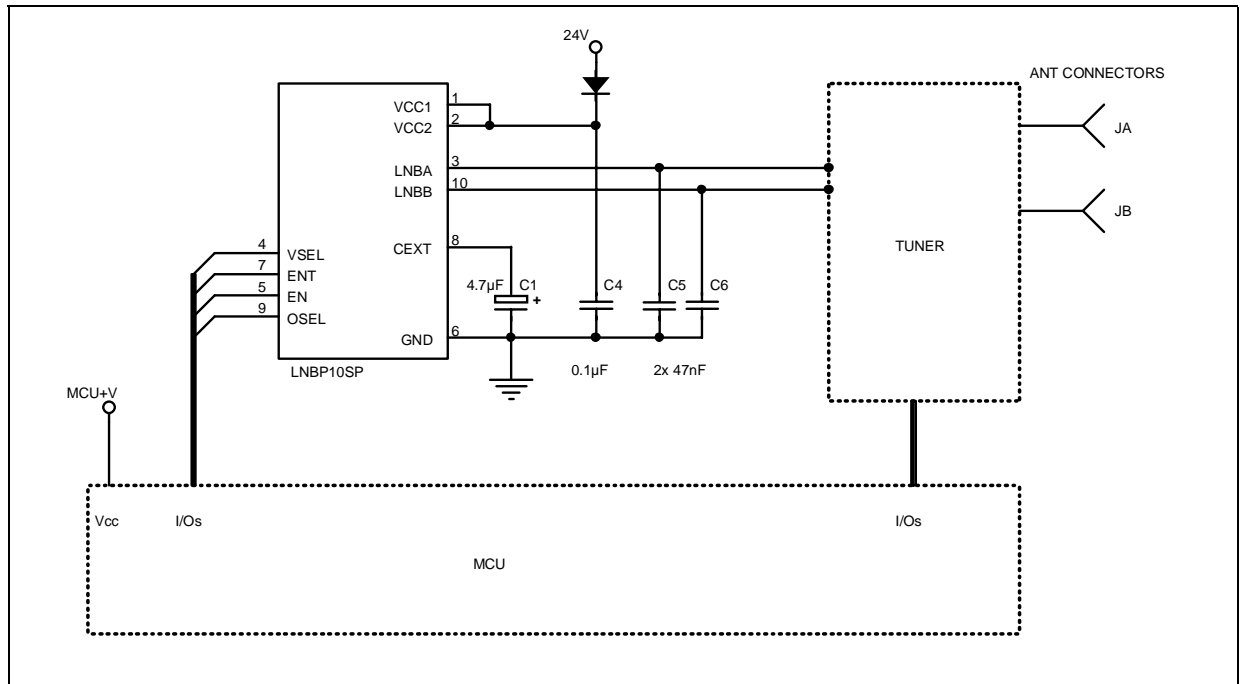


Figure 30: Single Antenna Receiver With Master Receiver Port - Low Cost Solution

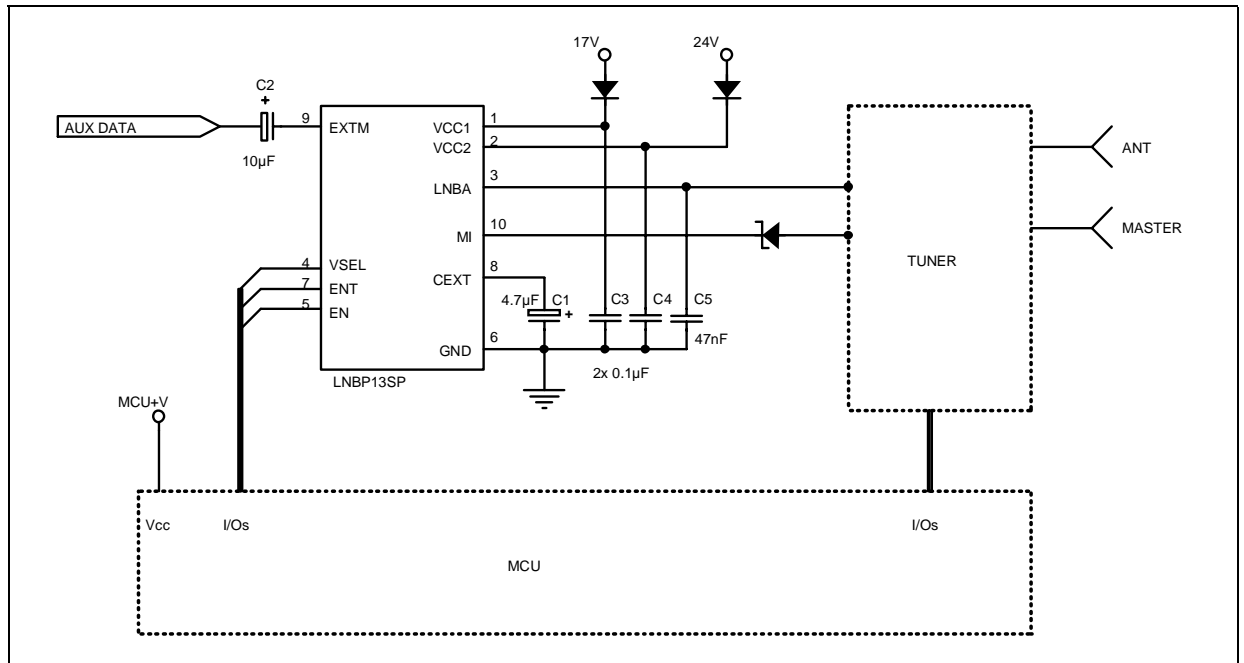
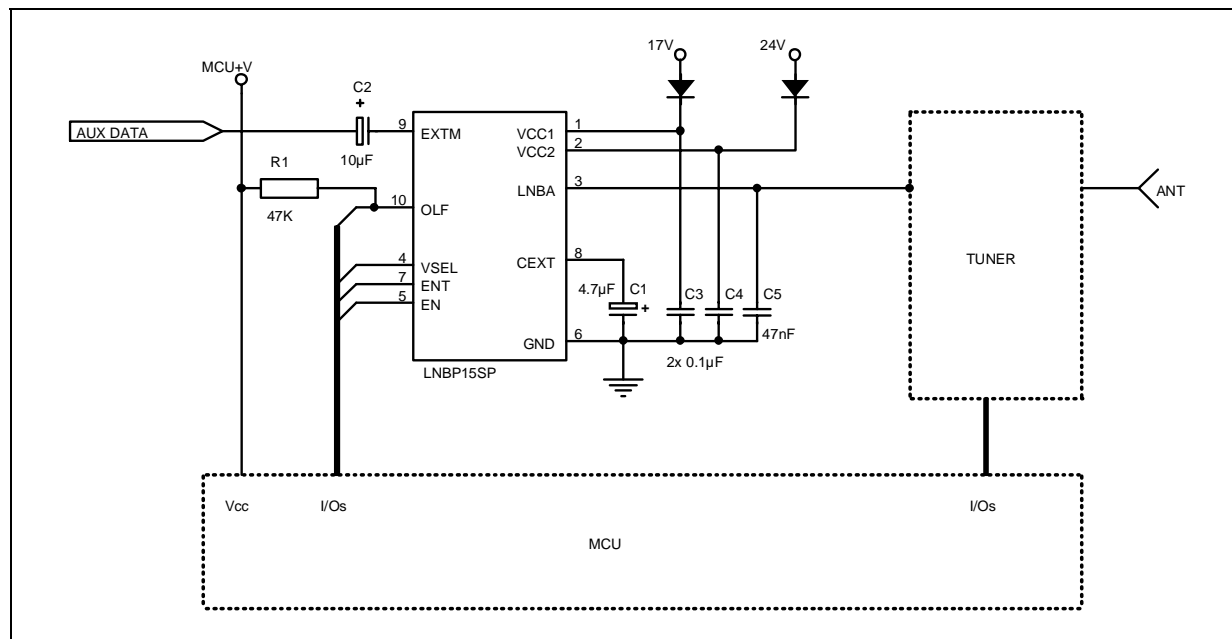
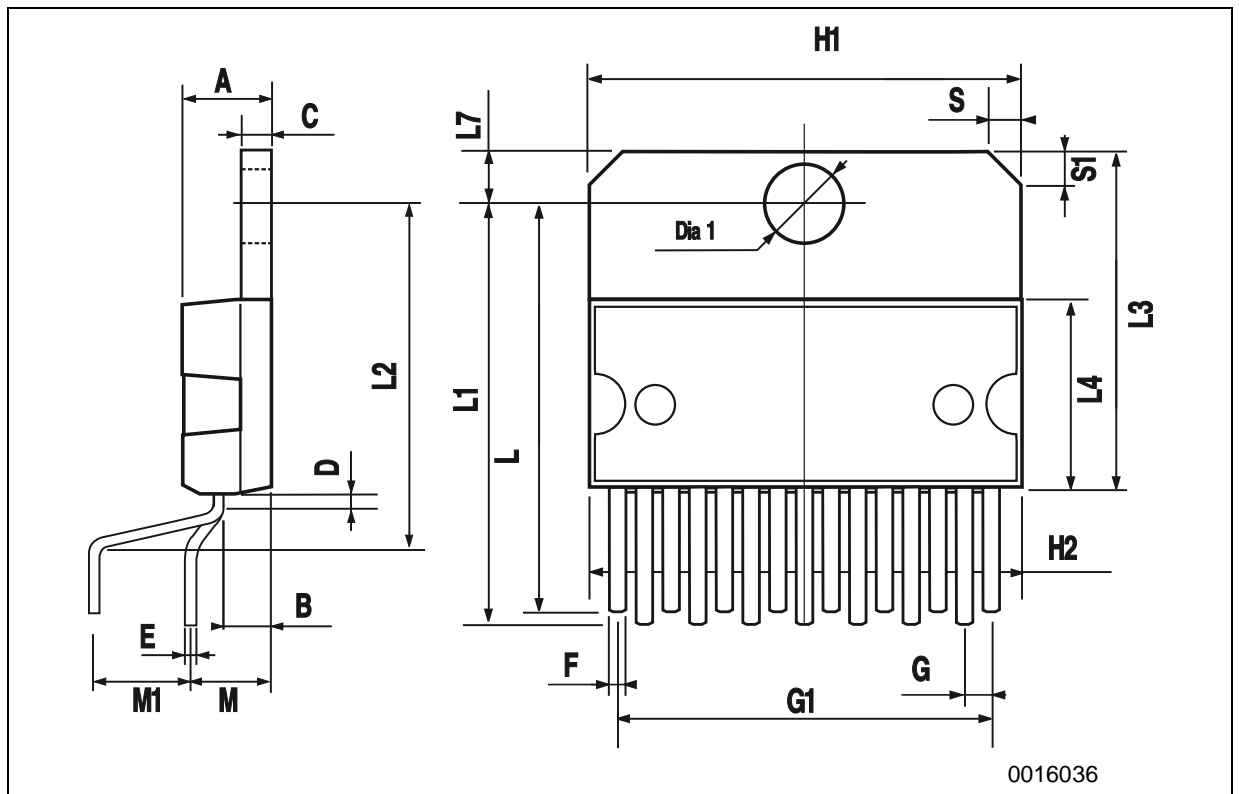


Figure 31: Single Antenna Receiver With Overload Diagnostic



MULTIWATT-15 MECHANICAL DATA

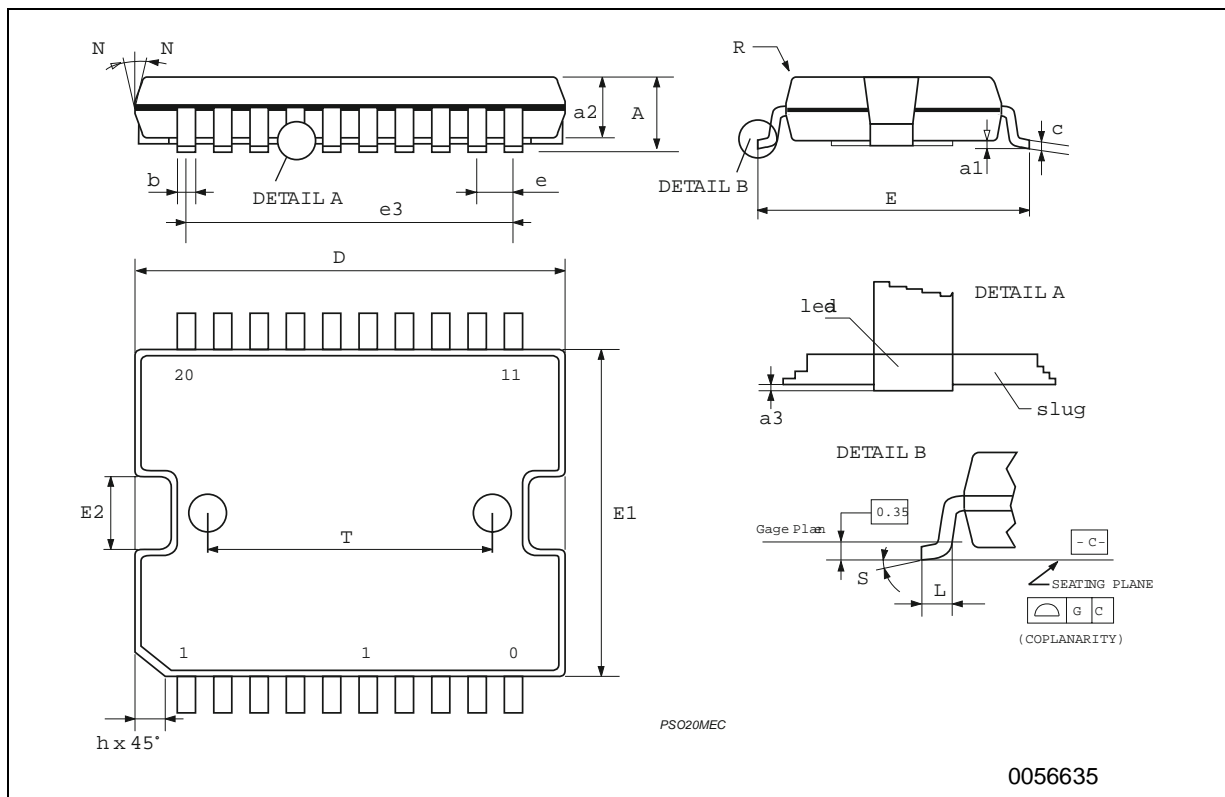
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152



PowerSO-20 MECHANICAL DATA

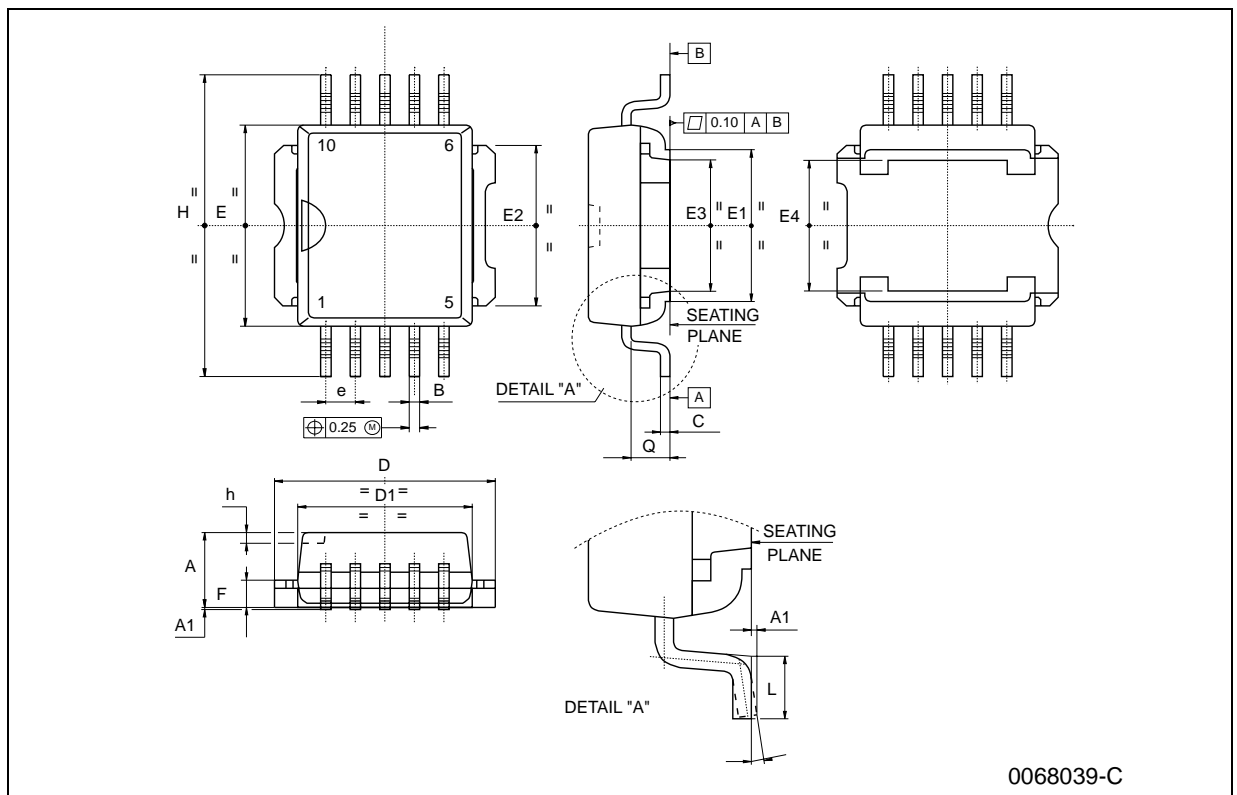
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
c	0.23		0.32	0.0090		0.0013
D (1)	15.80		16.00	0.6220		0.630
E	13.90		14.50	0.5472		0.5710
e		1.27			0.0500	
e3		11.43			0.4500	
E1 (1)	10.90		11.10	0.4291		0.4370
E2			2.90			0.1141
G	0		0.10	0.0000		0.0039
h			1.10			0.0433
L	0.80		1.10	0.0314		0.0433
N			10°			10°
S	0°		8°	0°		8°
T		10.0			0.3937	

(1) "D and E1" do not include mold flash or protusions - Mold flash or protusions shall not exceed 0.15mm (0.006")



PowerSO-10 MECHANICAL DATA

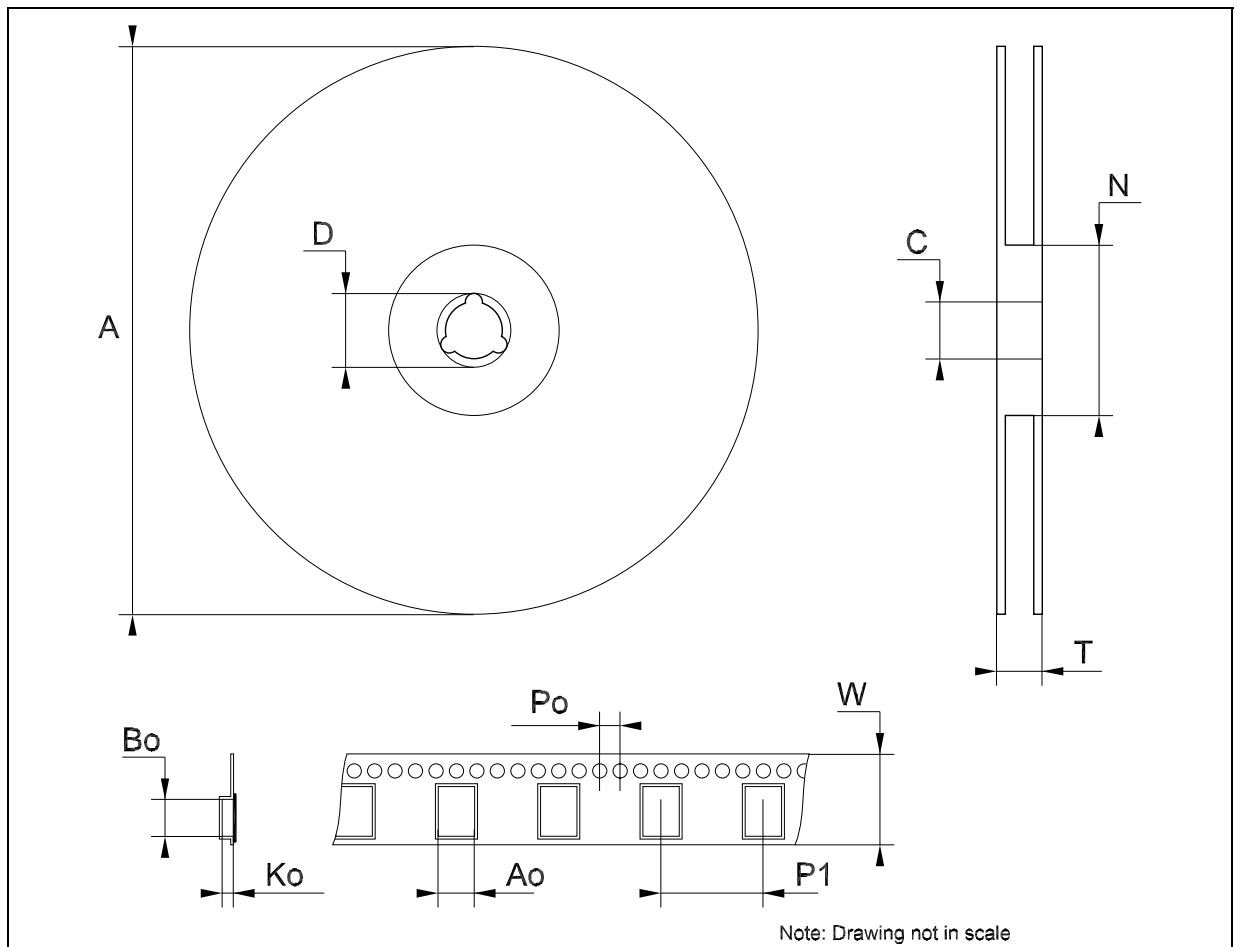
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
	0°		8°			



0068039-C

Tape & Reel PowerSO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	15.1		15.3	0.594		0.602
Bo	16.5		16.7	0.650		0.658
Ko	3.8		4.0	0.149		0.157
Po	3.9		4.1	0.153		0.161
P	23.9		24.1	0.941		0.949
W	23.7		24.3	0.933		0.957



Tape & Reel PowerSO10 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	14.9		15.1	0.587		0.594
Bo	9.9		10.1	0.390		0.398
Ko	4.15		4.35	0.163		0.171
Po	3.9		4.1	0.153		0.161
P	23.9		24.1	0.941		0.949
W	23.7		24.3	0.933		0.957

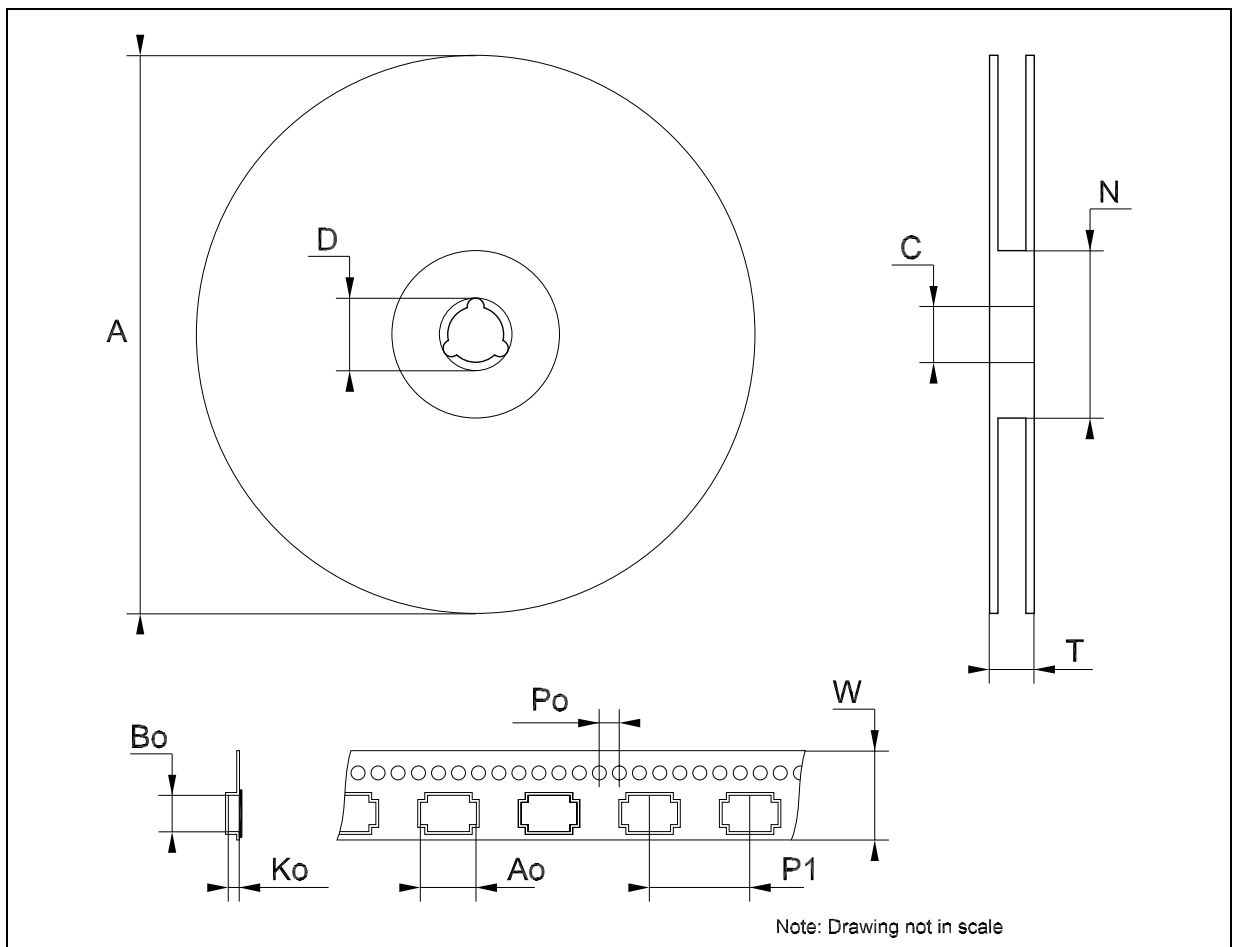


Table 7: Revision History

Date	Revision	Description of Changes
08-Jun-2004	7	Typing Error V_{O1} and V_{O2} on Table 6 - Page 6.
21-Dec-2004	8	Table 2 has been updated on GND row.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2004 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com