T-46-13-29

Am27C2048

2 Megabit (131,072 x 16-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  – 100 ns
- **Low power consumption**
  – 25 µA typical CMOS standby current
- **JEDEC-approved pinout**
  – plug in upgrade of 1 Megabit EPROM
  – 40-pin DIP/PDIP
  – 44-pin LCC/PLCC
- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  – typical programming time of 15 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  – both CMOS and TTL input/output compatibility
  – two line control functions

GENERAL DESCRIPTION

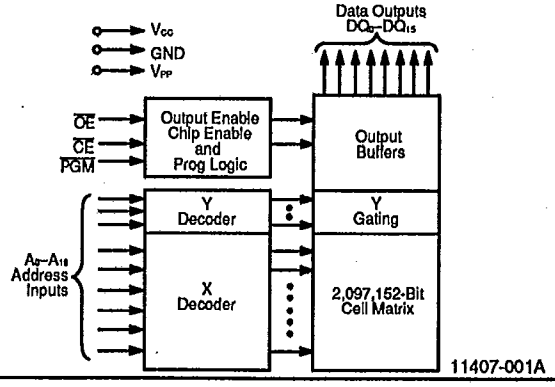
The Am27C2048 is a 2 megabit, ultraviolet erasable programmable read-only memory. It is organized as 128K words by 16 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. The Am27C2048 is ideal for use in 16-bit microprocessor systems. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C2048 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 125 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C2048 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming times of 15 seconds.

BLOCK DIAGRAM



11407-001A

PRODUCT SELECTOR GUIDE

Family Part No.	Am27C2048				
Ordering Part No: ±5% Vcc Tolerance	-105	-125			-255
±10% Vcc Tolerance		-120	-150	-200	-250
Max. Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	50	65	75	100

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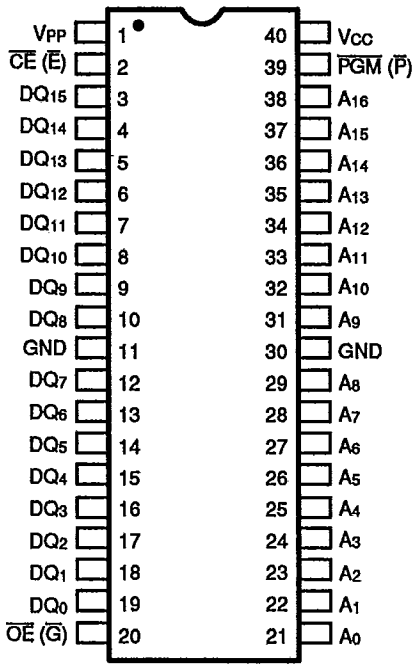
Issue Date: March 1991

CONNECTION DIAGRAMS
(Top View)

T-46-13-29

DIPs



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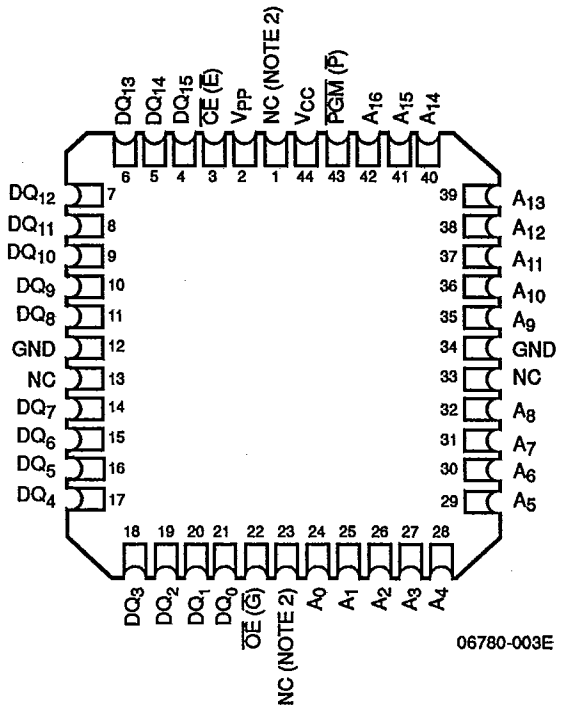
LCC*



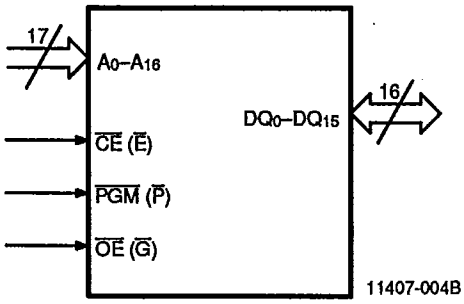
06780-003E

Notes:

1. JEDEC nomenclature is in parenthesis.
2. Don't use (DU) for PLCC.

*Also available in a 44-Pin Plastic Leaded Chip Carrier.

LOGIC SYMBOL



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PIN DESCRIPTION

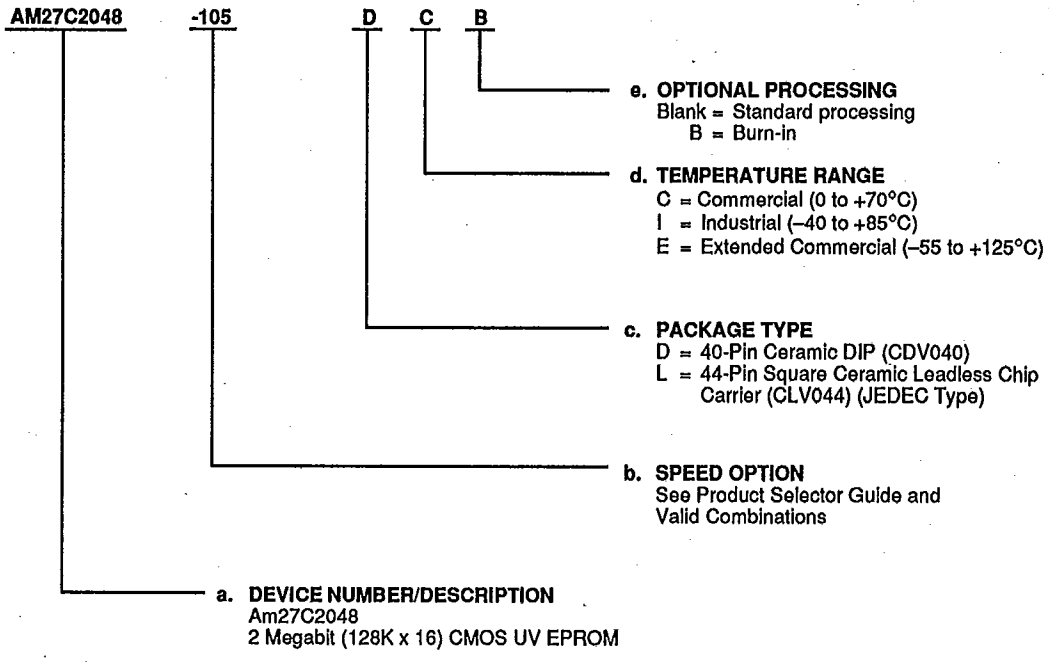
$A_0 - A_{16}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_{15}$	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connect
DU	=	No External Connect

ORDERING INFORMATION
EPROM Products

T-46-13-29

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27C2048-105	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C2048-120	
AM27C2048-125	
AM27C2048-150	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C2048-200	
AM27C2048-255	

Valid Combinations

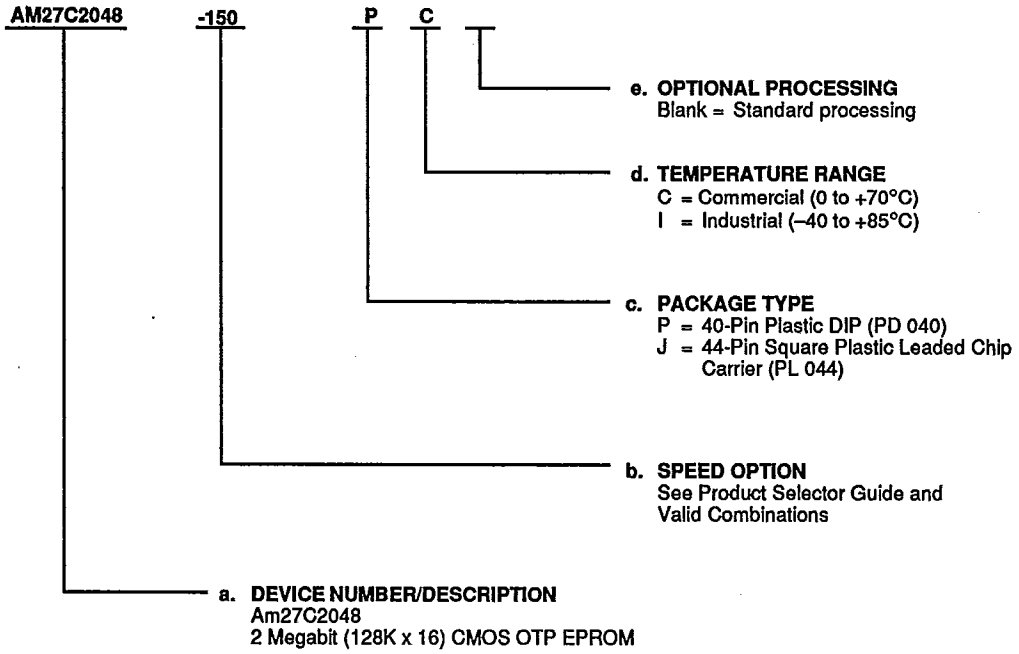
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products

T-46-13-29

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27C2048-125	PC, JC, PI, JI
AM27C2048-150	
AM27C2048-155	
AM27C2048-200	
AM27C2048-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

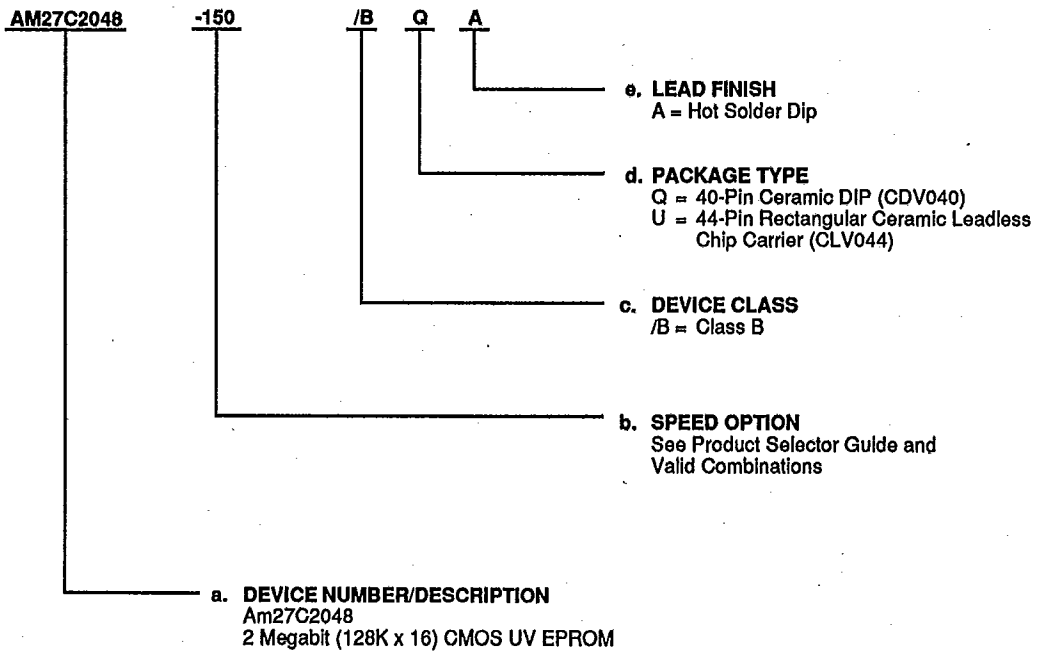
MILITARY ORDERING INFORMATION

T-46-13-29

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27C2048-150	/BQA, /BUA
AM27C2048-200	
AM27C2048-250	

For other Surface Mount Package options, contact NVD Military Marketing.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

T-46-13-29

Erasing the Am27C2048

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C2048 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C2048. This dosage can be obtained by exposure to an ultraviolet lamp —wavelength of 2537 Angstroms (Å) —with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C2048 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C2048, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C2048 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C2048

Upon delivery, or after each erasure, the Am27C2048 has all 2,097,152 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C2048 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, and $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}.

For programming, the data to be programmed is applied 16 bits in parallel to the data pins.

The flowchart (Figure 2) shows AMD's Flashrite algorithm. The Flashrite algorithm reduces programming time by using 100 µs programming pulse and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C2048. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP}$ = 5.25 V.

Program Inhibit

Programming of multiple Am27C2048s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C2048 may be common. A TTL low-level program pulse applied to an Am27C2048 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V and $\overline{PGM}$ LOW will program that Am27C2048. A high-level $\overline{CE}$ input inhibits the other Am27C2048 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$, at V_{IL}, PGM at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C2048.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C2048. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and Byte 1 ($A_0 = V_{IH}$), the device identifier code. For the Am27C2048, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C2048 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C2048 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C2048 also has a TTL-standby mode which reduce the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the outut pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

T-46-13-29

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	X	High Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	98H

Notes:

1. X can be either V_{IL} or V_{IH}
2. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
3. $A_1 - A_8 = A_{10} - A_{16} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	−65 to +125°C
All Other Products	−65 to +150°C
Ambient Temperature with Power Applied	−55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	−0.6 to V_{CC} +0.6 V
A_9 and V_{PP} (Note 2)	−0.6 to 13.5 V
V_{CC}	−0.6 to 7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Notes:

1. During transitions, the input may overshoot GND to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to −2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

T-46-13-29

Commercial (C) Devices	
Case Temperature (Tc)	0 to +70°C
Industrial (I) Devices	
Case Temperature (Tc)	−40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (Tc)	−55 to +125°C
Military (M) Devices	
Case Temperature (Tc)	−55 to +125°C
Supply Read Voltages:	
V_{CC} for Am27C2048-XX5	+4.75 to +5.25 V
V_{CC} for Am27C2048-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 4, 5 & 8) (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

T-46-13-29

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
TTL and NMOS						
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Notes 5 & 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH},	C/I Devices		1.0	mA
			E/M Devices		1.0	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA
CMOS						
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		V_{CC} – 0.8		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			0.7 V_{CC}	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Notes 5 & 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		150	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

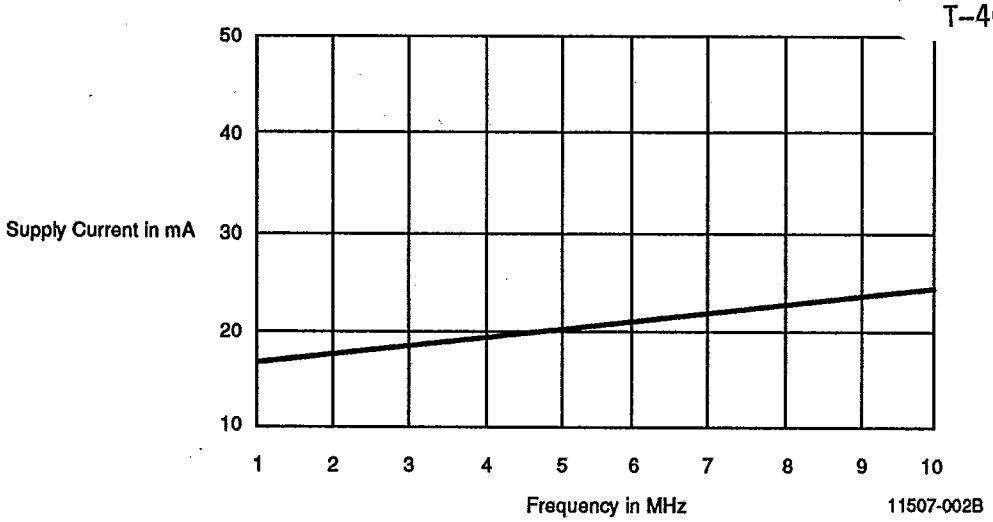


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.0 V, T = 25°C

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV044		CLV044		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27C2048 must not be removed from, or inserted into, a socket or board when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. Minimum DC input voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
9. For typical supply current values at various frequencies, refer to Figure 1.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

T-46-13-29

PRELIMINARY

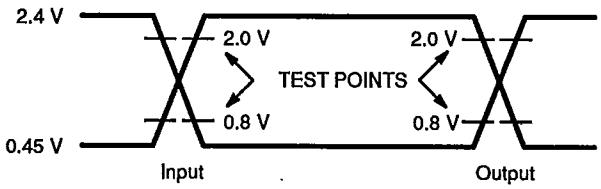
Parameter Symbols		Parameter Description	Test Conditions		Am27C2048					
JEDEC	Standard				-105	-120, -125	-150	-200	-250, -255	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.						ns
				Max.	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.						ns
				Max.	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.						ns
				Max.	50	50	65	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.	0	0	0	0	0	ns
				Max.	40	40	50	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	ns
				Max.						

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27C2048 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF,
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.45 to 2.4 V,
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V,
   Outputs: 0.8 V and 2 V.

SWITCHING TEST WAVEFORM

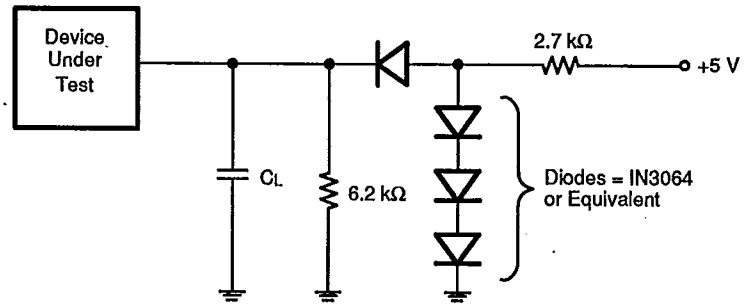
T-46-13-29



10205-009A

AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

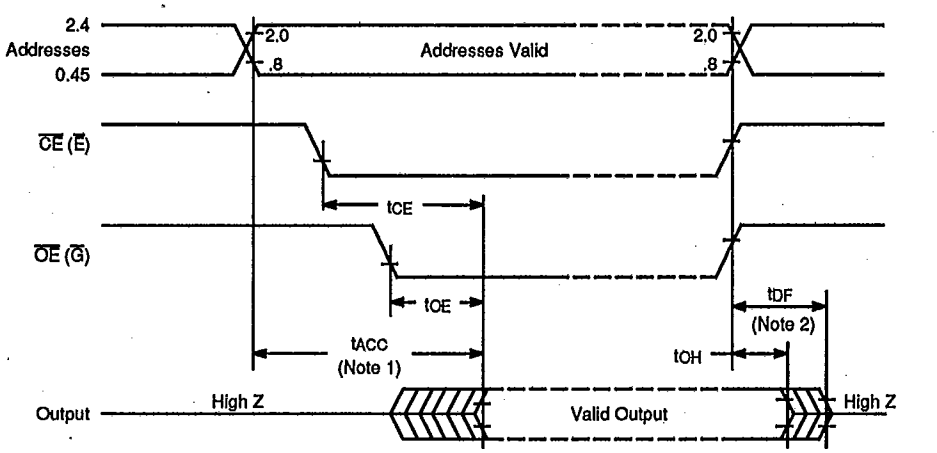
KEY TO SWITCHING WAVEFORMS

T-46-13-29

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORM



10205-005A

Notes:

1. $\overline{OE}$ ($\overline{G}$) may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING FLOW CHART

T-46-13-29

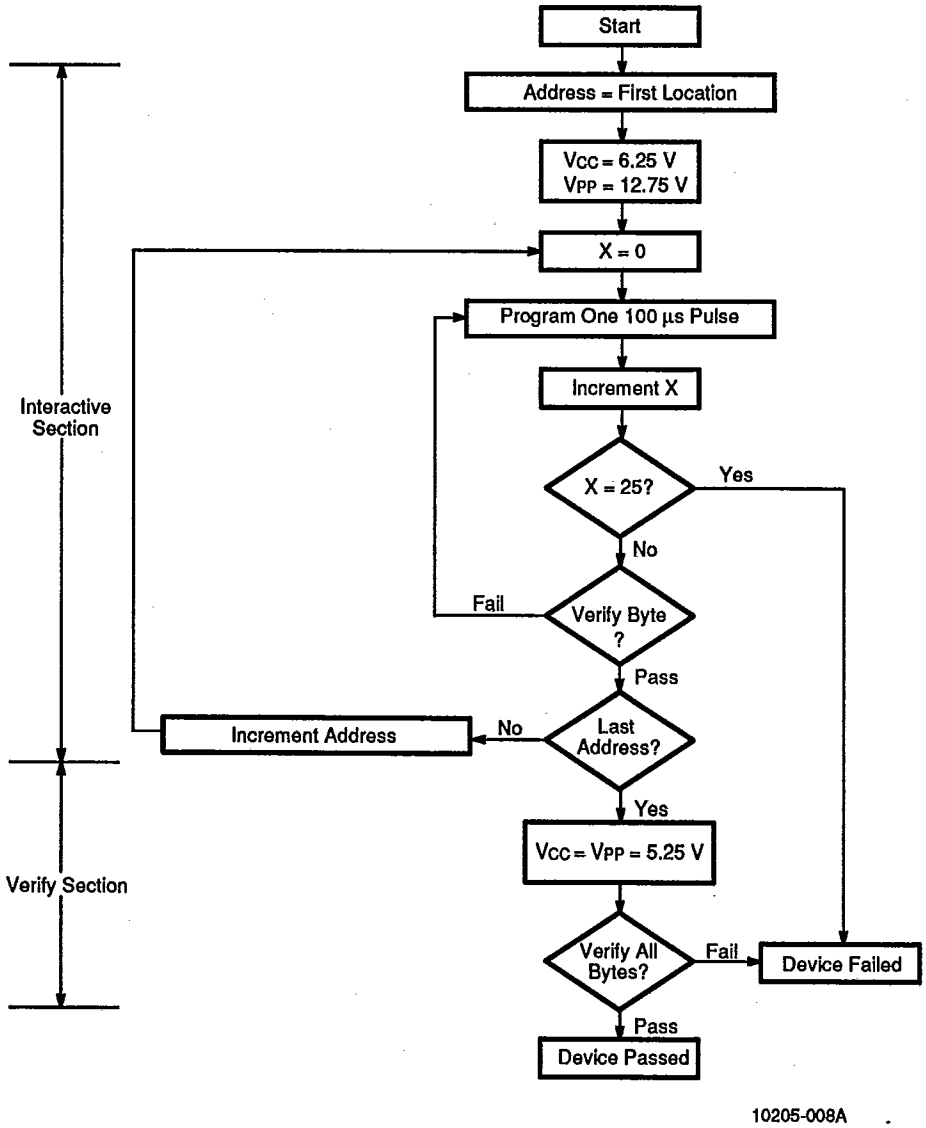


Figure 2. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

PRELIMINARY

T-46-13-29

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input LOW Level (All Inputs)		−0.5	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = −400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

PRELIMINARY

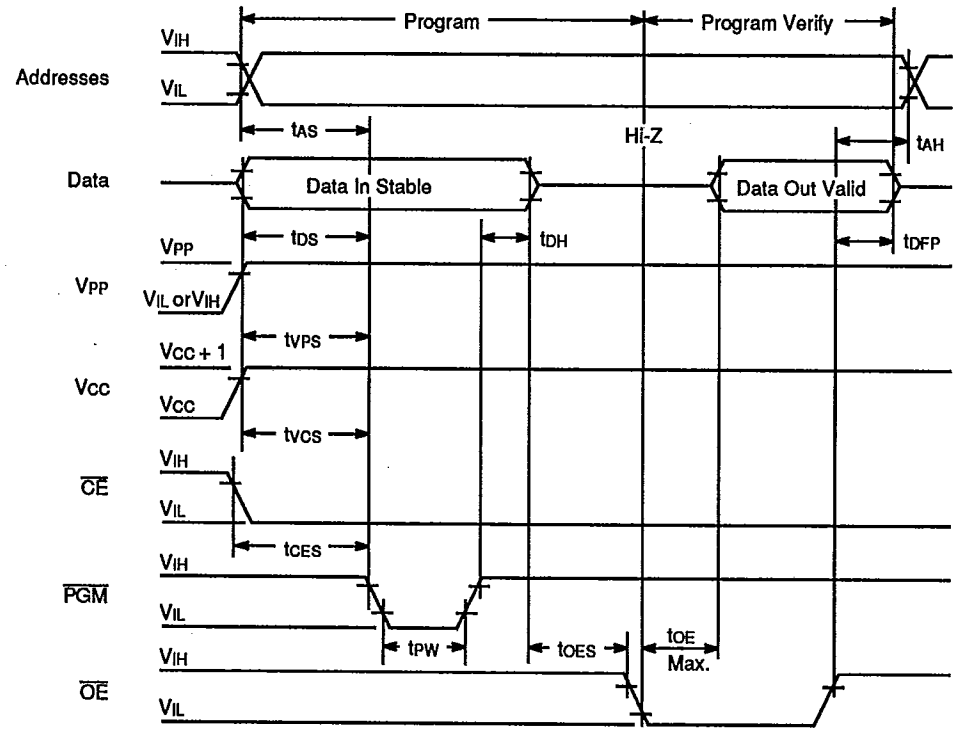
Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C2048, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 & 2)

T-46-13-29



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Notes:

1. The input timing reference level is 0.8 for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.