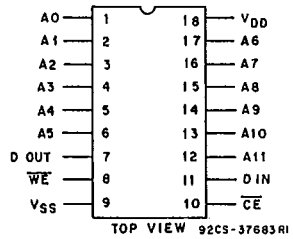
T-46-23-05

CMM5104/3
CMM5104/3Z



TERMINAL ASSIGNMENT
18-Lead Dual-In-Line Ceramic Package

High-Reliability, Radiation-Hardened CMOS/SOS 4096-Word by 1-Bit LSI Static RAM

Radiation Features:

- *Manufactured on 100K rads (S_i) production line*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec, 20-ns pulse*

Features:

- *Fully static operation*
- *Single power supply: 4.5 V to 6.5 V*
- *All inputs and outputs TTL compatible*
- *3-state outputs*
- *Industry-standard 18-pin configuration*
- *Fast access time: t_{AVQV} = 200 ns*
- *Low standby and operating power*

Package Specifications

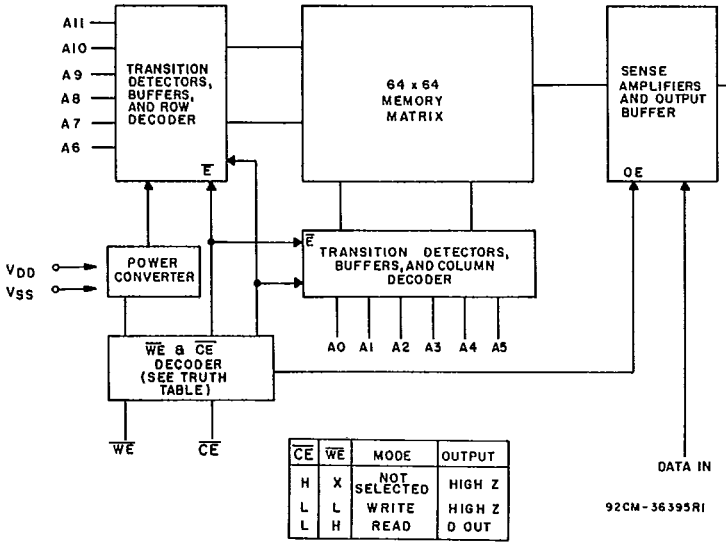
See Section 11, Fig. 3, b1

The RCA-CMM5104/3 and CMM5104/3Z are high-reliability 4096-word by 1-bit static random-access memories using CMOS/SOS technology. These devices are designed for use in memory systems where low power and simplicity in use are desirable.

CMOS/SOS technology permits operation in high-radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistant to single-event upset caused by cosmic rays or heavy ions.

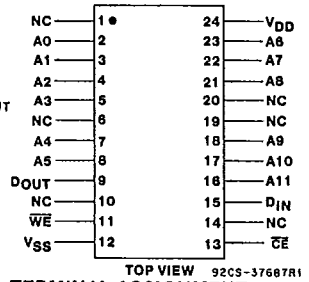
TTL compatibility on all input and output terminals permits easy system integration. The data-out signal has the same polarity as the input data. A separate data input and a separate tri-state output are used.

The CMM5104/3 and CMM5104/3Z are supplied in a 18-lead dual-in-line side-brazed ceramic package (D suffix). The parts are also available in a 24-lead flat-pack ceramic package (K suffix), and in a 24-terminal leadless ceramic chip package (J suffix).



CE	WE	MODE	OUTPUT
H	X	NOT SELECTED	HIGH Z
L	L	WRITE	HIGH Z
L	H	READ	D OUT

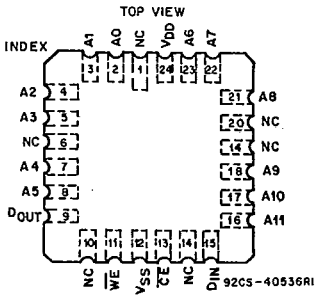
Fig. 1 - Functional block diagram.



TERMINAL ASSIGNMENT
24-Lead Flat-Pack Package

Package Specifications

See Section 11, Fig. 25



TERMINAL ASSIGNMENT
24-Terminal Leadless Chip-Carrier Package

Package Specifications

See Section 11, Fig. 34, c1

T-46-23-05

CMM5104/3
CMM5104/3Z

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING FOR D AND K PACKAGE TYPES):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	6.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%, V_{IN} = 0 V or V_{DD}, Except as Noted

CHARACTERISTIC		TEST CONDITIONS	LIMITS						UNITS
			+25°C		-55°C/+125°C		POST RADIATION‡ +25°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	—	—	0.1•	—	1•	—	1•	mA
Operating Device Current	I_{OPR}*	—	—	4.5	—	4.5	—	4.5	
Operating Device Current (Deselected)	I_{OPRD}	—	—	0.1	—	1	—	1	
Output Low Drive (Sink) Current	I_{DN}	V_{OUT}=0.4 V	4•	—	2.5•	—	2.5•	—	
Output High Drive (Source) Current	I_{DP}	V_{OUT}= V_{DD}-0.4 V	3•	—	2•	—	2•	—	
Output Voltage Low Level	V_{OL}	—	—	0.1	—	0.1	—	0.1	V
Output Voltage High Level	V_{OH}	—	V_{DD}-0.1	—	V_{DD}-0.1	—	V_{DD}-0.1	—	
Input Low Voltage△	V_{IL}	—	—	0.8•	—	0.8•	—	0.8•	
Input High Voltage△	V_{IH}	—	$V_{DD}/2$•	—	$V_{DD}/2$•	—	$V_{DD}/2$•	—	
Input Leakage Current	I_{IN}	—	—	±2•	—	±10•	—	±10•	μA
3-State Output Leakage Current	I_{OZ}	—	—	±5•	—	±30•	—	±30•	
Input Capacitance§	C_{IN}	—	—	5	—	5	—	5	pF
Output Capacitance§	C_{OUT}	—	—	7	—	7	—	7	

‡Radiation measuremments are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100K rads (Si).
•Limit with black dot (•) designates actual measurement, all other limits are inherent design characteristics.
*Operating current measured using 1-MHz cycle and C_L = 50 pF.
△Measured using 1-MHz cycle.
§Capacitance measurements are made with no bias applied.

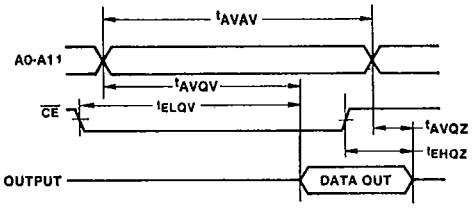
T-46-23-05

CMM5104/3
CMM5104/3Z

DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%, C_L = 50 pF

CHARACTERISTIC		LIMITS						UNITS
		+25°C		-55°C/+125°C		POST RADIATION‡ +25°C		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read-Cycle Times (Fig. 2)								
Read Cycle	t_{AVAV}	200	—	250	—	250	—	ns
Access From Address	t_{AVQV}	—	200•	—	250•	—	250•	ns
Access From $\overline{CE}$	t_{ELQV}	—	220•	—	280•	—	280•	ns
Output Hold From Address	t_{AVQZ}	—	80	—	100	—	100	ns
Output Hold From $\overline{CE}$	t_{EHQZ}	—	80	—	100	—	100	ns

‡Radiation measurements are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100K rads (Si).
•Limit with black dot (•) designates actual measurement, all other limits are inherent design characteristics.



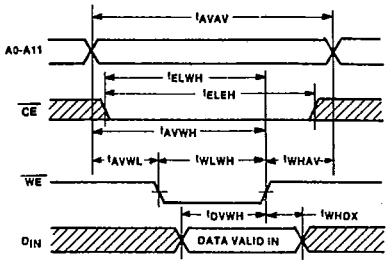
TIMING MEASUREMENT IS REFERENCED TO $V_{DD}/2$. 92CS-37682R2

Fig. 2 - Read-cycle timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%, C_L = 50 pF

CHARACTERISTIC		LIMITS						UNITS
		+25°C		-55°C/+125°C		POST RADIATION‡ +25°C		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write-Cycle Times (Fig. 3)								
Write Cycle	t_{AVAV}	200•	—	250•	—	250•	—	ns
Write Pulse Width	t_{WLWH}*	125•	—	145•	—	145•	—	ns
Address Set-up to Beginning of Write	t_{AVWL}	0•	—	0•	—	0•	—	ns
Address Set-up to End of Write	t_{AVWH}	160•	—	205•	—	205•	—	ns
Address Hold Time	t_{WHAV}	40•	—	45•	—	45•	—	ns
$\overline{CE}$ to Write Set-up Time	t_{ELWH}	160•	—	205•	—	205•	—	ns
$\overline{CE}$ Pulse Width	t_{ELEH}*	180•	—	220•	—	220•	—	ns
Data to Write Set-up Time	t_{DVWH}	100•	—	120•	—	120•	—	ns
Data Hold From Write	t_{WHDX}	5•	—	10•	—	10•	—	ns

‡Radiation measurements are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100K rads (Si).
•Limit with black dot (•) designates actual measurement, all other limits are inherent design characteristics.
*$\overline{CE}$ and $\overline{WE}$ must overlap for at least t_{WLWH} min. value, t_{DVWH} min. value must occur during this overlap.



TIMING MEASUREMENT IS REFERENCED TO $V_{DD}/2$. 92CS-37690R1

* $\overline{CE}$ AND $\overline{WE}$ MUST OVERLAP FOR AT LEAST t_{WLWH} MIN. VALUE, t_{DVWH} MIN. VALUE MUST OCCUR DURING THIS OVERLAP.

Fig. 3 - Write-cycle timing waveforms.

1901 C-06

CMM5104/3
CMM5104/3Z

T-46-23-05

DATA RETENTION CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS						UNITS
			+25°C		-55°C/+125°C		POST RADIATION‡ +25°C		
See Fig. 4		V_{DD} (V)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Minimum Data Retention Voltage	V_{DR}	—	—	2•	—	2.5•	—	2.5•	V
Data Retention Quiescent Current	$I_{DD}DR$	—	—	40•	—	400•	—	400•	μA
V_{DD} to V_{DR} Rise and Fall Time	t_r, t_f	5	1	—	1	—	1	—	μs

‡Radiation measurements are made on 2 samples/wafers. The limits shown are for within 1 hour of radiating to 100K rads (Si).
•Limit with black dot (•) designates actual measurement, all other limits are inherent design characteristics.

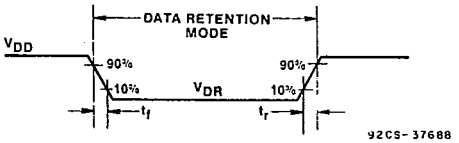


Fig. 4 - Low V_{DD} data retention timing waveforms.

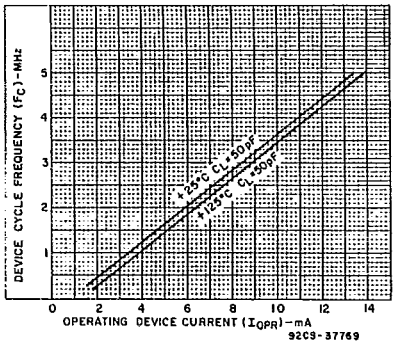


Fig. 5 - Typical operating device-current (selected) as a function of cycle frequency.

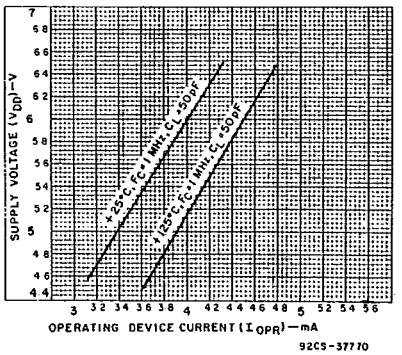


Fig. 6 - Typical operating device-current (selected) as a function of supply voltage.

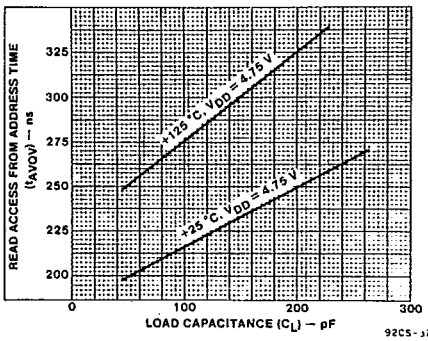


Fig. 7 - Read access from address time (t_{AVQV}) as a function of load capacitance. (Time measurements made at 50% V_{DD} point.).

CMM5104/3
CMM5104/3Z

/3Z SCREENING FLOW

Radiation Verification	Method 1019 - 100K rads (Si) Total Dose 2 samples/wafer, 0 rejects (/3Z Screening continues below)

/3 SCREENING FLOW (Without Radiation Verification)

Internal Visual (100%)	Method 2010 - Condition B (Modified) - See Note 1
Pre-Seal Bake (100%)	—
Stabilization Bake (100%)	Method 1008 - Condition C 24 hrs., 25°C No End-Point Measurements Required
Temperature Cycling (100%)	Method 1010 - Condition C
Constant Acceleration (100%)	Method 2001 - Condition E_1, Y_1 Direction, Centrifuge
Seal:	
Fine (100%)	Method 1014 - Condition A or B
Gross (100%)	Method 1014 - Condition C
Initial Electrical Tests (100%)	Per Applicable Device Specification, 25°C
High-Temperature Stress (100%)	48 hrs, 125°C, See Table II
Interim Electrical Tests I (100%)	Per Applicable Device Specifications, 25°C PDA 10% all tests. See Table I.
Static Burn-In (100%)	160 hrs, 125°C, See Table II
Interim Electrical Tests II (100%)	Per Applicable Device Specifications, 25°C PDA 5% all tests, PDA 3% Functional, See Table I
Final Electrical Tests (100%)	Per Applicable Device Specifications, 25°C
External Visual (100%)	Method 2009
Quality Conformance	
Group A (All Tests)	Method 5005 (Class B), See Table I
Group B (Optional)	Method 5005 (Class B), See Table I
Group C (Optional)	Method 5005 (Class B), See Table I
Group D (Optional)	Method 5005 (Class B), See Table I

TABLE I - ELECTRICAL TESTS

Post Radiation	See STATIC and DYNAMIC Characteristics (Post Radiation, 25°C)
Initial Electrical Tests	Same as above (25°C)
Interim Electrical Tests I	Same as above (25°C)
Interim Electrical Tests II	Same as above (25°C)
Final Electrical Tests	Same as above (-55°C, 25°C, 125°C)
Quality Conformance:	
Group A	Same as above (-55°C, 25°C, 125°C)
Group B	Same as above (25°C)
Group D	Same as above (25°C)

TABLE II - BURN-IN AND LIFE-TEST CIRCUITS AND TIMING WAVEFORMS

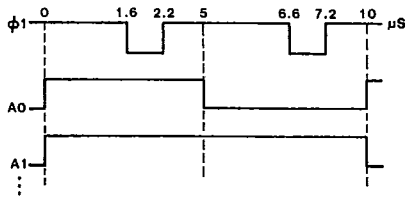
TEST	TEMPERATURE	DURATION	V_{DD}
Stress	125°C	48 hrs.	7 V
Static	125°C	160 hrs.	7 V
Life Test	125°C	1000 hrs.	5.5 V Min.

ALL INPUTS ARE CONNECTED THROUGH A 1 TO 6-KΩ RESISTOR TO THE FOLLOWING:

Test Package	STRESS[c]			STATIC[c]			LIFE TEST[a]		
	D	J	K	D	J	K	D	J	K
Pin No.									
1	V_{SS}	—	—	V_{SS}	—	—	A_0	—	—
2	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_1	A_0	A_0
3	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_2	A_1	A_1
4	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_3	A_2	A_2
5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_4	A_3	A_3
6	V_{SS}	—	—	V_{SS}	—	—	A_5	—	—
7	—	V_{SS}	V_{SS}	—	V_{SS}	V_{SS}	—	A_4	A_4
8	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	ϕ_1	A_5	A_5
9	V_{SS}	—	—	V_{SS}	—	—	V_{SS}	—	—
10	V_{SS}	—	—	V_{SS}	—	—	A_{13}	—	—
11	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_{12}	ϕ_1	ϕ_1
12	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_{11}	V_{SS}	V_{SS}
13	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_{10}	A_{13}	A_{13}
14	V_{SS}	—	—	V_{SS}	—	—	A_9	—	—
15	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_8	A_{12}	A_{12}
16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_7	A_{11}	A_{11}
17	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_6	A_{10}	A_{10}
18	V_{DD}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	V_{SS}	V_{DD}	A_9	A_9
19	—	—	—	—	—	—	—	—	—
20	—	—	—	—	—	—	—	—	—
21	—	V_{SS}	V_{SS}	—	V_{SS}	V_{SS}	—	A_8	A_8
22	—	V_{SS}	V_{SS}	—	V_{SS}	V_{SS}	—	A_7	A_7
23	—	V_{SS}	V_{SS}	—	V_{SS}	V_{SS}	—	A_6	A_6
24	—	V_{DD}	V_{DD}	—	V_{DD}	V_{DD}	—	V_{DD}	V_{DD}

[a]The following timing waveforms are used for the Dynamic and Life Tests.
[c]Memory array is pre-initialized with all 0's.
NOTE:
Pin 7 on D-type package, and Pin 9 on J and K packages are the outputs connected to $V_{DD}/2$ in High Z state.
— indicates no connection.
ϕ_1 is connected to WE on all packages (D, J, and K).
A_{13} is connected to CE on all packages (D, J, and K).

9



A1 TO A13 ARE SUCCESSIVE DIVISIONS BY 2 BASED ON A0

92CS-37686

Fig. 8 - Burn-in circuit timing waveforms.

CMM5104/3
CMM5104/3Z

NOTES:

1. Internal Visual Inspection Modified for LSI
Internal Visual Inspection is performed to MIL-STD-883, Method 2010, Condition B **except** as follows:

A. **High magnification inspection** is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required.

B. **Metallization Voids** (3.2.1.2) Criteria 3.2.1.1a Metallization Scratches and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed.

C. **Metallization Alignment** (3.2.1.7) Diffusion and Passivation Layer(s) Faults (3.2.0).

High magnification inspection is performed at 200X to 300X, applied to the center and two opposite corners of the chip, consisting only of the area exposed to the immediate field of view.

D. **Scribing and Die Defects** (3.2.3) in addition:

A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line to be unacceptable.

Semicircular cracks that point away from the active circuit area are acceptable.

2. SOS Technology Devices;

A. Diffusion faults are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.

B. The 1-mil wire clearance criteria is not applicable.

C. Passivation faults are not applicable because a second free flow oxide is used prior to metallization.

D. Oxide gate bridge inspection is not applicable.

E. Semicircular cracks not in an active area which start and end at the pellet edge are acceptable.