



Flash-ROM Module 4MByte (1Mx32Bit), 80Pin-SMM, 3.3V Design  
Part No. HMF1M32F2VA

## GENERAL DESCRIPTION

The HMF1M32F2VA is a high-speed flash read only memory (FROM) module containing 1,048,576 words organized in a x32bit configuration. The module consists of two 1M x 16 FROM mounted on a 80-pin stackable type, double - sided, FR4-printed circuit board.

Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Output enable (/OE) and write enable (/WE) can set the memory input and output. The host system can detect a program or erase operation is complete by observing the Ready Pin, or reading the DQ7(Data # Polling) and DQ6(Toggle) status bits. When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single + 3.0V DC power supply and all inputs and outputs are LVTTTL-compatible.

## FEATURES

### w Part Identification

- HMF1M32F2VA : Socket 5mm

### w Access time: 70, 80, 90, 120ns

### w High-density 4MByte design

### w High-reliability, low-power design

### w Single + 3.0V $\pm$ 0.5V power supply

### w All in/outputs are LVTTTL-compatible

### w FR4-PCB design

### w 80-pin Designed by

40-pin Fine Pitch Connector (x 2EA)

### w Minimum 1,000,000 write/erase cycle

### w Sector erases architecture

## OPTIONS MARKING

### w Timing

70ns access	-70
80ns access	-80
90ns access	-90
120ns access	-120

### w Packages

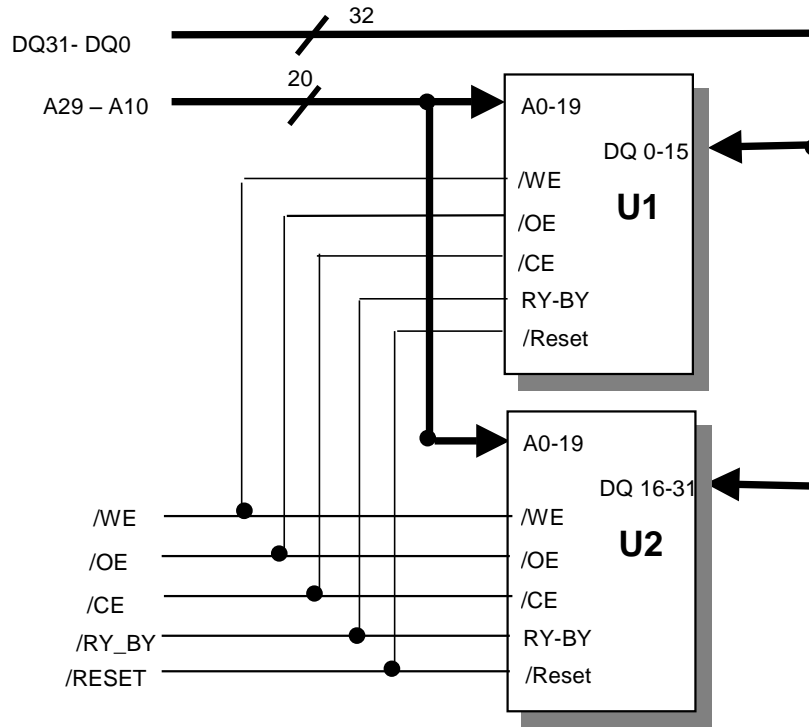
80-pin SMM	F
------------	---

## PIN ASSIGNMENT

P1				P2			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vcc	21	Vcc	1	Vcc	21	Vcc
2	NC	22	DQ16	2	DQ15	22	NC
3	NC	23	DQ24	3	DQ7	23	NC
4	NC	24	DQ17	4	DQ14	24	/BYTE
5	NC	25	DQ25	5	DQ6	25	/OE
6	/RY_BY	26	DQ18	6	DQ13	26	/CE
7	Vss	27	Vss	7	Vss	27	Vss
8	/RESET	28	DQ26	8	DQ5	28	A13
9	/WE	29	DQ19	9	DQ12	29	A29
10	A10	30	DQ27	10	DQ4	30	A11
11	A21	31	DQ20	11	DQ11	31	A12
12	A20	32	DQ28	12	DQ3	32	A22
13	A19	33	DQ21	13	DQ10	33	A23
14	Vss	34	Vss	14	Vss	34	Vss
15	A18	35	DQ29	15	DQ2	35	A24
16	A17	36	DQ22	16	DQ9	36	A25
17	A16	37	DQ30	17	DQ1	37	A26
18	A15	38	DQ23	18	DQ8	38	A27
19	A14	39	DQ31	19	DQ0	39	A28
20	Vcc	40	Vcc	20	Vcc	40	Vcc

4 cf : Address & Data Bus is organized for LG Specification.  
( A10 & DQ0 are MSB, A29 & DQ31 are LSB )

FUNCTIONAL BLOCK DIAGRAM



4 cf : Address & Data Bus is organized for LG Specification Request.  
( A10 & DQ0 are MSB, A29 & DQ31 are LSB)

## TRUTH TABLE

MODE	/OE	/CE	/WE	/RESET	DQ ( /BYTE=L )	POWER
STANDBY	X	H	X	V <sub>CC</sub> ±0.3V	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
READ	L	L	H	H	D <sub>OUT</sub>	ACTIVE
WRITE or ERASE	X	L	L	H	D <sub>IN</sub>	ACTIVE

NOTE: X means don't care

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	V <sub>IN,OUT</sub>	-0.5V to V <sub>CC</sub> +0.5V
Voltage with respect to ground V <sub>CC</sub>	V <sub>CC</sub>	-0.5V to +4.0V
Storage Temperature	T <sub>STG</sub>	-65°C to +150°C
Operating Temperature	T <sub>A</sub>	-55°C to +125°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
V <sub>CC</sub> for ± 10% device Supply Voltages	V <sub>CC</sub>	2.7V		3.6V
Ground	V <sub>SS</sub>	0	0	0

DC AND OPERATING CHARACTERISTICS ( 0°C ≤ T<sub>A</sub> ≤ 70 °C )

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT	
Input Load Current	V <sub>CC</sub> =V <sub>CC</sub> max, V <sub>IN</sub> = GND to V <sub>CC</sub>	I <sub>L1</sub>		±1.0	μA	
Output Leakage Current	V <sub>CC</sub> =V <sub>CC</sub> max, V <sub>OUT</sub> = GND to V <sub>CC</sub>	I <sub>L0</sub>		±1.0	μA	
Output High Voltage	I <sub>OH</sub> = -2.0mA, V <sub>CC</sub> = V <sub>CC</sub> min	V <sub>OH</sub>	2.4		V	
Output Low Voltage	I <sub>OL</sub> = 4.0mA, V <sub>CC</sub> =V <sub>CC</sub> min	V <sub>OL</sub>		0.45	V	
V <sub>CC</sub> Active Read Current (1)	/CE = V <sub>IL</sub> , /OE = V <sub>IH</sub> ,	I <sub>CC1</sub>	5MHZ	18	32	mA
			1MHZ	4	8	
V <sub>CC</sub> Active Write Current (2)	/CE = V <sub>IL</sub> , /OE=V <sub>IH</sub>	I <sub>CC2</sub>	40	60	mA	
V <sub>CC</sub> Standby Current	/CE, /RESET=V <sub>CC</sub> ±0.3V	I <sub>CC3</sub>		60	mA	
Low V <sub>CC</sub> Lock-Out Voltage		V <sub>LKO</sub>	2.3	2.5	V	

- Notes:
1. The I<sub>CC</sub> current listed is typically less than 2mA/MHz, with /OE at V<sub>IH</sub>.
  2. I<sub>CC</sub> active while embedded algorithm (program or erase) is in progress
  3. Maximum I<sub>CC</sub> current specifications are tested with V<sub>CC</sub>=V<sub>CC</sub> max

## ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	0.7	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time		25		sec	
Byte Programming Time	-	9	300	μs	Excludes system-level overhead
Chip Programming Time	-	18	54	sec	

## TSOP CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0	6	7.5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0	8.5	12	pF
C <sub>IN2</sub>	Control Pin Capacitance	V <sub>IN</sub> = 0	7.5	9	pF

Notes : Test conditions T<sub>A</sub> = 25° C, f=1.0 MHz.

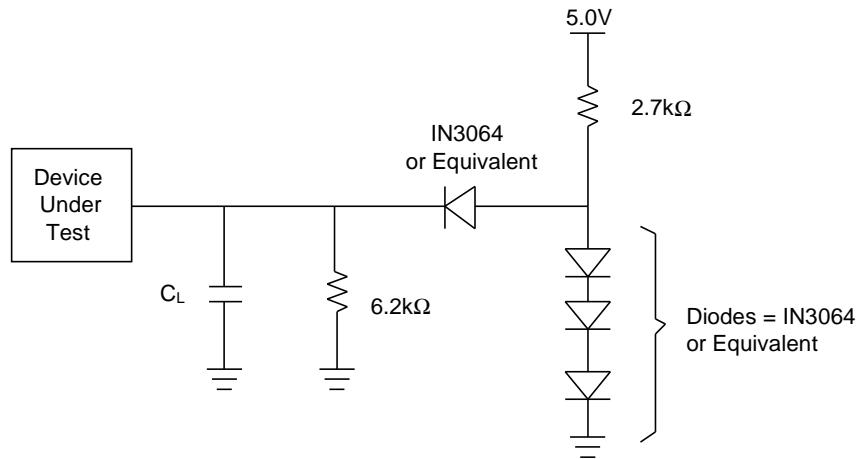
## TEST SPECIFICATIONS

TEST CONDITION	70R, 80	90, 120	UNIT
Output load	1TTL gate		
Output load capacitance, C <sub>L</sub> (Including jig capacitance)	30	100	pF
Input rise and full times	5		ns
Input pulse levels	0.0-3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

## AC CHARACTERISTICS

## u Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION	TEST SETUP	Speed Options				UNIT
JEDEC	STANDARD			-70R	-80	-90	-120	
t <sub>AVAV</sub>	t <sub>RC</sub>	Read Cycle Time	Min	70	80	90	120	ns
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address to Output Delay	/CE = V <sub>IL</sub> /OE = V <sub>IL</sub> Max	70	80	90	120	ns
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable to Output Delay	/OE = V <sub>IL</sub> Max	70	80	90	120	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Chip Enable to Output Delay	Max	30	30	35	35	ns
t <sub>EHQZ</sub>	t <sub>DF</sub>	Chip Enable to Output High-Z	Max	25	25	30	30	ns
t <sub>GHQZ</sub>	t <sub>DF</sub>	Output Enable to Output High-Z	Max	25	25	30	30	ns
t <sub>AXQX</sub>	t <sub>QH</sub>	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First	Min	0				ns



Note :  $C_L = 100\text{pF}$  including jig capacitance

### U Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION	Speed Options				UNIT	
JEDEC	STANDARD		70R	80	90	120		
$t_{AVAV}$	$t_{WC}$	Write Cycle Time	Min	70	80	90	12	ns
$t_{AVWL}$	$t_{AS}$	Address Setup Time	Min	0				ns
$t_{WLAX}$	$t_{AH}$	Address Hold Time	Min	45	45	45	50	ns
$t_{DVWH}$	$t_{DS}$	Data Setup Time	Min	35	35	45	50	ns
$t_{WHDX}$	$t_{DH}$	Data Hold Time	Min	0				ns
	$t_{OES}$	Output Enable Setup Time	Min	0				ns
$t_{GHWL}$	$t_{GHWL}$	Read Recover Time Before Write	Min	0				ns
$t_{ELWL}$	$t_{CS}$	/CE Setup Time	Min	0				ns
$t_{WHEH}$	$t_{CH}$	/CE Hold Time	Min	0				ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	Min	35	35	35	50	ns
$t_{WHWL}$	$t_{WPH}$	Write Pulse Width High	Min	30				ns
$t_{WHWH1}$	$t_{WHWH1}$	Byte Programming Operation	Typ	9				$\mu\text{s}$
$t_{WHWH2}$	$t_{WHWH2}$	Sector Erase Operation (Note1)	Typ	0.7				sec
	$t_{VCS}$	Vcc set up time	Min	50				$\mu\text{s}$

- Notes :
- 1 . This does not include the preprogramming time
  - 2 . This timing is only for Sector Protect operations

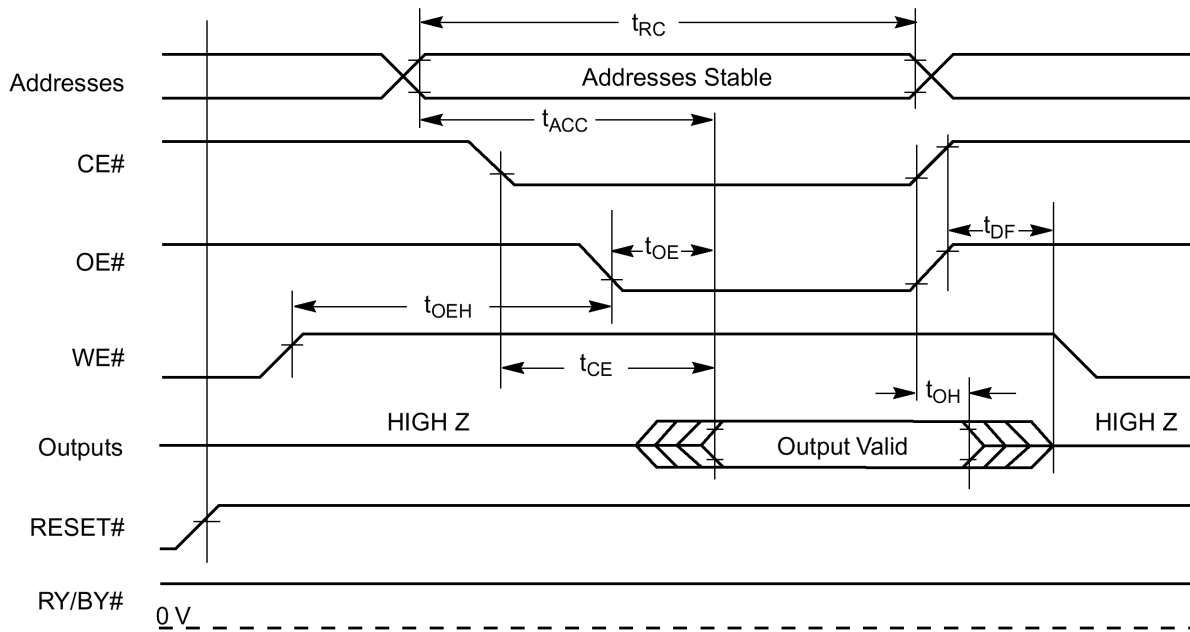
## ⌋ Erase/Program Operations

### Alternate /CE Controlled Writes

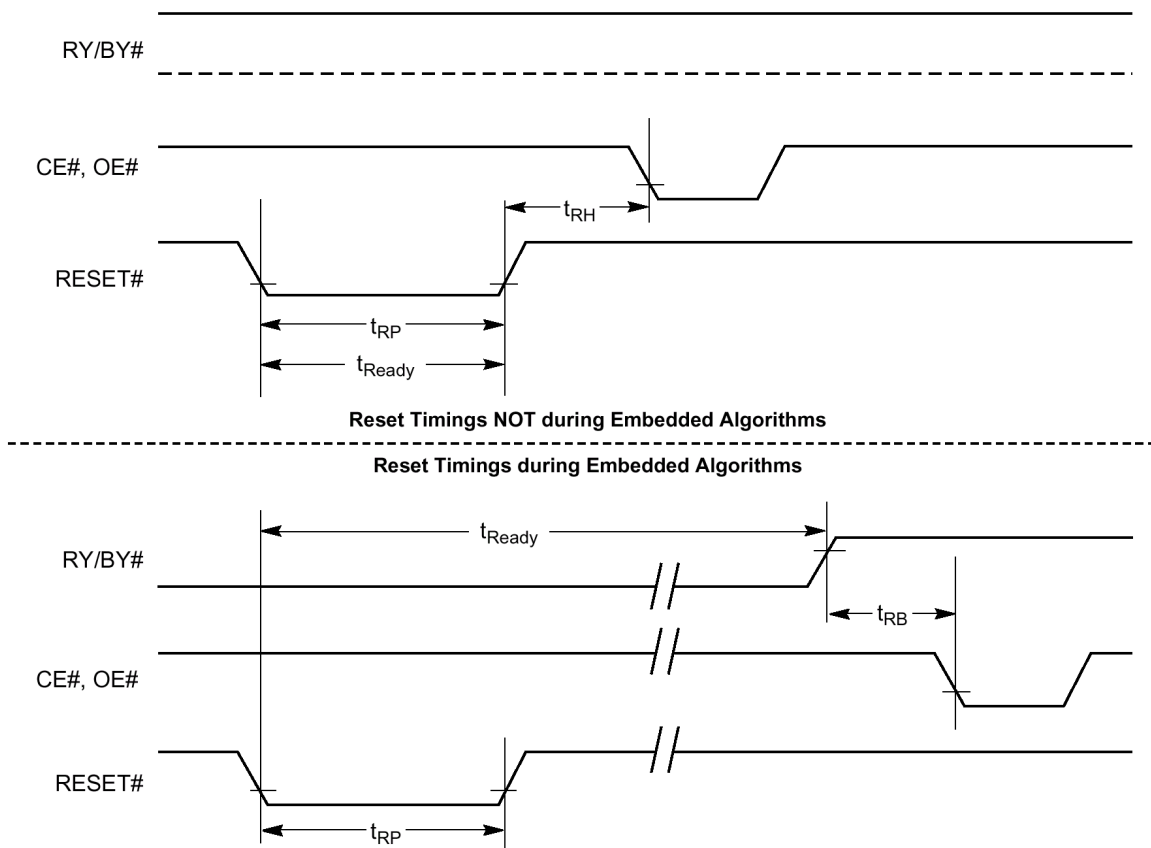
PARAMETER SYMBOLS		DESCRIPTION		Speed Options				UNIT
JEDEC	STANDARD			-70R	-80	-90	120	
t <sub>AVAV</sub>	t <sub>WC</sub>	Write Cycle Time	Min	70	80	90	12	ns
t <sub>AVWL</sub>	t <sub>AS</sub>	Address Setup Time	Min	0				ns
t <sub>WLAX</sub>	t <sub>AH</sub>	Address Hold Time	Min	45	45	45	50	ns
t <sub>DVWH</sub>	t <sub>DS</sub>	Data Setup Time	Min	35	35	45	50	ns
t <sub>WHDX</sub>	t <sub>DH</sub>	Data Hold Time	Min	0				ns
	t <sub>OES</sub>	Output Enable Setup Time	Min	0				ns
t <sub>GHWL</sub>	t <sub>GHWL</sub>	Read Recover Time Before Write	Min	0				ns
t <sub>ELWL</sub>	t <sub>CS</sub>	/CE Setup Time	Min	0				ns
t <sub>WHEH</sub>	t <sub>CH</sub>	/CE Hold Time	Min	0				ns
t <sub>WLWH</sub>	t <sub>WP</sub>	Write Pulse Width	Min	35	35	35	50	ns
t <sub>WHWL</sub>	t <sub>WPH</sub>	Write Pulse Width High	Min	30				ns
t <sub>WHWH1</sub>	t <sub>WHWH1</sub>	Byte Programming Operation	Typ	9				μs
t <sub>WHWH2</sub>	t <sub>WHWH2</sub>	Sector Erase Operation (Note1)	Typ	0.7				sec

- Notes :**
1. This does not include the preprogramming time
  2. This timing is only for Sector Protect operations

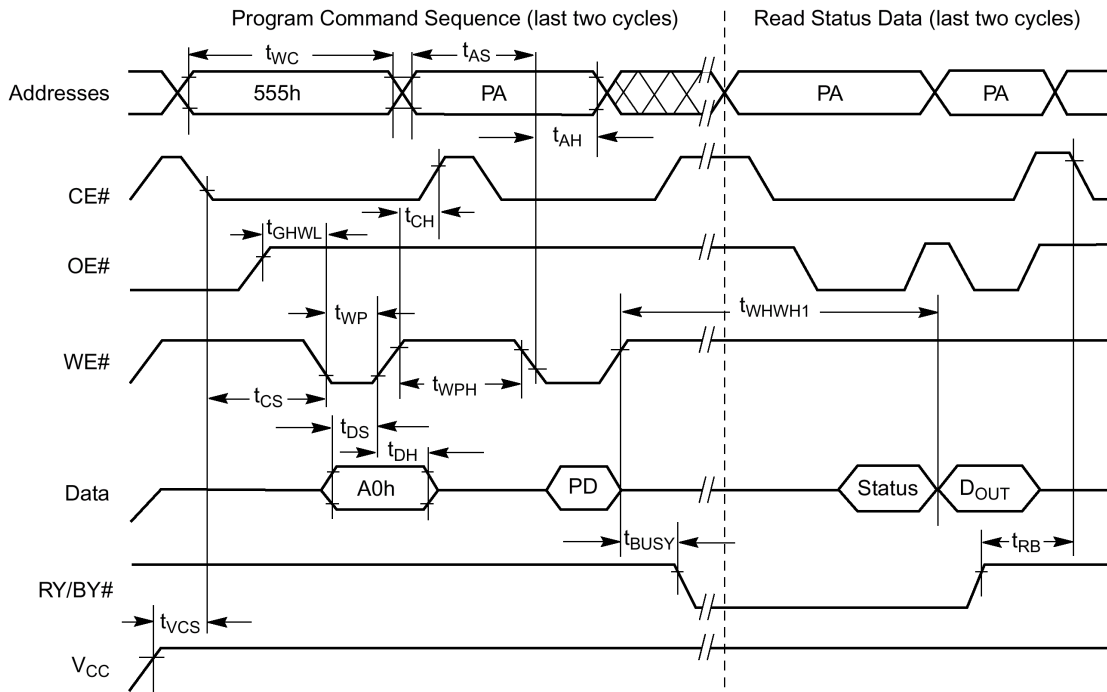
⌌ READ OPERATIONS TIMING



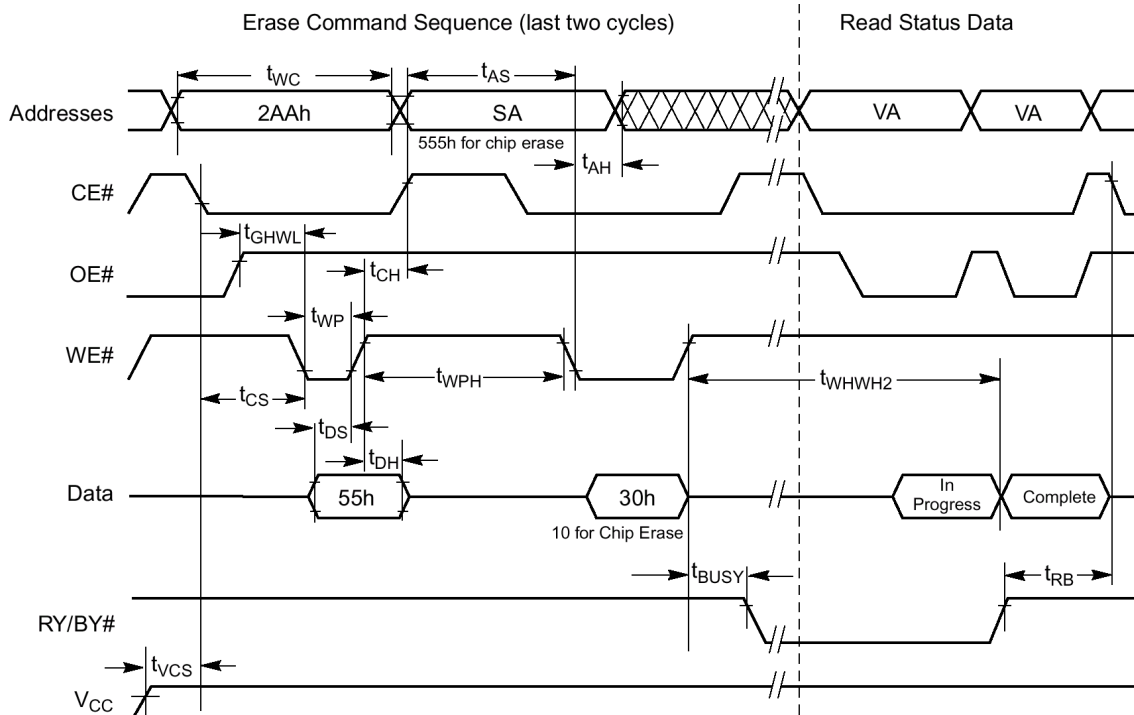
⌌ RESET TIMING



PROGRAM OPERATIONS TIMING

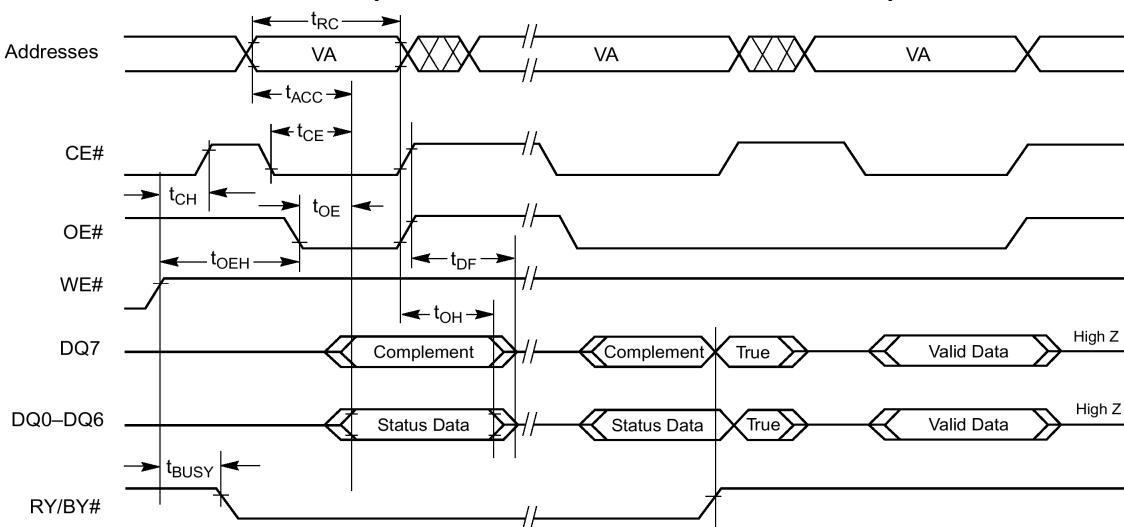


CHIP/SECTOR ERASE OPERATION TIMINGS

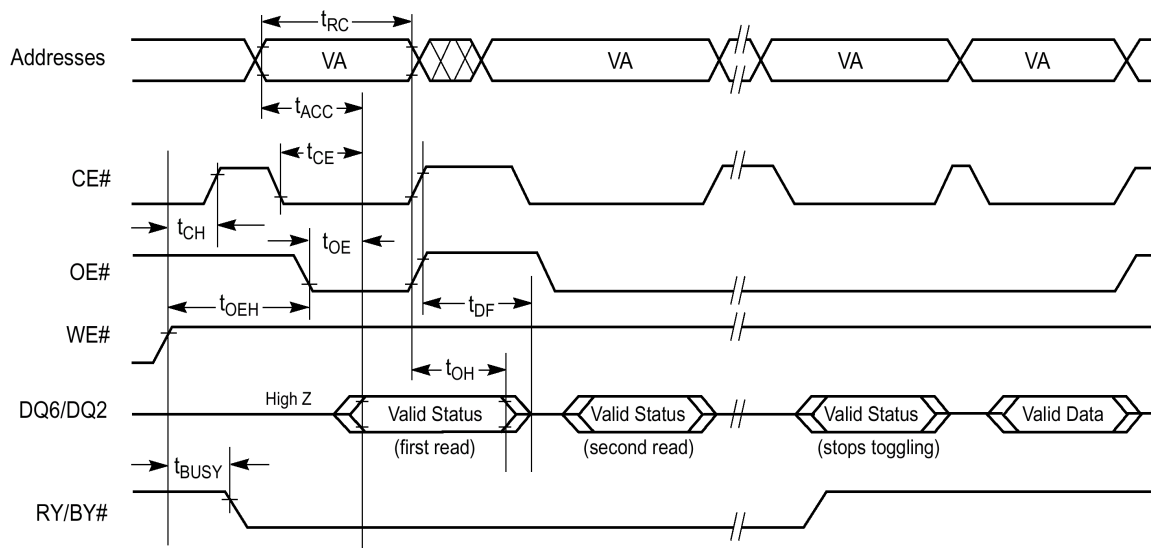




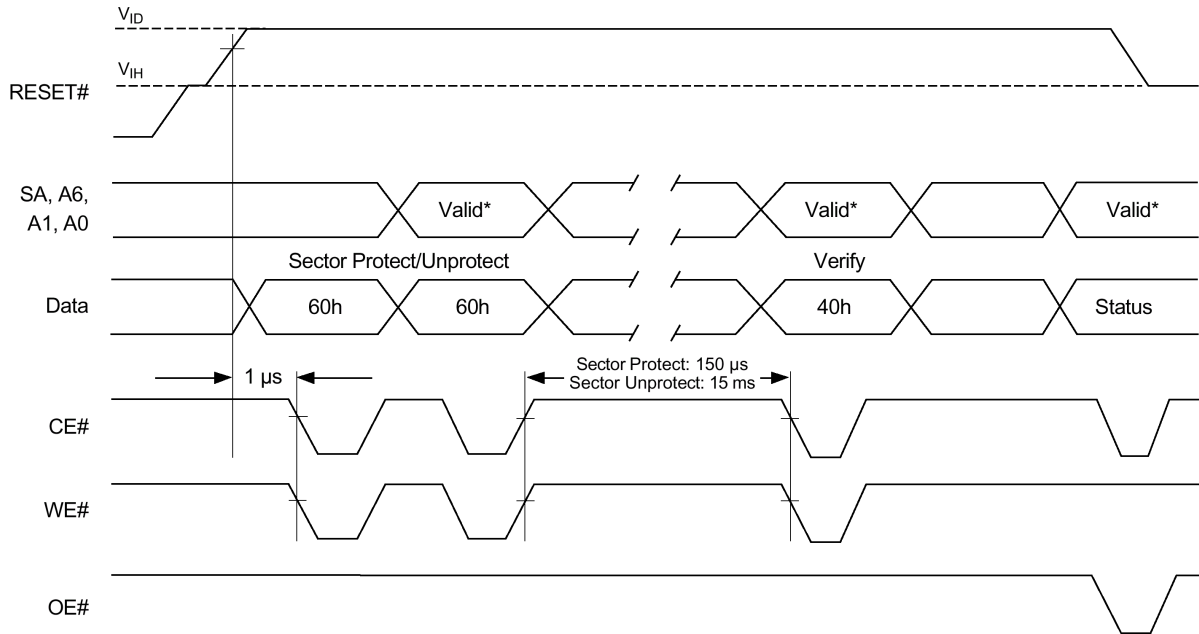
**U DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)**



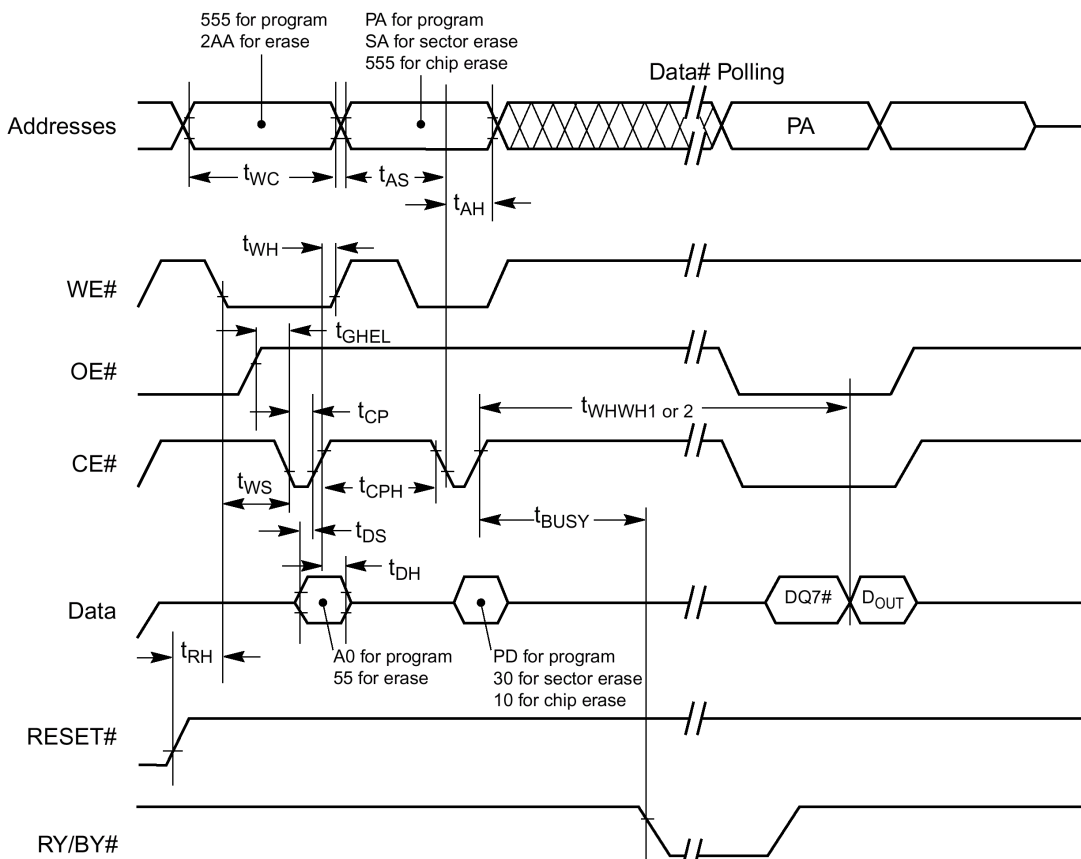
**U TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)**



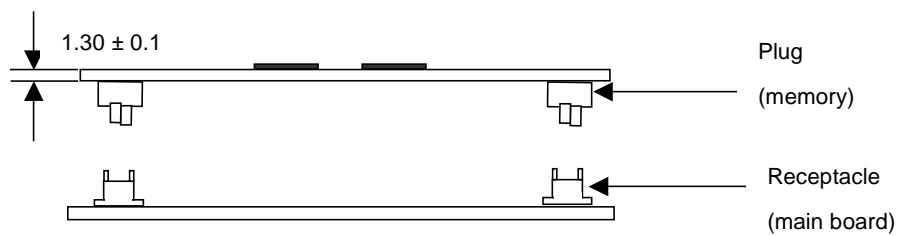
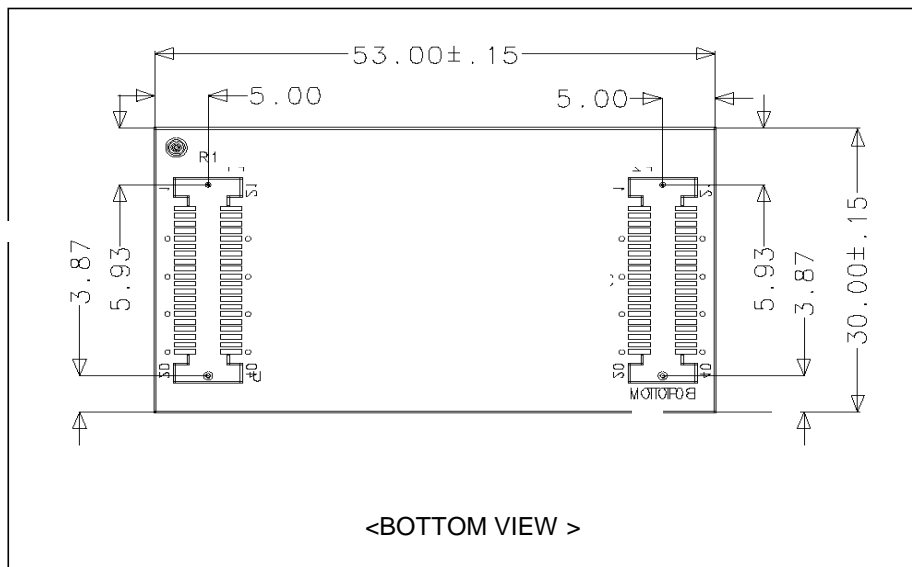
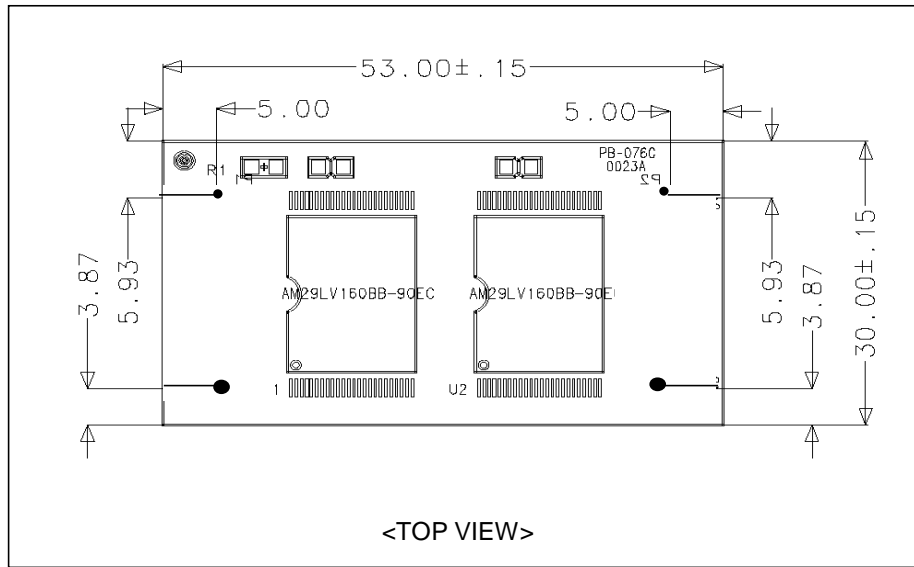
U SECTOR PROTECT UNPROTECT TIMEING DIAGRAM



U ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



PACKAGE DIMENSIONS



**ORDERING INFORMATION**

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
<b>HMF1M32F2VA-70</b>	4MByte	x 32	80Pin –SMM	2EA	3.3V	70ns
<b>HMF1M32F2VA-80</b>	4Mbyte	x 32	80Pin –SMM	2EA	3.3V	80ns
<b>HMF1M32F2VA-90</b>	4Mbyte	x 32	80Pin –SMM	2EA	3.3V	90ns
<b>HMF1M32F2VA-120</b>	4Mbyte	x 32	80Pin -SMM	2EA	3.3V	120ns