16 x 16 multiplier-accumulators

LMA2010/2043

general information

The LMA2010/2043 are high speed, low power CMOS multiplier-accumulators (MACs). The LMA2010/LMA2043 are pin and functionally compatible with the TRW TDC1010/1043 and AMD Am29510 in surface mount packages. The LOGIC Devices LMA1010/1043 offer compatible pinouts for DIP packages.

The LMA2010/2043 produce the 32-bit product of two 16-bit numbers. The results of a series of multiplications may be accumulated to form a sum of products. Accumulation is performed to 35-bit precision with the multiplier product sign extended as appropriate.

Data present at the A and B input registers is latched in on the rising edges of CLK A and CLK B respectively, RND, TC, ACC, and SUB controls are latched on the rising edge of the logical OR of CLK A and CLK B. The TC control specifies the inputs as two's complement (TC high) or unsigned magnitude (TC low). RND, when high, adds 1 to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

The ACC and SUB inputs control accumulator operation. Assertion of ACC results in addition of the multiplier result and the accumulator contents, with the result stored in the accumulator register at the rising edge of CLK R. ACC and SUB high results in subtraction of the accumulator contents from the multiplier product, with the result again stored in the accumulator register. With ACC low, no accumulation occurs and the next product is loaded directly into the output register.

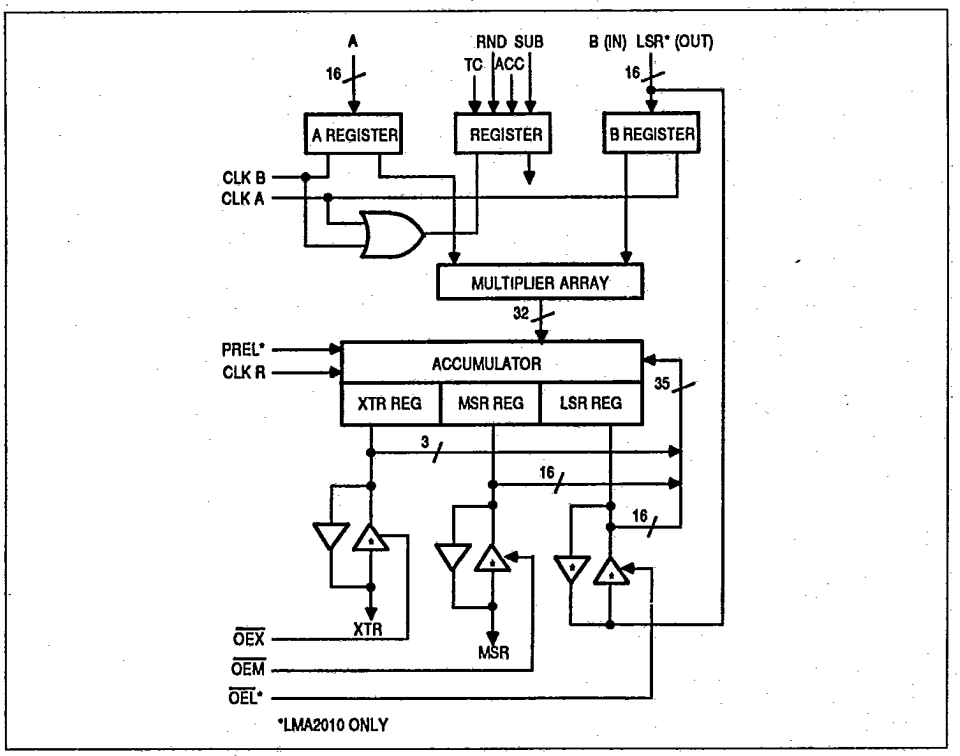
The LMA2010/2043 output (accumulator) register is divided into three independently controlled sections. The least significant result (LSR) and the most significant result (MSR) registers are 16 bits in length. The extended result register (XTR) is three bits long. In the LMA2010, the LSR output pins are multiplexed with the B inputs.

Each output register has an independent output enable control. In addition to providing three state control of the output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are high and PREL is high data can be preloaded via the bidirectional output pins into the appropriate output registers (LMA2010 only). Data present on the output pins is loaded in on the rising edge of CLK R. The interrelation of the PREL and the enable controls is summarized in the preload truth table.

features

- High-speed (45ns), low-power CMOS Multiplier-Accumulator
- Replaces TRW TDC1010/TDC1043 and AMD Am29510
- 16 x 16 bit multiplication and 35-bit product accumulation
- TTL compatible inputs and outputs
- Three-state outputs
- Two's complement and unsigned magnitude operands
- Accumulator performs accumulation, subtraction, and rounding
- Accumulator can be preloaded from external source (LMA2010 only)
- Available in: LCC, low cost plastic LCC, or Ceramic Leadless Chip Carrier. (For others see LMA1010/1043)
- Available with full High-Rel screening

functional diagram



PRELOAD TRUTH TABLE
(LMA 2010 ONLY)

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

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device pinouts

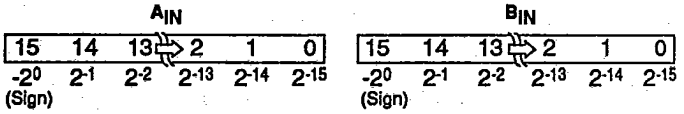
PIN	FUNCTION-LMA2010/2043 J,K[1]
1	A6
2	A7
3	A8
4	A9
5	A10
6	A11
7	A12
8	A13
9	A14
10	A15
11	$\overline{OEL}$/NC
12	RND
13	SUB
14	ACC
15	CLKA
16	CLKB
17	V_{CC}
18	V_{CC}
19	V_{CC}
20	V_{CC}
21	TC
22	$\overline{OEX}$
23	PREL/GND
24	$\overline{OEM}$
25	CLKR
26	R34
27	R33
28	R32
29	R31
30	R30
31	R29
32	R28
33	R27
34	R26
35	R25
36	R24
37	R23
38	R22
39	R21
40	R20
41	R19
42	R18
43	R17
44	R16
45	R15/B15
46	R14/B14
47	R13/B13
48	R12/B12
49	R11/B11
50	R10/B10
51	R9/B9
52	R8/B8
53	GND
54	GND
55	R7/B7
56	R6/B6
57	R5/B5
58	R4/B4
59	R3/B3
60	R2/B2
61	R1/B1
62	R0/B0
63	A0
64	A1
65	A2
66	A3
67	A4
68	A5

NC= No Connection
1) Pins are sequenced counterclockwise from the pin 1 indicator in the top view

INPUT FORMATS

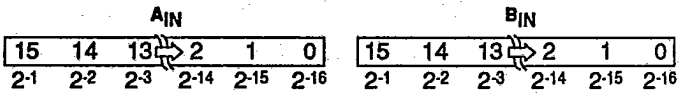
Fractional Two's Complement

TC=1



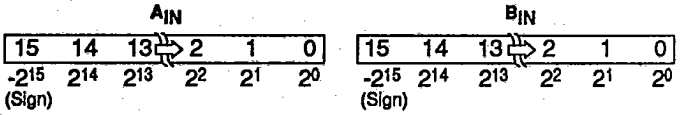
Unsigned Fractional

TC=0



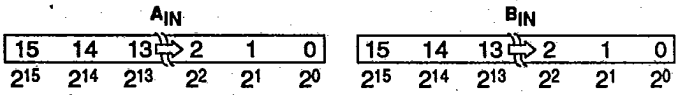
Integer Two's Complement

TC=1



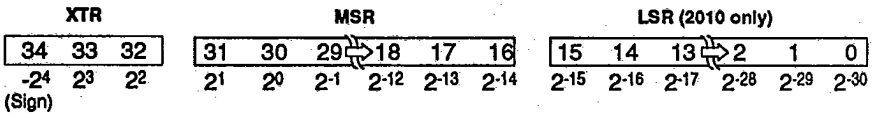
Unsigned Integer

TC=0

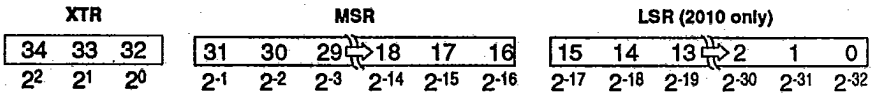


OUTPUT FORMATS

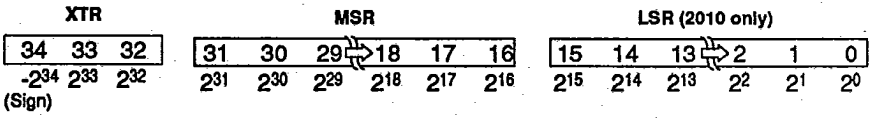
Fractional Two's Complement



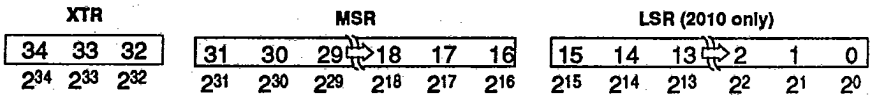
Unsigned Fractional



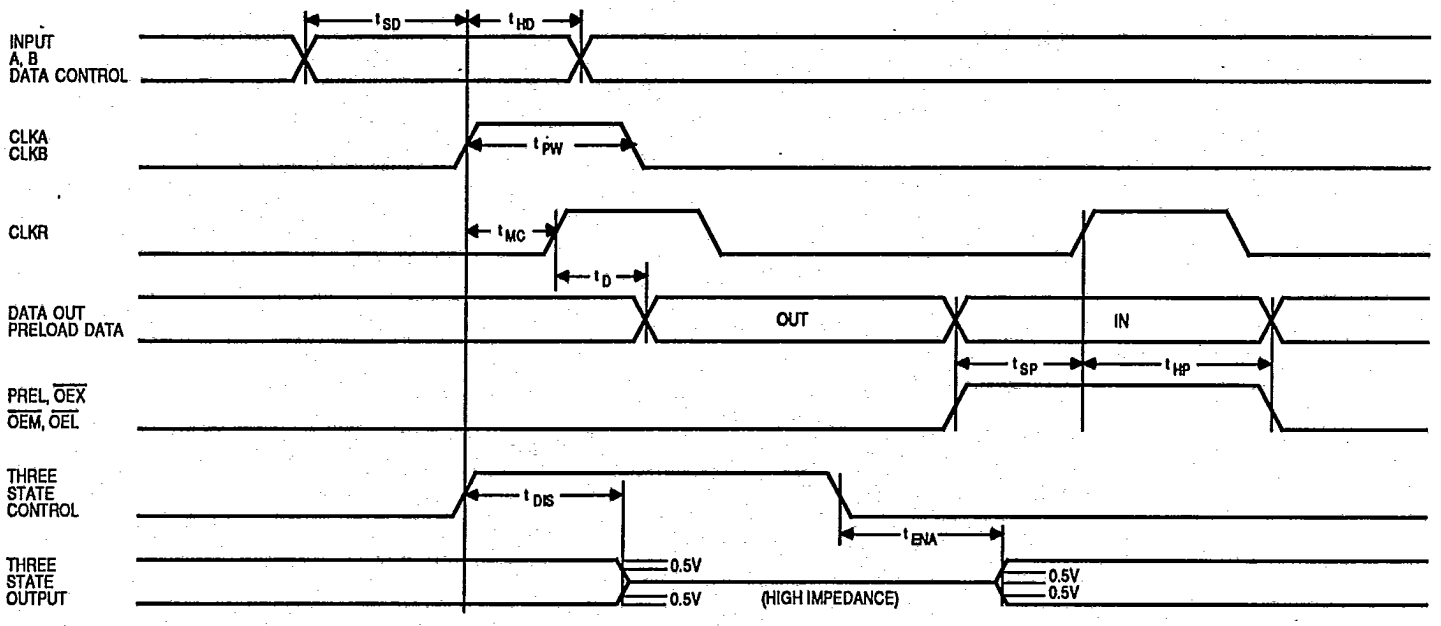
Integer Two's Complement



Unsigned Integer



timing diagram



switching characteristics

I. LMA2010/2043 Guaranteed Performance - Commercial Range

	Suffix:	None		65		55		45		units
PARAMETER	DESCRIPTION	min	max	min	max	min	max	min	max	
t_{MC}	Clocked Multiply-Accumulate Time		120		65		55		45	ns
t_D	Clock to Output Time		35		30		25		25	ns
t_{ENA}	Output Enable Time		35		30		30		30	ns
t_{DIS}	Output Disable Time		32		30		25		25	ns
t_{HD}	Data/Control Hold Time	3		0		0		0		ns
t_{HP}	Preload Hold Time	2		0		0		0		ns
t_{SD}	Data/Control Set-Up Time	20		15		15		10		ns
t_{SP}	Preload Set-Up Time	20		15		15		10		ns
t_{PW}	A, B, C, Clock Pulse Width	20		15		15		15		ns

AC TEST CONDITIONS: Input levels: 0 to 3V | Output timing reference level: 1.5V | Output load: 1.0KΩ to 5V, 820Ω to GND, 60pF to GND

II. LMA2010/2043 Guaranteed Performance - Military Range

	Suffix:	None		75		65		55		units
PARAMETER	DESCRIPTION	min	max	min	max	min	max	min	max	
t_{MC}	Clocked Multiply-Accumulate Time		140		75		65		55	ns
t_D	Clock to Output Time		45		35		30		30	ns
t_{ENA}	Output Enable Time		40		35		30		30	ns
t_{DIS}	Output Disable Time		40		35		25		25	ns
t_{HD}	Data/Control Hold Time	3		0		0		0		ns
t_{HP}	Preload Hold Time	3		0		0		0		ns
t_{SD}	Data/Control Set-Up Time	25		20		15		10		ns
t_{SP}	Preload Set-Up Time	25		20		15		10		ns
t_{PW}	A, B, C, Clock Pulse Width	25		20		15		15		ns

AC TEST CONDITIONS: Input levels: 0 to 3V | Output timing reference level: 1.5V | Output load: 1.0KΩ to 5V, 820Ω to GND, 60pF to GND

16 x 16 multiplier-accumulators

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absolute maximum ratings

Supply Voltage	-0.5V to 7.0V
Input Voltage	0V to 5.5V
Output Voltage	0V to 5.5V
Operating Temperature (Ambient)	-55°C to 125 °C
Storage Temperature	-65°C to 150°C

ordering information

Ordering Code	Speed (NS)	Package Type	Operating Range
LMA2010 JC-45 LMA2010 KC-45	45	J2 K3	Commercial
LMA2010 JC-55 LMA2010 KC-55	55	J2 K3	Commercial
LMA2010 KM-55 LMA2010 KMB-55	55	K3 K3	Military
LMA2010 JC-65 LMA2010 KC-65	65	J2 K3	Commercial
LMA2010 KM-65 LMA2010 KMB-65	65	K3 K3	Military
LMA2010 KM-75 LMA2010 KMB-75	75	K3 K3	Military
LMA2010 JC LMA2010 KC	120	J2 K3	Commercial
LMA2010 KM LMA2010 KMB	140	K3 K3	Military

recommended operating conditions

PARAMETER	DESCRIPTION		min	typ	max	unit
V_{CC}	Supply Voltage	Commercial	4.75	5.0	5.25	V
		Military	4.50	5.0	5.5	V
I_{OL}	Low Level Output Current				4.0	mA
I_{OH}	High Level Output Current				-2.0	mA
T_{AMB}	Operating Temperature	Commercial	0	25	70	°C
		Military	-55	25	125	°C

electrical characteristics

PARAMETER	DESCRIPTION		min	typ	max	unit
V_{IL}	Low level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{OL}	Low Level Output Voltage (I_{OL} = 8 mA)				0.5	V
V_{OH}	High Level Output Voltage (I_{OH} = -2 mA)		3.5			V
I_{IL}	Low Level Input Current (V_{IL} = 0.4 V)				20	µA
I_{IH}	High Level Input Current (V_{IH} = 2.4 V)				20	µA
I_{OZ}	Output Current (High-Impedance State)				20	µA
I_{CC}	Supply Current	(Quiescent)			1.0	mA
		(Dynamic)		121	252	mA

1) 5 MHz clock rate, TTL input levels; V_{CC} = 5V; T_A = 25° C; random input patterns; no load.
2) 5 MHz clock; V_{IH} = 2.0V, V_{IL} = 0.8V, V_{CC} = 5.5V, T_A = -55°C, all outputs toggling every cycle; no load.

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