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Mosaic Semiconductor Inc.

MIXED TECHNOLOGY PUMA

PUMA 2X0215

ISSUE 1.1 : October 1991

ADVANCE PRODUCT INFORMATION

524,288 bit EEPROM and 524,288 bit SRAM

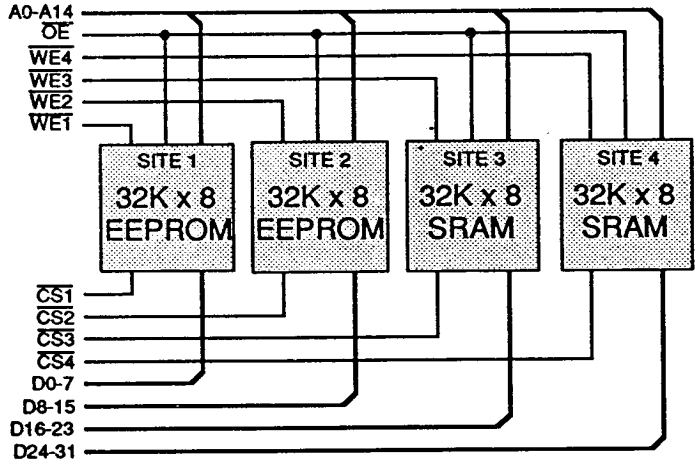
Features

Output user configurable as 8 / 16 bit wide.
Average Power EEPROM 732 / 1155 mW (max).
SRAM 666 / 1023 mW (max).
Standby Power 83 mW (max).
Single Power Supply voltage of V_{CC} = 5.0V±10%.
On-board decoupling capacitors.
All Inputs and Outputs TTL Compatible.
May be screened in accordance with MIL-STD-883C.

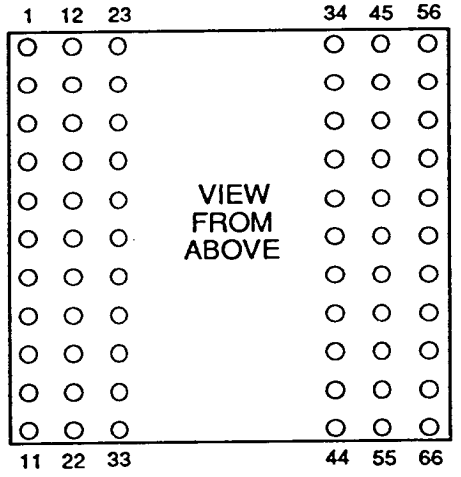
EEPROM Data Access times of 90/120 ns.
Write Cycle Endurance of 10^4 cycles.
Data Retention Time of 10 years.
Hardware and Software Data Protection.
Page Write of 1 to 64 bytes in 10ms.

SRAM Data Access times of 35/45/55/70 ns.
Completely Static Operation.

Block Diagram



Pin Definition

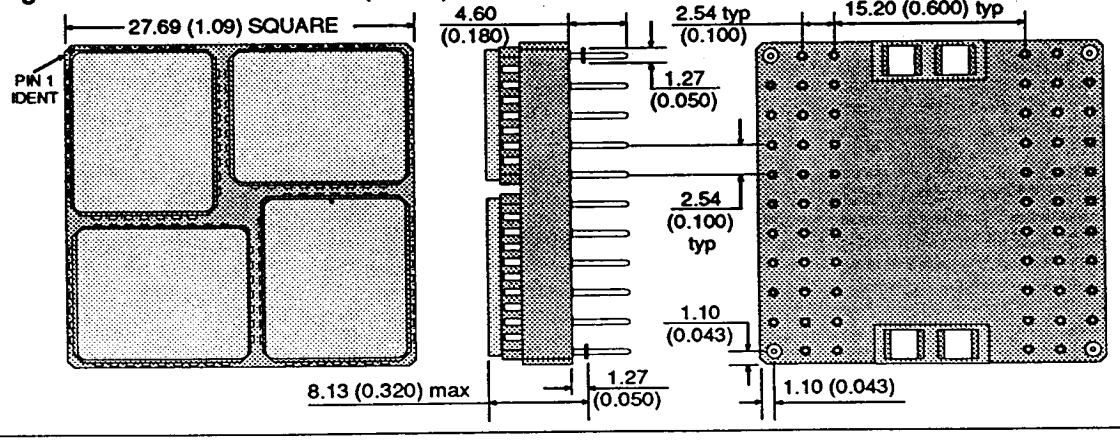


For pinout see page 2.

Pin Functions

A0~14	Address Inputs
D0~31	Data Inputs/Outputs
$\overline{CS1}$~4	Chip Selects (active low)
$\overline{OE}$	Output Enable
$\overline{WE1}$~4	Write Enable
NC	No Connect
V_{CC}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



GENERAL DESCRIPTION AND COMMON PARAMETERS

The PUMA 2X0215 provides two types of memory storage in one package; 524,288 bit CMOS Non-volatile EEPROM organised as 32,768 x 16, and 524,288 bit CMOS SRAM organized as 32,768 x 16.

The way in which the EEPROMs operate is obviously different to the operation of the Static RAMs. For this reason, the technical data which follows is separated into an EEPROM section (pages 4 to 9) and a SRAM section (pages 10 to 13) with both 8 and 16 bit modes covered for both types of memory. Note that the DC Electrical Characteristics parameters in both sections are for the ***entire*** module, irrespective of whether they are in the EEPROM section or the SRAM section.

On this module the EEPROMs are controlled by input lines $\overline{CS1}$, $\overline{CS2}$, $\overline{WE1}$ and $\overline{WE2}$, while the SRAMs are controlled by lines $\overline{CS3}$, $\overline{CS4}$, $\overline{WE3}$ and $\overline{WE4}$.

The EEPROM part of the PUMA 2X0215 contains non-volatile memories which will retain data without power for a minimum of 10 years. The EEPROMs are accessed in a similar way to Static RAM for the Read and Write cycles, but with extended write cycles in order to write the data into the non-volatile memory cells. In order to speed up this write cycle, an internal 64 byte page register is provided, which allows up to 64 bytes to be written simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are latched, thus freeing the address and data buses for other operations. Following the initiation of a write cycle, the EEPROMs will automatically write the latched data using an internal control timer, with the end of the write operation being indicated by both $\overline{DATA}$ polling and Toggle bit.

The PUMA 2X0215 also has an optional Software Data Protection mechanism for the EEPROMs to guard against accidental writes during normal device operation and during power supply transitions. Data corruption during switch on and switch off are further prevented by internal circuitry which detects both a V_{cc} drop and noise pulses on $\overline{WE1,2}$ and $\overline{CS1,2}$.

The SRAMs used on the PUMA 2X0215 are CMOS devices giving high speed combined with low power consumption. They are fully static in operation, with a reduced power consumption standby mode when disabled by taking $\overline{CS3,4}$ to a high voltage level.

Connection Table

PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name
1	D8	2	D9	3	D10	4	A13	5	A14
6	NC	7	NC	8	NC	9	D0	10	D1
11	D2	12	$\overline{WE2}$	13	$\overline{CS2}$	14	GND	15	D11
16	A10	17	A11	18	A12	19	V_{cc}	20	$\overline{CS1}$
21	NC	22	D3	23	D15	24	D14	25	D13
26	D12	27	$\overline{OE}$	28	NC	29	$\overline{WE1}$	30	D7
31	D6	32	D5	33	D4	34	D24	35	D25
36	D26	37	A6	38	A7	39	NC	40	A8
41	A9	42	D16	43	D17	44	D18	45	V_{cc}
46	$\overline{CS4}$	47	$\overline{WE4}$	48	D27	49	A3	50	A4
51	A5	52	$\overline{WE3}$	53	$\overline{CS3}$	54	GND	55	D19
56	D31	57	D30	58	D29	59	D28	60	A0
61	A1	62	A2	63	D23	64	D22	65	D21
66	D20								

Absolute Maximum Ratings (1)

Input Voltage	V_{IN}	-0.5	to	+6.25	V
Temperature Under Bias	T_{BIAS}	-55	to	+125	°C
Storage Temperature	T_{STG}	-65	to	+150	°C
Power Dissipation	P_T		2		W

Notes (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the above conditions for extended periods may affect device reliability.

Recommended Operating Conditions

			min	*typ*	*max*	
DC Supply Voltage		V_{CC}	4.5	5.0	5.5	V
Input High Voltage	TTL levels	V_{IH}	2.2	-	V_{CC}+0.3	V
	CMOS levels	V_{IHC}	V_{CC}-0.2	-	V_{CC}+0.3	V
Input Low Voltage	TTL levels	V_{IL}	-0.3	-	0.8	V
	CMOS levels	V_{ILC}	-0.3	-	0.3	V
Operating Temperature		T_A	0	-	70	°C
		T_{AI}	-40	-	85	°C (I suffix)
		T_{AM}	-55	-	125	°C (M, MB suffix)

Capacitance (V_{CC}=5V±10%,T_A=25°C, f=1MHz)

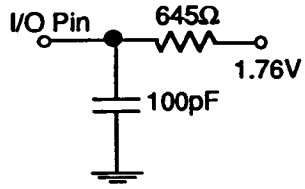
Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	A0-14, $\overline{OE}$	C_{IN1}	V_{IN} = 0V	-	46	pF
	$\overline{CS1\text{-}4}$ & $\overline{WE1\text{-}4}$	C_{IN2}	V_{IN} = 0V	-	27	pF
Output Capacitance	D0-D15	C_{OUT1}	$V_{I/O}$ = 0V	-	22	pF
	D15-D31	C_{OUT2}	$V_{I/O}$ = 0V	-	14	pF

Note : Capacitance calculated, not measured.

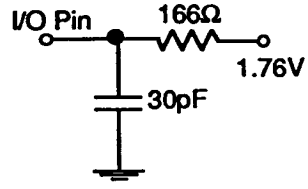
AC Test Conditions

* Input pulse levels: 0.8V to 2.4V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* V_{CC}=5V±10%
* The PUMA 2X0215 is tested in 16 bit mode.

Output Loads - EEPROM



SRAM



EPROM DATA

DC Electrical Characteristics (T_A = -55°C to +125°C, V_{CC} = 5V ± 10%)

Parameter		Symbol	Test Condition	min	typ(2)	max	Unit
I/P Leakage Current	A0 -A16, $\overline{OE}$	I_{LI1}	V_{CC} = V_{CC} max, V_{IN} = 0V or V_{CC}	-	-	±30	µA
	$\overline{WE1-2}$, $\overline{CS1-2}$	I_{LI2}	V_{CC} = V_{CC} max, V_{IN} = 0V or V_{CC}	-	-	±10	µA
Output Leakage Current	D0-D15	I_{LO}	V_{CC} = V_{CC} max, V_{OUT} = 0V or V_{CC}	-	-	±10	µA
V_{CC} Average Operating Current	16 bit	I_{CCO16}	$\overline{CS}$ (1) = V_{IL}, I_{OUT} = 0mA, f = 5MHz	-	-	210	mA
	8 bit	I_{CCO8}	As above	-	-	133	mA
Standby Supply Current	TTL	I_{SB1}	$\overline{CS}$ (1) = V_{IH}	-	-	56	mA
	CMOS	I_{SB2}	$\overline{CS}$ (1) = V_{IHC}, $V_{ILC} \geq V_{IN} \geq V_{IHC}$	-	-	15	mA
Output Low Voltage	D0-D15	V_{OL}	I_{OL} = 6.0 mA.	-	-	0.45	V
Output High Voltage	TTL loading	V_{OH1}	I_{OH} = -4.0 mA. (D0-D15)	2.4	-	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1-2}$. These inputs must be operated simultaneoulsy for 16 bit operation and singly for 8 bit mode.

(2) Typical figures are measured at 25°C and nominal V_{CC}

(3) During the above operations, $\overline{CS3-4}$ and $\overline{WE3-4}$ must be held at a logic high level.

EEPROM Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

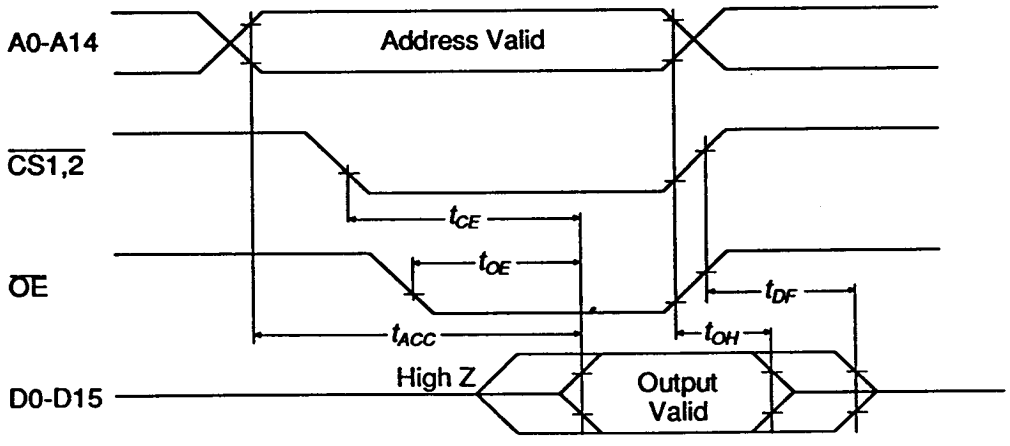
Parameter	Symbol	90 min	90 max	120 min	120 max	Unit
Address to Output Delay	t_{ACC}	-	90	-	120	ns
$\overline{CS1,2}$ to Output Delay	t_{CS}	-	90	-	120	ns
$\overline{OE}$ to Output Delay (1)	t_{OE}	0	40	0	50	ns
$\overline{CS1,2}$ or $\overline{OE}$ to Output Float (2)(3)	t_{DF}	0	40	0	50	ns
Output Hold from $\overline{OE}$, $\overline{CS1,2}$ or Address	t_{OH}	0	-	0	-	ns

Notes: (1) $\overline{OE}$ may be delayed up to t_{CS} - t_{OE} after the falling edge of $\overline{CS1,2}$ without impact on t_{CS} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.

(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CS1,2}$ whichever occurs first (C_L = 5pF).

(3) This parameter is only sampled and is not 100% tested.

Read Cycle Timing Waveform

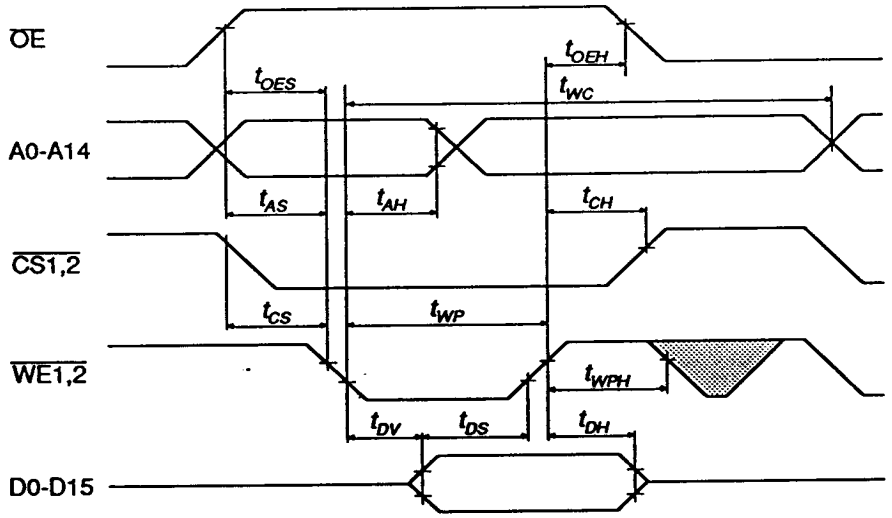


Write Cycle

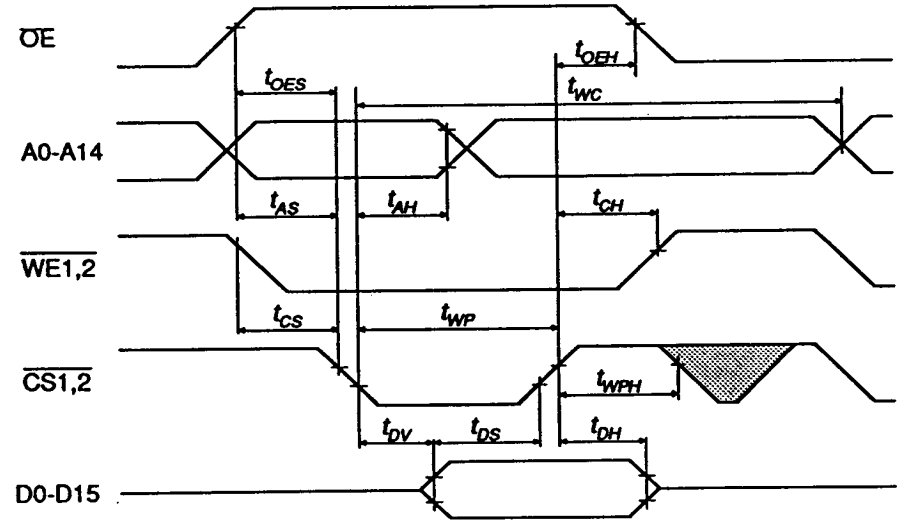
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Address, OE Set-up Time	t_{AS}, t_{OES}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width ($\overline{WE1,2}$ or $\overline{CS1,2}$)	t_{WP}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data, OE Hold Time	t_{DH}, t_{OEH}	0	-	-	ns
Time to Data Valid	t_{DV}	NR	-	-	
Write Cycle Time	t_{WC}	-	-	10	ms

Note: NR = No Restriction

AC Write Waveform - $\overline{WE}$ Controlled



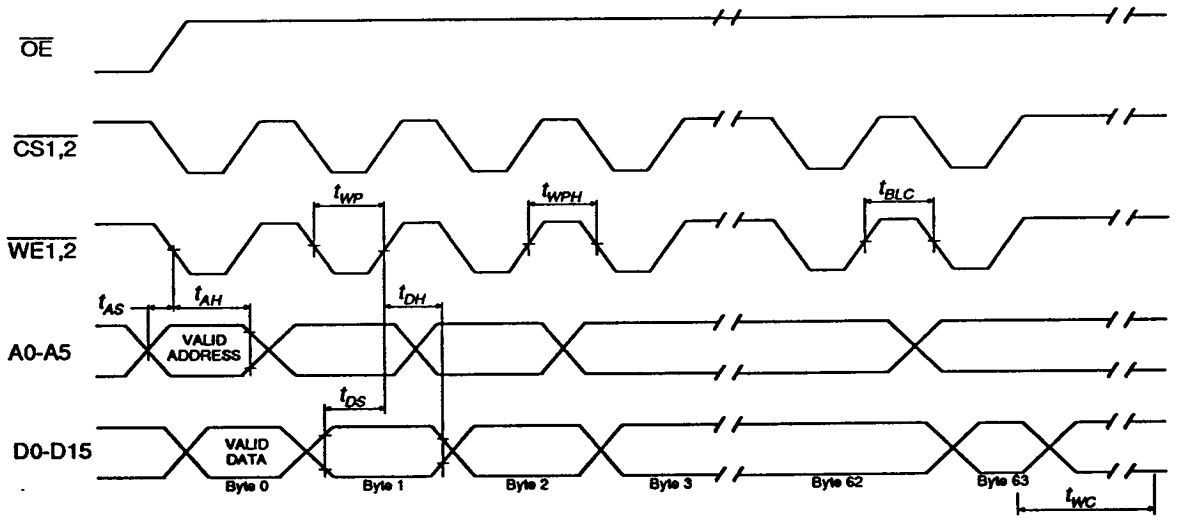
AC Write Waveform - $\overline{CS}$ Controlled



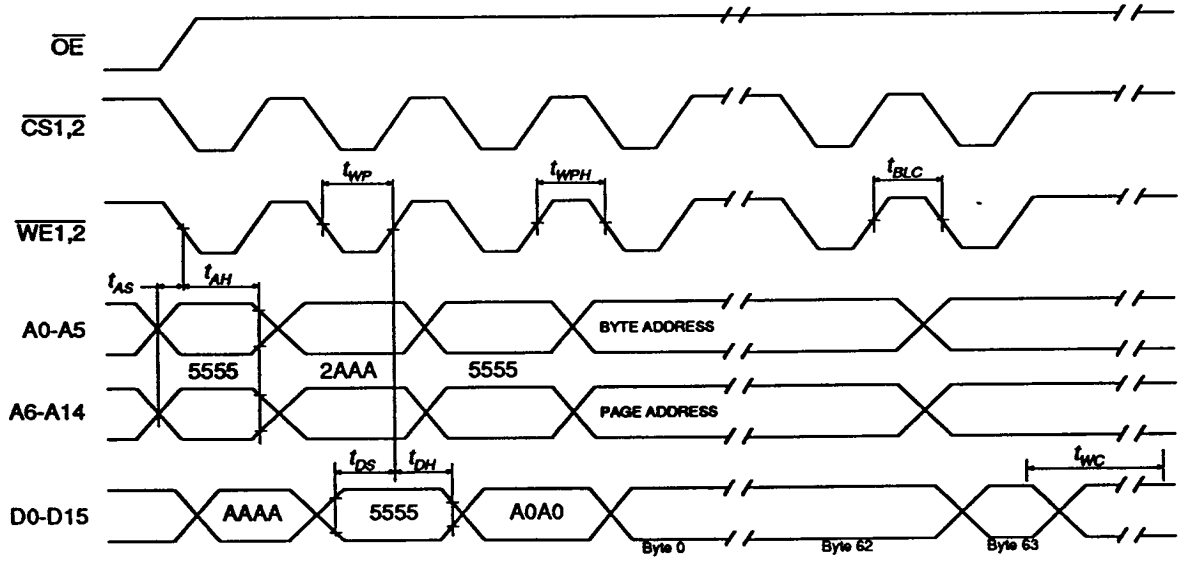
PAGE MODE WRITE CHARACTERISTICS

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Write Cycle Time	t_{WC}	-	-	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	0	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
Byte Load Cycle Time	t_{BLC}	-	-	150	µs
Write Pulse Width High	t_{WPH}	50	-	-	ns

Page Mode Write Waveform (1)



Software Protected Write Waveform (1)



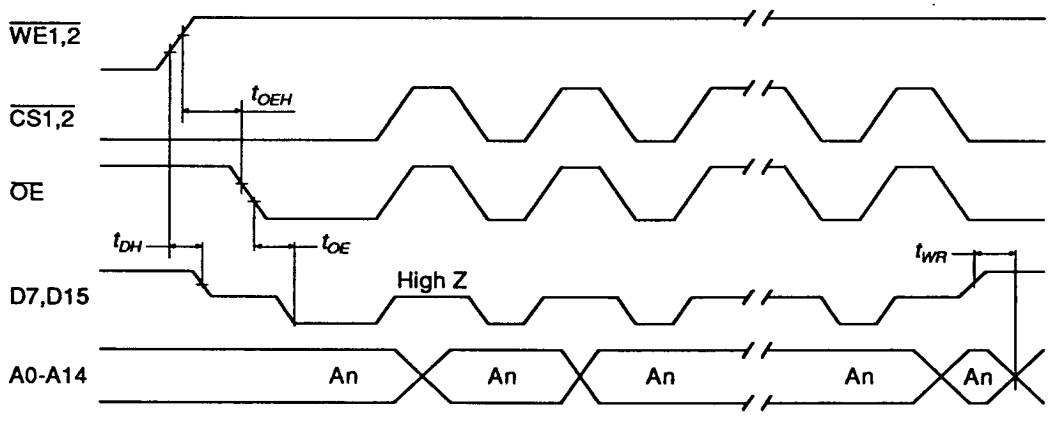
Note (1) A6 through A14 must specify the page address during each high to low transition of $\overline{WE1,2}$ (or $\overline{CS1,2}$). $\overline{OE}$ must be high only when $\overline{WE1,2}$ and $\overline{CS1,2}$ are low.

DATA Polling Characteristics (1)

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Data Hold Time	t_{DH}	0	-	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	-	-	ns
$\overline{OE}$ to Output Delay	t_{OE}	-	-	100	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Note : (1) These parameters are sampled and not 100% tested.

DATA Polling Waveform

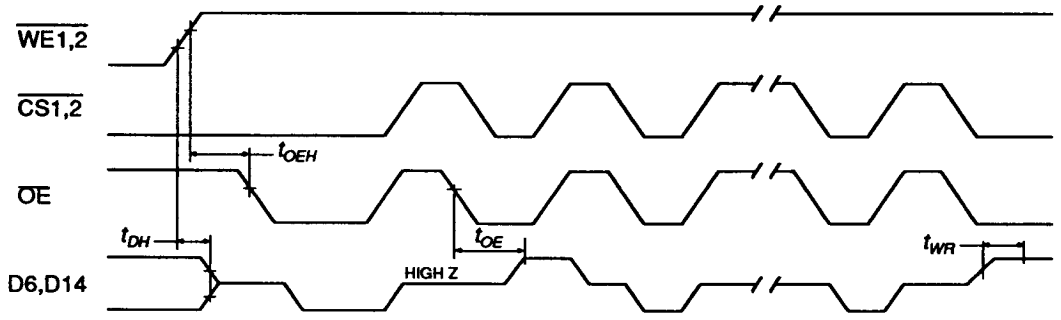


Toggle Bit Characteristics (1)

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Data Hold Time	t_{DH}	10	-	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	10	-	-	ns
$\overline{OE}$ to Output Delay	t_{OE}	-	-	100	ns
$\overline{OE}$ High Pulse	t_{OEHP}	150	-	-	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Note : (1) These parameters are sampled and not 100% tested.

Toggle Bit Waveform



Notes : (1) Toggling either $\overline{OE}$ or $\overline{CS1,2}$ or both $\overline{OE}$ and $\overline{CS1,2}$ will operate toggle bit.
(2) Beginning and ending state of D6,D14 may vary.
(3) Any address location may be used but the address should not vary.

EEPROM Operation

Operating Modes

The table below shows the logic inputs required to control the operating modes of the EEPROMs.

MODE	$\overline{CS1,2}$	$\overline{OE}$	$\overline{WE1,2}$	Outputs
Standby	1	X	X	High Z
Output Disable	X	1	X	High Z
Read	0	0	1	D_{OUT}
Write	0	1	0	D_{IN}
Write Inhibit	X	X	1	
	X	0	X	

$1 = V_{IH}$ $0 = V_{IL}$ X = Don't care

Read

The EEPROMs are accessed in the same way as a static RAM, with the data stored at the memory location detemined by the address pins being placed on the output pins when $\overline{CS1,2}$ and $\overline{OE}$ are low, and $\overline{WE1,2}$ is high. Whenever $\overline{CS1,2}$ or $\overline{OE}$ are high, the outputs are in the OFF or high impedance state.

Write

A low pulse on $\overline{WE1,2}$ with $\overline{CS1,2}$ low or a low pulse on $\overline{CS1,2}$ with $\overline{WE1,2}$ low indicates a Write Cycle. The address is latched on the falling edge of $\overline{CS1,2}$ or $\overline{WE1,2}$, and the data is latched on the first rising edge of $\overline{CS1,2}$ or $\overline{WE1,2}$. Once a Byte Write has begun it will automatically time itself to completion.

Page Mode Write

This mode allows 1 to 64 bytes of data to be loaded into the EEPROMs, which are then simultaneously written. Once the first byte has been written, each subsequent byte must have the high to low transition of $\overline{WE1,2}$ (or $\overline{CS1,2}$) within 150µs of the same transition of the previous byte. If this 150µs time is exceeded, the load period ends and internal programming starts. A6 to A14 specify the page address (which must be valid during the above transitions) and A0 to A5 specify which bytes within the page are to be written. Note that the bytes may be loaded in any order and may be changed within the same load period.

$\overline{DATA}$ Polling

In order to detect the end of a Write Cycle, two methods are provided. During a Write operation (Byte or Page) an attempt to Read the device will result in the complement of the written data appearing on D7, D15. Once the Write Cycle is complete true data appears on the outputs and the next Write Cycle may begin.

TOGGLE bit

In addition to $\overline{DATA}$ polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6, D14 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read.

Hardware Data Protection

Four types of hardware protection give high security against accidental writes:

(a) If $V_{CC} < 3.2V$ write is inhibited

(b) At power on, the device times out 5ms before allowing a Write.

(c) $\overline{OE}$ low, $\overline{CS1,2}$ or $\overline{WE1,2}$ high inhibits writes.

(d) Pulses of less than 15ns on $\overline{WE1,2}$ or $\overline{CS1,2}$ do not initiate a write cycle.

Software Data Protection

Software controlled data protection, once enabled by the user, necessitates the use of a software algorithm before any Write can be performed. To enable this feature a special sequence of Writes must be performed, and must be reused for each subsequent Write cycle. Once set the data protection remains operational until it is disabled by using a second algorithm; power transitions will not reset this feature.

Note that the EEPROMs are supplied with the Software Data Protection feature **disabled.**

The algorithms to enable and disable the protection are shown overleaf, with each flow chart showing the necessary actions for a single device. Once enabled, the same three bytes must be loaded to the same addresses before any Writes will occur to a particular device.

All software write commands must obey the Page Write timing specifications.

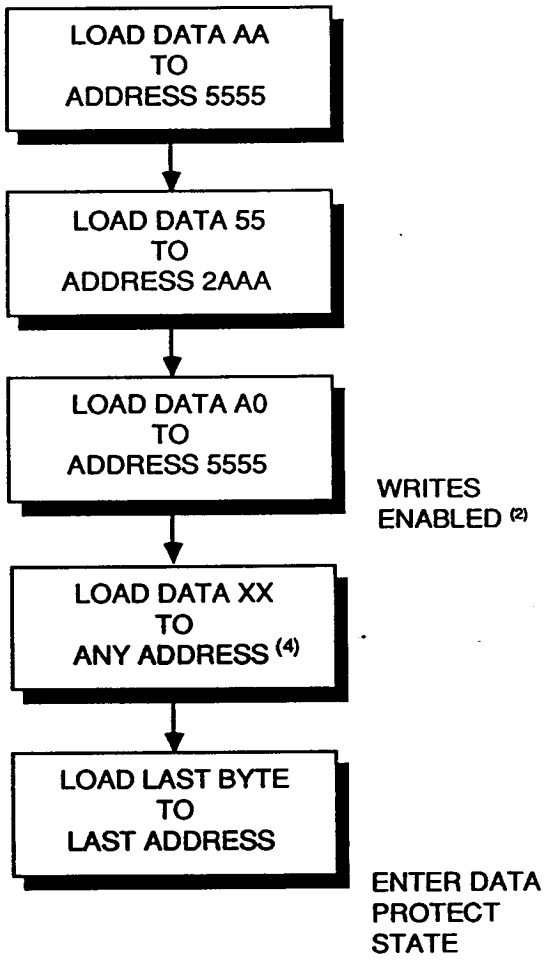
The process of disabling the Data Protection mode is very similar to that described for enable, except 6 bytes must be loaded to specific locations for each EEPROM as shown.

Note here the use of the word 'load' to describe enabling and disabling the protection modes in preference to

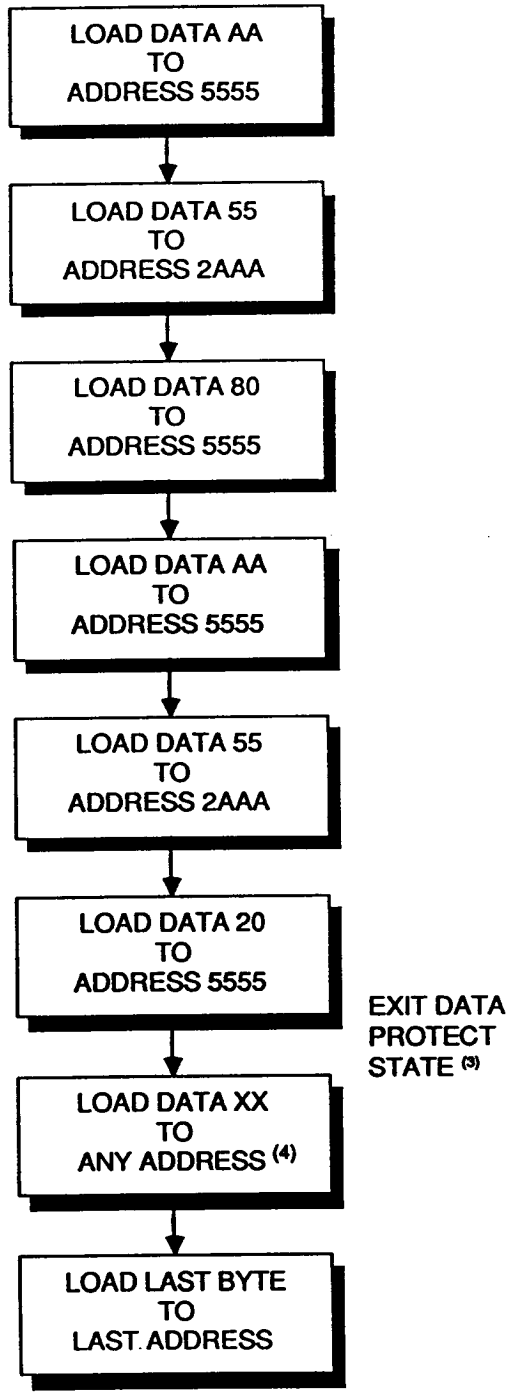
'write'. Although it may seem that if the Write command sequence is performed to enable protection then the three bytes at those addresses will be overwritten with AA,55,A0, this is not the case. This is because these Writes obey Page Write parameters, where A6 - A14 must remain valid to specify the page address, but during this enable sequence they change. Actual Writes therefore never occur, and data is not corrupted during an enable sequence.

For the same reasons no Writes are performed during the disable routine, in addition to the fact that since Data Protection is enabled no Writes can occur without the correct bytes being loaded in sequence.

ENABLE ALGORITHM



DISABLE ALGORITHM



NOTES

(1) Data D7 - D0 (hex); Address A14 - A0 (hex).

(2) Write Protect Mode will be activated at end of Write even if no other data is loaded.

(3) Write Protect Mode will be deactivated at end of Write even if no other data is loaded.

(4) 1 to 64 bytes of data may be loaded.

SRAM DATA

DC Electrical Characteristics (V_{CC}=5V±5%,T_A=-55°C to +125°C)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*(1)	*max*	*Unit*
I/P Leakage Current	A0-A14, $\overline{OE}$	I_{LI1}	V_{IN} = 0V to V_{CC}	-	-	±30	µA
	$\overline{WE3\text{-}4}$, $\overline{CS3\text{-}4}$	I_{LI2}	As above	-	-	±5	µA
Output Leakage Current	D16-D31	I_{LO}	$\overline{CS}$(2) = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}	-	-	±5	µA
Average Supply Current	16 bit	I_{CCA16}	$\overline{CS}$(2) = V_{IL}, Minimum cycle, $I_{I/O}$ = 0mA	-	-	186	mA
	8 bit	I_{CCA8}	As above	-	-	121	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}$(2) = V_{IH}	-	-	56	mA
	CMOS levels	I_{SB2}	$\overline{CS}$(2) ≥ V_{IHC}, V_{ILC} ≥ V_{IN} ≥ V_{IHC}	-	-	15	mA
Output Voltage Low	D16-D31	V_{OL}	I_{OL} = 8.0mA	-	-	0.4	V
Output Voltage High	D16-D31	V_{OH}	I_{OH} = - 4.0mA	2.4	-	-	V

Notes: (1) Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

(2) $\overline{CS}$ above is accessed through $\overline{CS3\text{-}4}$. These inputs must be operated simultaneously for 16 bit mode and singly for 8 bit mode.

(3) During the above operation, $\overline{CS1\text{-}2}$ and $\overline{WE1\text{-}2}$ must be held at a logic high level.

Operating Modes

This Table shows the inputs required to control the operating modes of the SRAMs on the PUMA 2X0215 and shows the SRAMs operating in 16 bit mode. If 8 bit operation is required, $\overline{CS3\text{-}4}$ and $\overline{WE3\text{-}4}$ are controlled independently.

Note that during 16 bit operation, $\overline{CS1\text{-}2}$ and $\overline{WE1\text{-}2}$, which control the EEPROM devices on the PUMA 2X0215, must be at a high level.

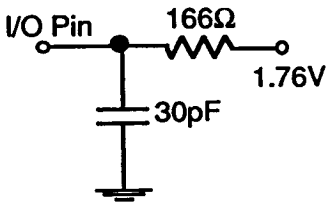
MODE	$\overline{CS3,4}$	$\overline{OE}$	$\overline{WE3,4}$	Outputs	Reference Cycle
Standby	1	X	X	High Z	
Read	0	1	1	High Z	Read Cycle
Read	0	0	1	D_{OUT}	Read Cycle
Write	0	X	0	D_{IN}	Write Cycle

1 = V_{IH} 0 = V_{IL} X = V_{IL} or V_{IH}

AC Test Conditions

* Input pulse levels: 0.45V to 2.4V.
* Input and Output timing reference levels: 0.8V and 2.0V
* Input rise and fall times: ≤ 10ns.
* Output load : see diagram
* Module is tested in 16 bit mode.

Output Load

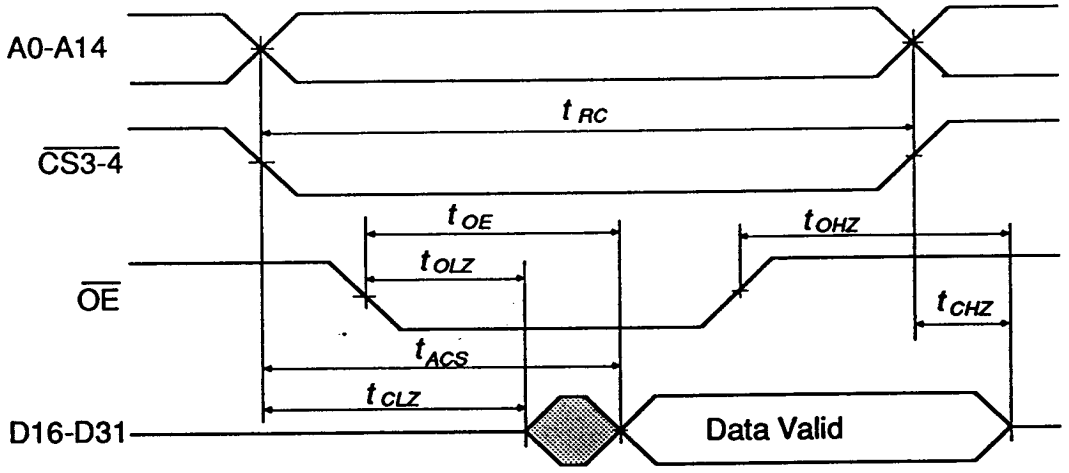


Electrical Characteristics & Recommended AC Operating Conditions

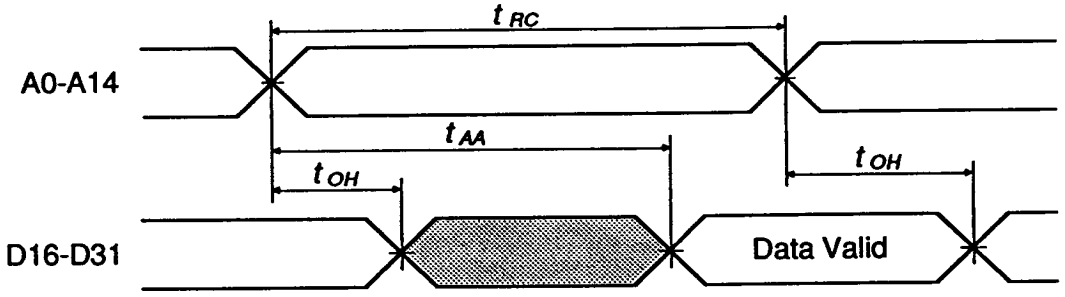
Read Cycle

Parameter	Symbol	-35 min	-35 max	-45 min	-45 max	-55 min	-55 max	-70 min	-70 max	Unit
Read Cycle Time	t_{RC}	35	-	45	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	45	-	55	-	70	ns
Chip Select Access Time	t_{ACS}	-	35	-	45	-	55	-	60	ns
Output Enable to Output Valid	t_{OE}	-	15	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z[5]	t_{CLZ}	6	-	6	-	6	-	6	-	ns
Output Enable to Output in Low Z[5]	t_{OLZ}	2	-	2	-	2	-	2	-	ns
Chip Deselection to Output in High Z[5]	t_{CHZ}	-	15	-	20	-	25	-	30	ns
Output Disable to Output in High Z[5]	t_{OHZ}	-	15	-	20	-	25	-	30	ns

Read Cycle 1 Timing Waveform [1] [3]



Read Cycle 2 Timing Waveform [1] [2]

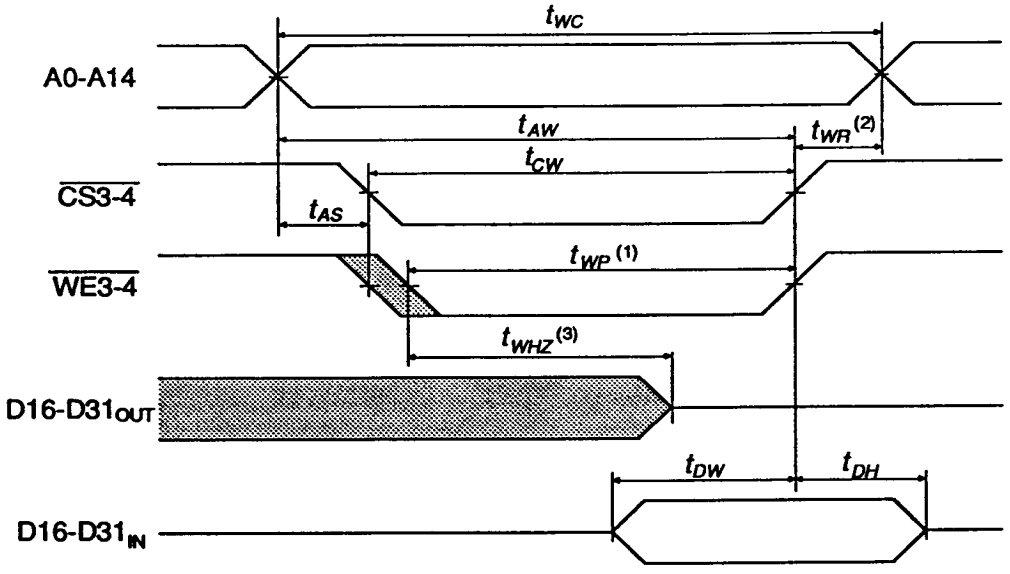


Notes: (1) $\overline{WE}$ is High for Read Cycle.
(2) Device is continuously selected, $\overline{CS}$=V_{IL}.
(3) Address valid prior to or coincident with $\overline{CS}$ transition Low.
(4) $\overline{OE}$=V_{IL}.
(5) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

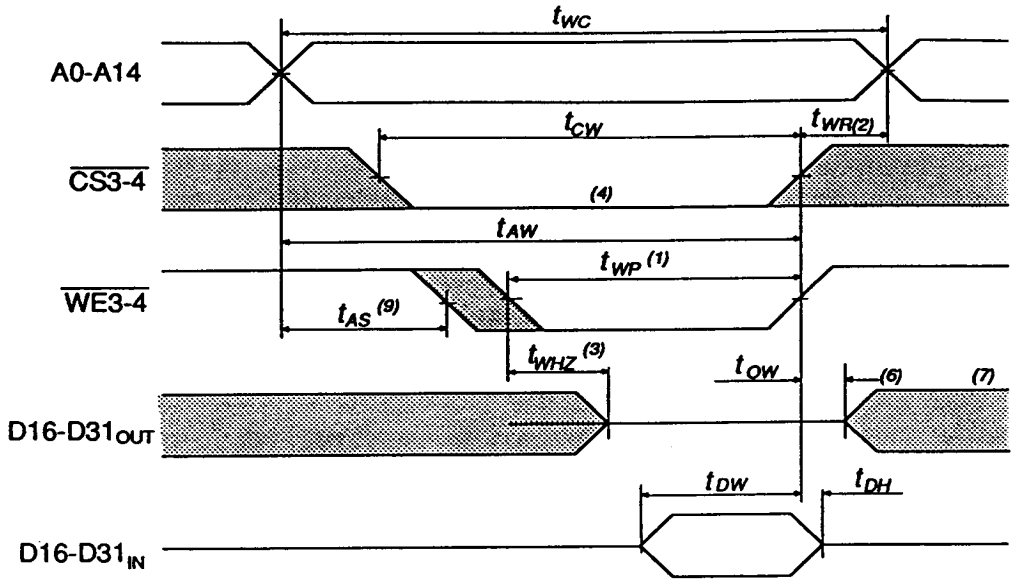
Write Cycle

Parameter	Symbol	-35 min	-35 max	-45 min	-45 max	-55 min	-55 max	-70 min	-70 max	Unit
Write Cycle Time	t_{WC}	35	-	45	-	55	-	70	-	ns
Chip Selection to End of Write	t_{CW}	30	-	40	-	50	-	60	-	ns
Address Valid to End of Write	t_{AW}	30	-	40	-	50	-	60	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	25	-	30	-	35	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z[10]	t_{WHZ}	0	18	0	20	0	25	0	30	ns
Data to Write Time Overlap	t_{DW}	20	-	20	-	25	-	30	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Write Disable to Output in Low Z[10]	t_{OW}	5	-	5	-	5	-	5	-	ns

Write Cycle 1 Timing Waveform



Write Cycle 2 Timing Waveform



AC Write Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})
(6) D_{OUT} is in the same phase as written data of this write cycle.
(7) D_{OUT} is the read data of next address.
(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
(9) $\overline{WE}$ must be high during all address transitions except when the device is deselected with $\overline{CS}$.
(10) t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C is shown below

MB MODULE SCREENING FLOW

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at T_A = +25°C (optional)	100%
Burn-In	Method 1015, Condition D, T_A = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at T_A=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per HMP or customer specification	

Ordering Information

PUMA 2X0215MB-1270

Field	Code	Meaning
SRAM Speed	35	35 ns
	45	45 ns
	55	55 ns
	70	70 ns
EEPROM Speed	90	90 ns
	12	120 ns
Temperature range	Blank	Commercial Temperature Range.
	I	Industrial Temperature Range.
	M	Military Temperature Range.
	MB	Screened in accordance with MIL-STD-883C
Organization	X0215	32K x 16 EEPROM on sites 1 and 2 32K x 16 SRAM on sites 3 and 4 (both user configurable as x8 outputs)
Module Type	PUMA 2	Ceramic 66 Pin Grid Array.

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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