MOTOROLA

Quad 2-Input NOR Gate with Strobe

Military 10H500

ELECTRICALLY TESTED PER:
MPG 10H500

The 10H500 is a quad 2 input NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

The MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply.

2

- Propagation Delay, 1.0 ns Typical
- 40 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10H500/BXAJC
X = CASE OUTLINE AS FOLLOWS:

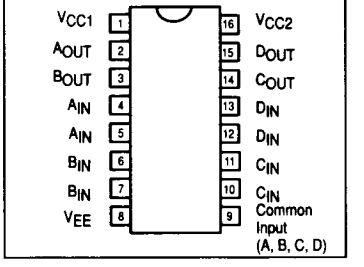
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

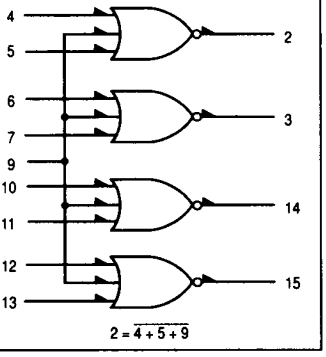
PIN ASSIGNMENTS

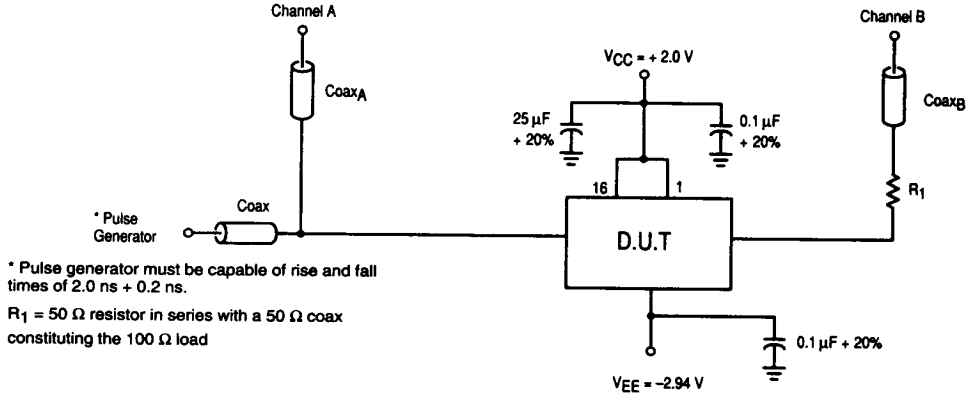
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	OPEN
A_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	OPEN
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
Common Input	9	13	12	OPEN
C_{IN}	10	14	13	OPEN
C_{IN}	11	15	14	OPEN
D_{IN}	12	16	15	OPEN
D_{IN}	13	1	17	OPEN
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM



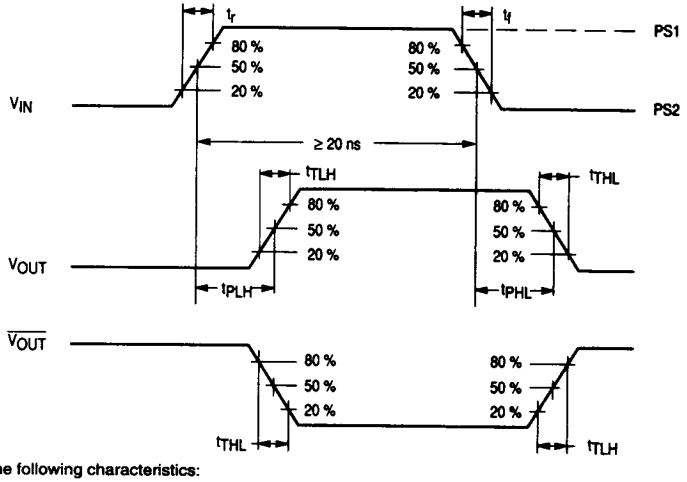


* Pulse generator must be capable of rise and fall times of 2.0 ns + 0.2 ns.

R_1 = 50 Ω resistor in series with a 50 Ω coax constituting the 100 Ω load

NOTES

1. Unused outputs should be loaded 100 Ω to GND.
2. Length of Coax$_A$ and Coax$_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns (20% - 80%) ± 0.2 ns.



NOTES

1. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.

Figure 1. Switching Test Circuit and Waveforms

10H500
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.11	-1.48	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IHA}	V_{ILA}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V		4, 5, 10, 11			8		1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	- 1.61	V	4-7, 9-13				8		1, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V				4-7, 9-13	8	8	1, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	-1.61	V			4-7, 9-13		8	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	- 26		- 29		- 29		mA					8		1, 16	8
I_{IH}	Input Current High		295		500		500	µA	4-7, 10-13				8		1, 16	4-7, 10-13
I_{IH1}	Input Current High		360		610		610	µA	9				8		1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4-7, 9-13			8		1, 16	4-7, 10-13

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, All tests rferenced to Fig 1, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.5	1.8	0.66	2.34	0.6	2.1	ns	4, 6	2, 3	1, 16	8	2, 3, 14, 15
t_{THL}	Fall time	0.5	1.8	0.66	2.34	0.6	2.1	ns	4, 6	2, 3	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High	0.6	1.5	0.84	2.04	0.66	1.92	ns	10, 13	14, 15	1, 16	8	2, 3, 14
t_{PHL}	Propagation Delay High to Low	0.6	1.5	0.84	2.04	0.66	1.92	ns	10, 13	14, 15	1, 16	8	2, 3, 14