STS20NHS3LL

N-CHANNEL 30 V - 0.0032 Ω - 20 A SO-8
STripFET™III MOSFET PLUS MONOLITHIC SCHOTTKY

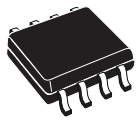
PRELIMINARY DATA

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS20NHS3LL	30V	< 0.004Ω	20A(1)

- TYPICAL R_{DS}(on) = 0.0032Ω @ 10V
- OPTIMAL R_{DS}(on) x Qg TRADE-OFF @ 4.5V
- REDUCED SWITCHING LOSSES
- REDUCED CONDUCTION LOSSES
- REDUCED DIODE RECOVERY LOSSES
- IMPROVED JUNCTION-CASE THERMAL RESISTANCE

Figure 1: Package

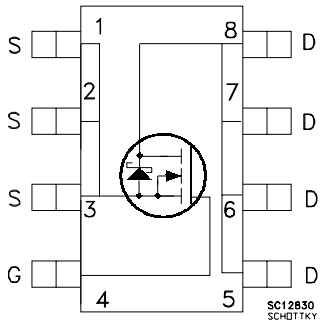


SO-8

DESCRIPTION

The **STS20NHS3LL** utilizes the latest advanced design rules of ST's proprietary STripFET™ technology, and a proprietary process for integrating a monolithic Schottky diode. The new MOSFET is optimized for the most demanding synchronous switch function in DC-DC converter for Computer and Telecom.

Figure 2: Internal Schematic Diagram



APPLICATIONS

- DC-DC CONVERTERS FOR TELECOM AND NOTEBOOK CPU CORE
- SYNCHRONOUS RECTIFICATION

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS20NHS3LL	20HS3LL-	SO-8	TAPE & REEL

Rev. 2

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{GS}	Gate- source Voltage	± 18	V
$I_{D(1)}$	Drain Current (continuous) at T_C = 25°C	20	A
I_D	Drain Current (continuous) at T_C = 100°C	12.6	A
I_{DM}(2)	Drain Current (pulsed)	80	A
P_{tot}	Total Dissipation at T_C = 25°C	2.7	W

Table 4: Thermal Data

Rthj-amb (3) T_j T_{stg}	Thermal Resistance Junction-ambient Max Maximum Operating Junction Temperature Storage Temperature	47 -55 to 150 -55 to 150	°C/W °C °C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AV}	Not-Repetitive Avalanche Current (pulse width limited by T_j max)	12.5	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25°C, I_D = I_{AV}, V_{DD} = 24V)	1.3	J

ELECTRICAL CHARACTERISTICS (T_J =25°C UNLESS OTHERWISE SPECIFIED)

Table 6: On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1mA, V_{GS} = 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = 24V			500	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 18V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1mA	1		2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 10A V_{GS} = 4.5V, I_D = 10A		0.0032 0.004	0.004 0.0055	Ω Ω

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (4)	Forward Transconductance	V_{DS}=15V, I_D = 12A		30		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		3950 720 70		pF pF pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 8: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 15V, I_D = 10A R_G = 4.7Ω , V_{GS} = 4.5V (see Figure 15)		TBD TBD		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=15V, I_D=20A V_{GS}= 4.5V (see Figure 17)		27.5 7.9 8.7	37	nC nC nC

Table 9: Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 15V, I_D = 10A R_G= 4.7Ω , V_{GS} = 4.5V (see Figure 15)		TBD TBD		ns ns

Table 10: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				20 80	A A
V_{SD} (4)	Forward On Voltage	I_{SD} = 10A ,V_{GS} = 0			0.7	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 10A, di/dt = 100A/µs V_{DD} = 25V, T_j = 150°C (see Figure 16)		 1.9	26 25	ns nC A

Notes:
1. This value is rated according to Rthj-pcb
2. Pulse width limited by safe operating area
3. When mounted on FR-4 board with 1 inch^2 pad, 2 oz of Cu and t < 10sec
4. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Figure 3: Safe Operating Area

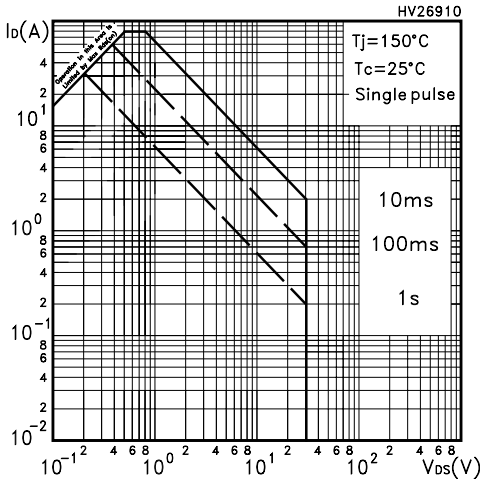


Figure 4: Output Characteristics

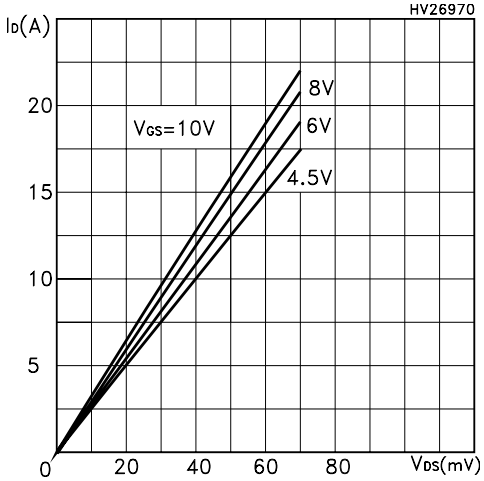


Figure 5: Transconductance

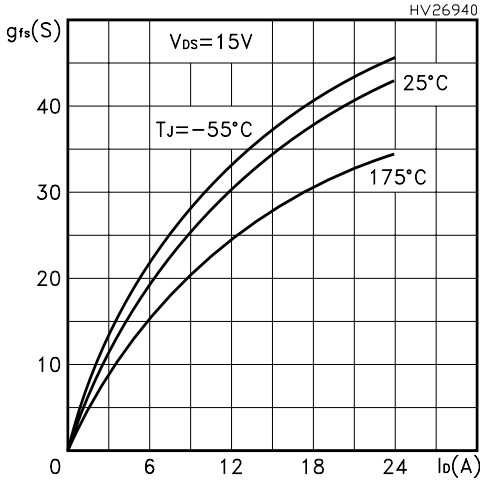


Figure 6: Thermal Impedance

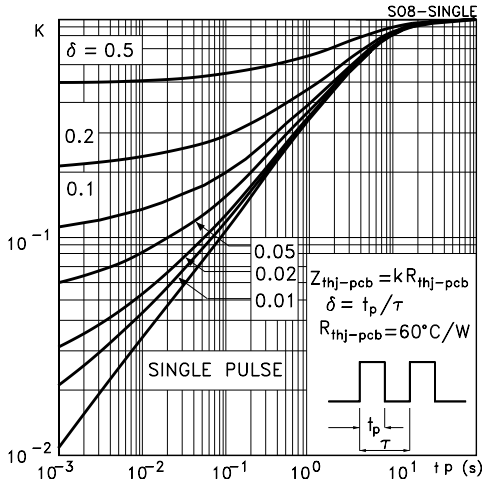


Figure 7: Transfer Characteristics

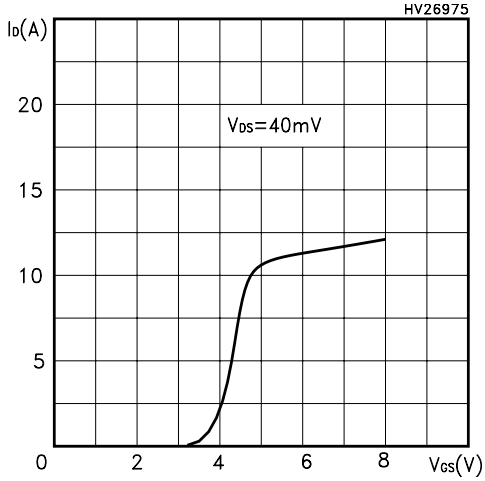


Figure 8: Static Drain-source On Resistance

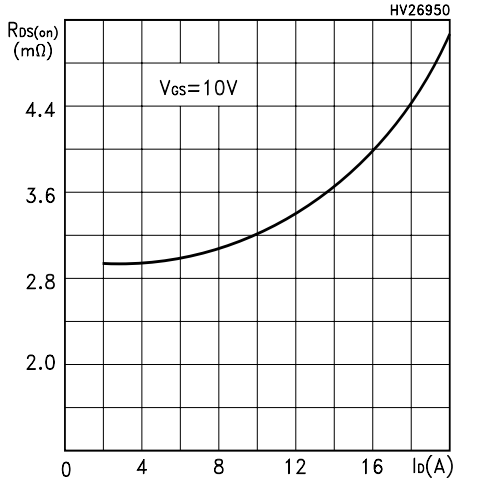


Figure 9: Gate Charge vs Gate-source Voltage

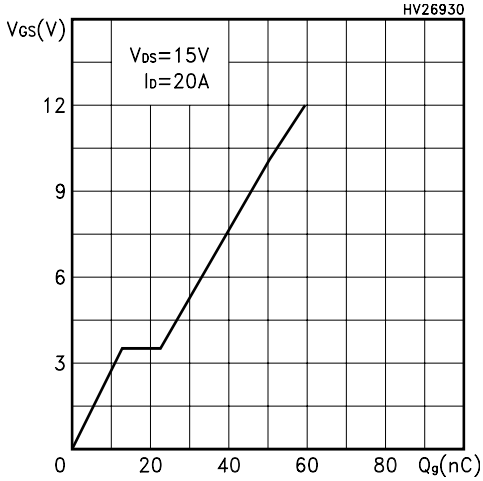


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

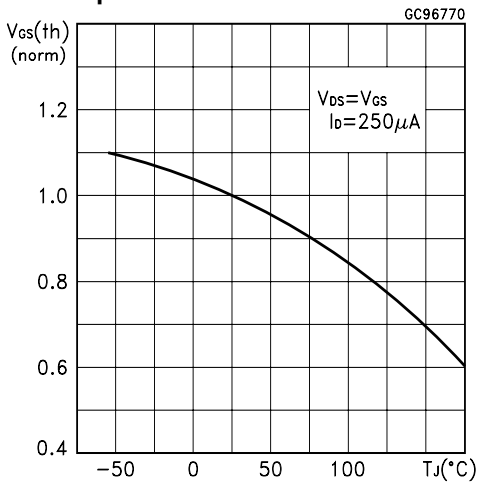


Figure 11: Normalized On Resistance vs Temperature

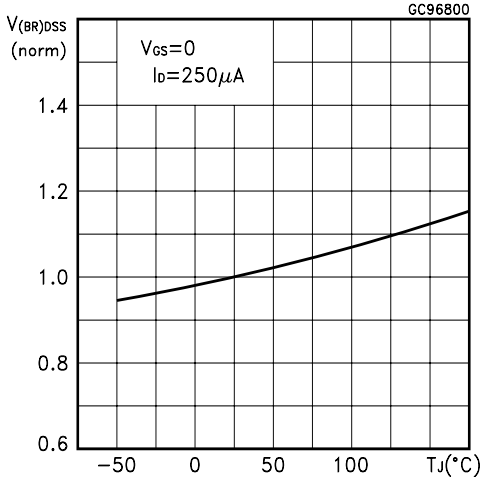


Figure 12: Capacitance Variations

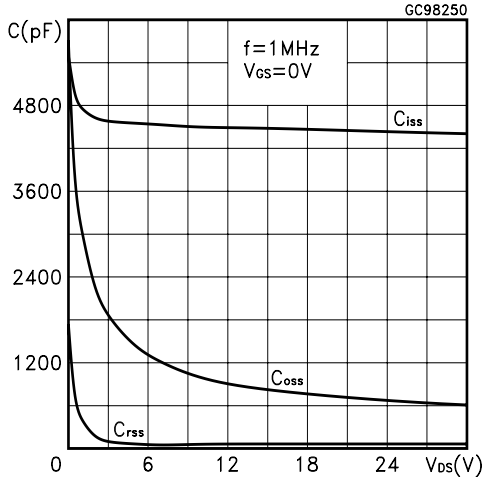


Figure 13: Normalized BVDSS vs Temperature

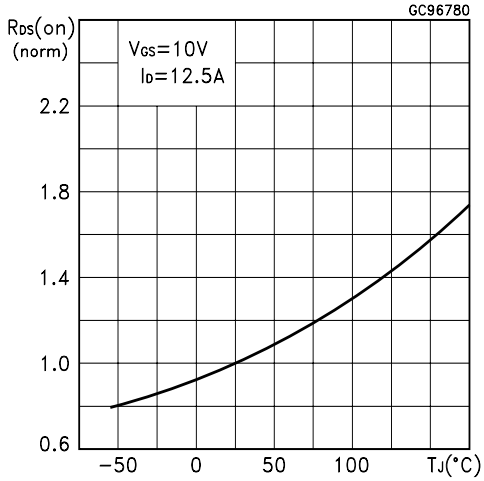


Figure 14: Source-Drain Diode Forward Characteristics

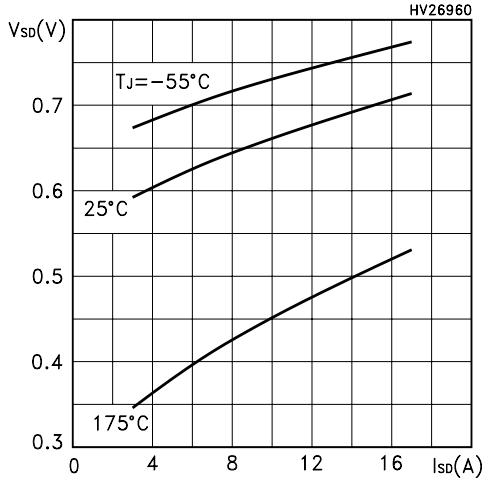


Figure 15: Switching Times Test Circuit For Resistive Load

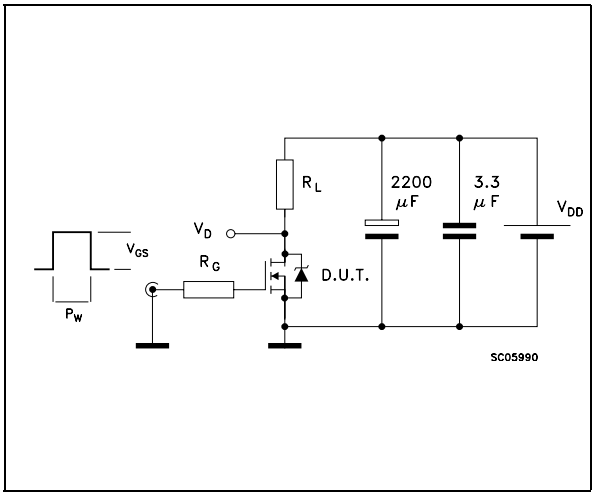


Figure 16: Test Circuit For Diode Recovery Times

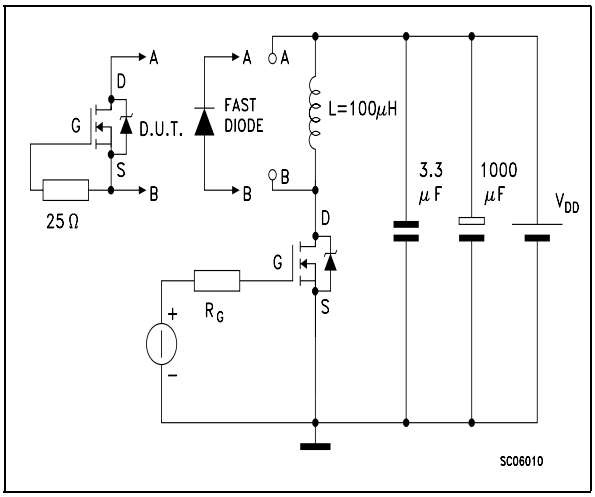
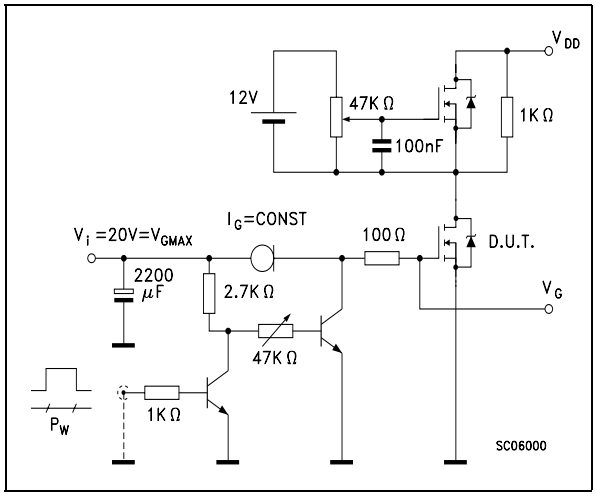


Figure 17: Gate Charge Test Circuit



SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					

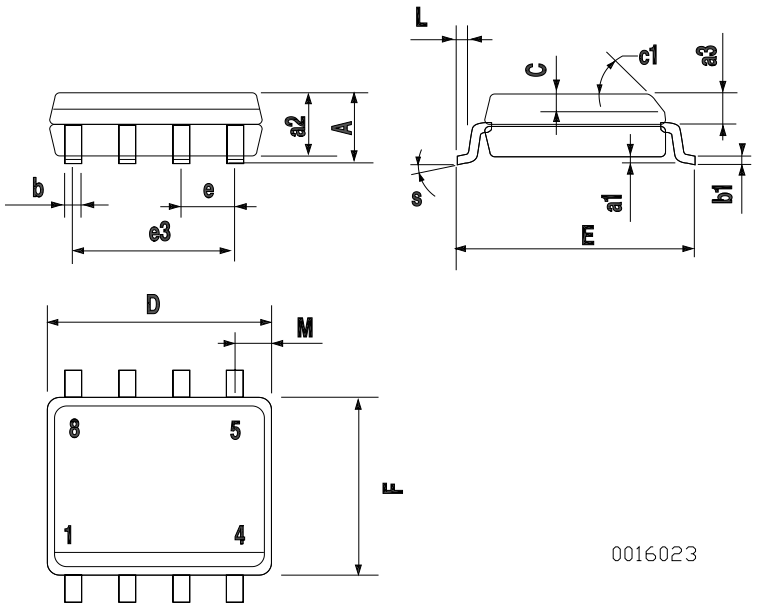


Table 11: Revision History

Date	Revision	Description of Changes
24-May-2005	1	First release
19-Dec-2005	2	Inserted curves