

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 8×8-bit digital multiplier integrated circuit, unsigned magnitude data format.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	ADSP-1081ASD/883B
-2	ADSP-1081ATD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-40A.

1.3 Absolute Maximum Ratings.

Supply Voltage	-0.3 V to 7 V
Input Voltage	-0.3 V to V_{DD}
Output Voltage	-0.3 V to V_{DD}
Operating Temperature Range (Ambient)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

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Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	-1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	-1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = -1.0 mA	V min
Digital Output Low Voltage*	V _{OL}	-1, 2	0.4	0.6	0.6			V _{DD} = min I _{OL} = +4.0 mA	V max
Digital Input High Current	I _{IH}	-1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	-1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	-1, 2	50	50	50			V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	-1, 2	50	50	50			V _{DD} = max V _{IH} = 0 V (High Z)	μA max
Supply Current*	I _{DD1}	-1, 2	45	55	55			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	-1, 2	30	35	35			V _{DD} = max All V _{IN} = 2.4 V	
Output Delay	t _D	-1, 2	25			30	30	Note 2	ns max
Three-State Enable* (High Z to High or Low)	t _{ENA}	-1, 2	20			25	25	Notes 2 and 3	ns max
Three-State Disable* (High or Low to High Z)	t _{DIS}	-1, 2	20			25	25	Notes 2 and 3	ns max
Input Setup Time	t _S	-1, 2	20			20	20	Note 2	ns min
Clock Pulse Width	t _{PW}	-1, 2	15			15	15	Note 2	ns min
Input Hold Time	t _H	-1, 2	2			3	3	Note 2	ns min
Multiply Time*	t _{MC}	-1	45			55	55	Note 2	ns max
		-2	33			45	45		

NOTES

*Indicates that a limit for this parameter has changed from REV. A.

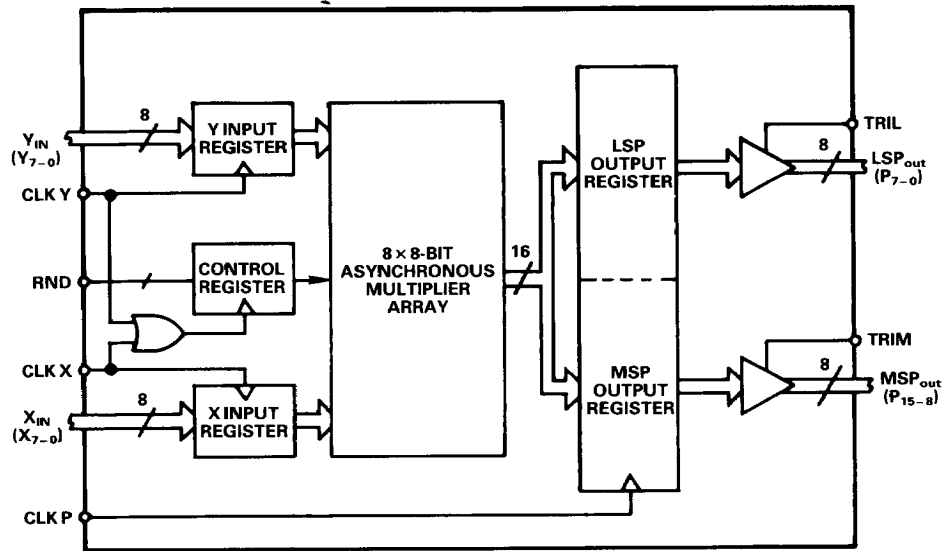
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	P10	21	X6
2	P9	22	X7 (MSB)
3	P8	23	CLK X
4	CLK P	24	CLK Y
5	TRIM	25	RND
6	TRIL	26	Y0
7	P7	27	Y1
8	P6	28	Y2
9	P5	29	Y3
10	P4	30	V _{DD}
11	P3	31	Y4
12	P2	32	GND
13	P1	33	Y5
14	P0	34	Y6
15	X0	35	Y7 (MSB)
16	X1	36	P15 (MSB)
17	X2	37	P14
18	X3	38	P13
19	X4	39	P12
20	X5	40	P11

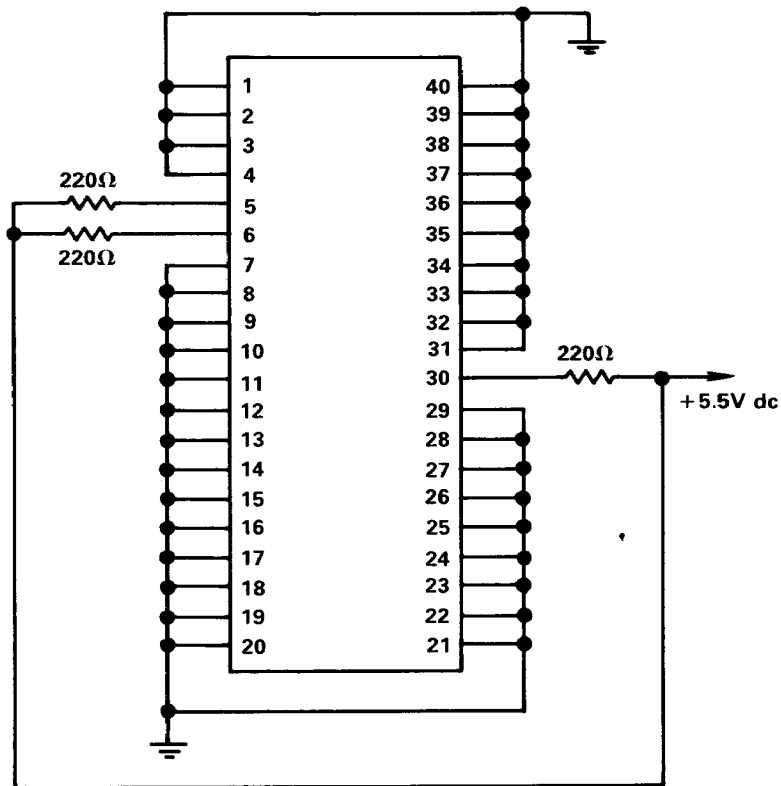
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

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4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1081AD Life Test and Burn-In Circuit

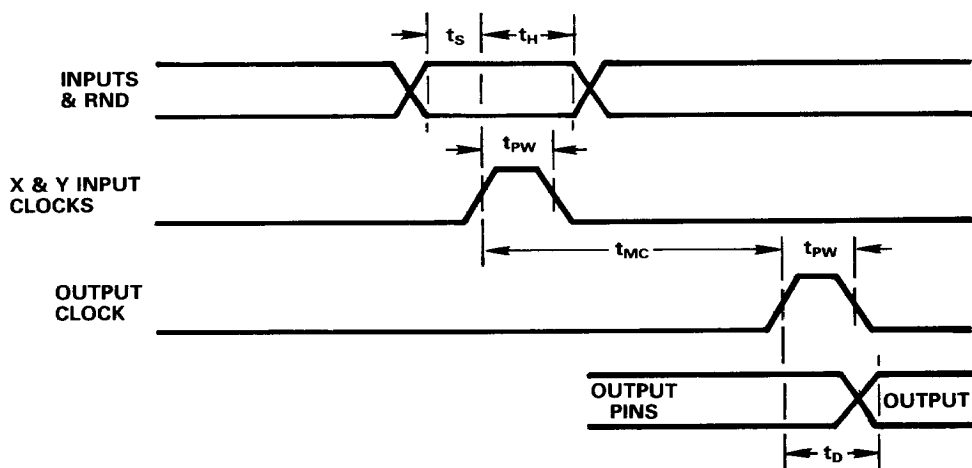


Figure 1. ADSP-1081A Timing Diagram

REV. B

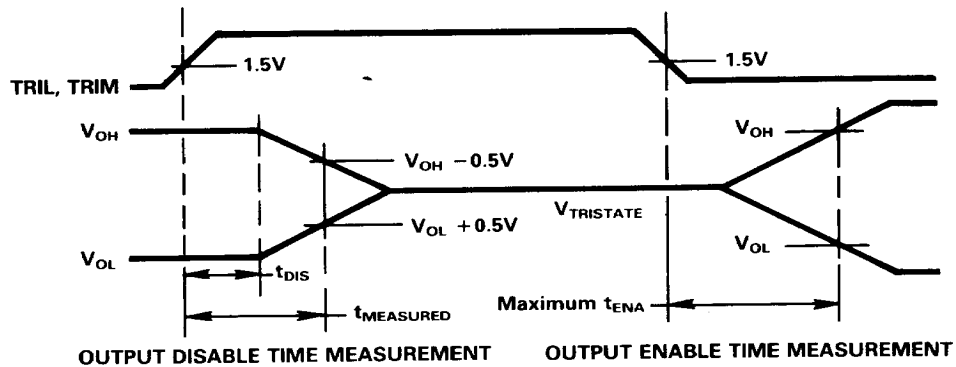


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 \text{ V}}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

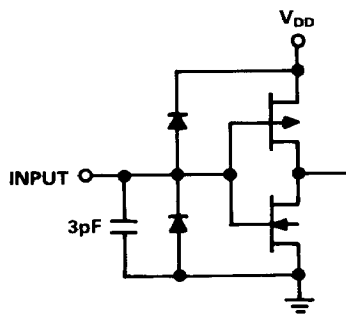


Figure 3. Equivalent Input Circuit

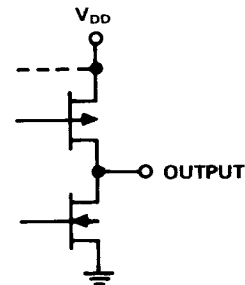


Figure 4. Equivalent Output Circuit

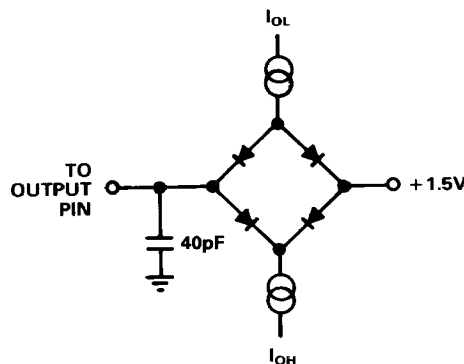


Figure 5. Normal Load Circuit for AC Measurements

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X & Y INPUT DATA FORMAT								OUTPUT DATA FORMATS															
								MSP (P ₁₅₋₈)								LSP (P ₇₋₀)							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNSIGNED FRACTIONAL																							
2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶
UNSIGNED INTEGER																							
2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰

Table 2. Data Formats