COM'L

AmPAL22P10B/AL/A

24-Pin Combinatorial TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As fast as 15 ns maximum propagation delay**
- **Universal combinatorial architecture**
- **Programmable output polarity**
- **Programmable replacement for high-speed TTL logic**
- **Extensive third–party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The AmPAL22P10 utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The AmPAL22P10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

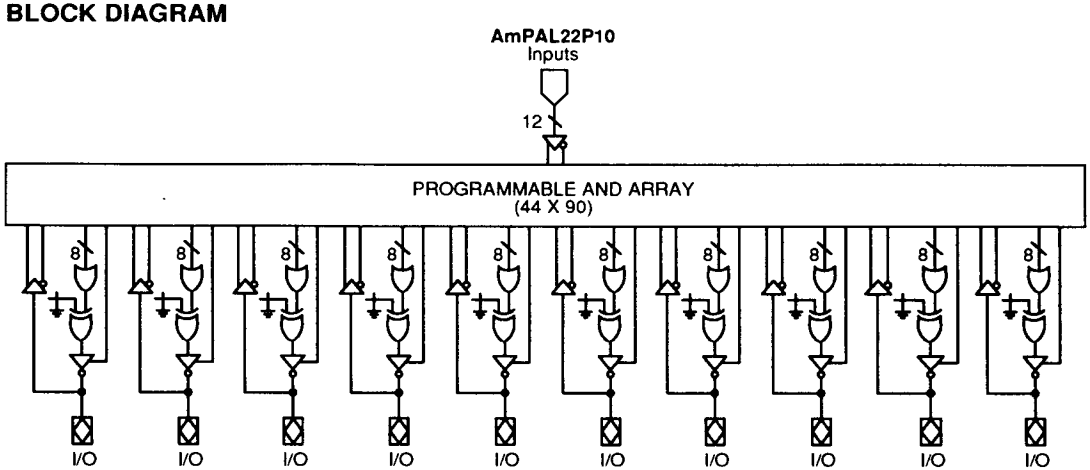
The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the FusionPLD partners. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

BLOCK DIAGRAM



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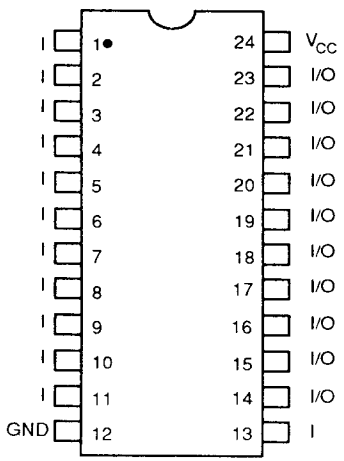
PRODUCT SELECTOR GUIDE

Family	t_{PD} ns (Max.)	I_{CC} mA (Max.)	I_{OL} mA (Min.)
Very High Speed ("B") Versions	15	210	24
High Speed ("A") Versions	25	210	24
High Speed, Half Power ("AL") Versions	25	105	24

CONNECTION DIAGRAMS
Top View

SKINNYDIP



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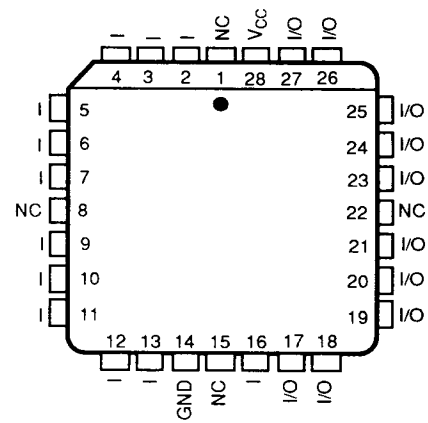
PLCC



Note:
Pin 1 is marked for orientation

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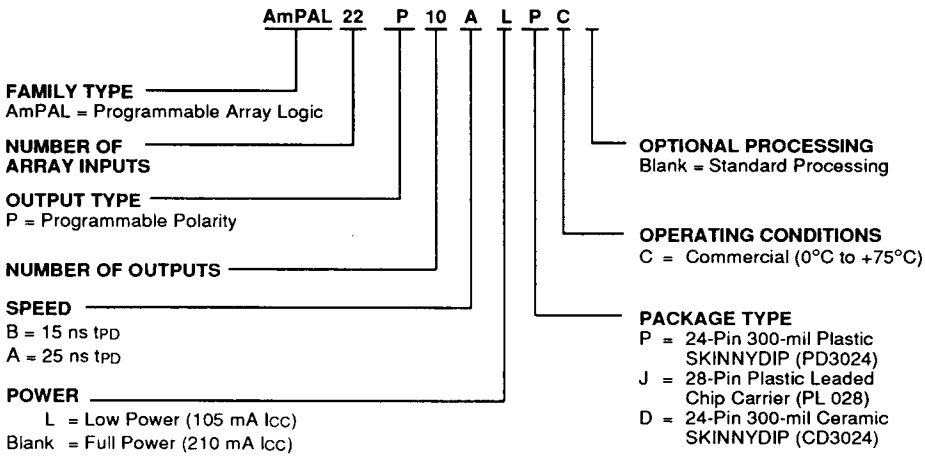
PIN DESIGNATIONS

GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
Vcc	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
AmPAL22P10	B, AL, A	PC, JC, DC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The AmPAL22P10 has twelve dedicated input lines, and all ten combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Polarity

The polarity of each output can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts. Selection is through a programmable fuse which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if the fuse is 1 (programmed) and active low if the fuse is 0 (intact).

Security Fuse

After programming and verification, an AmPAL22P10 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

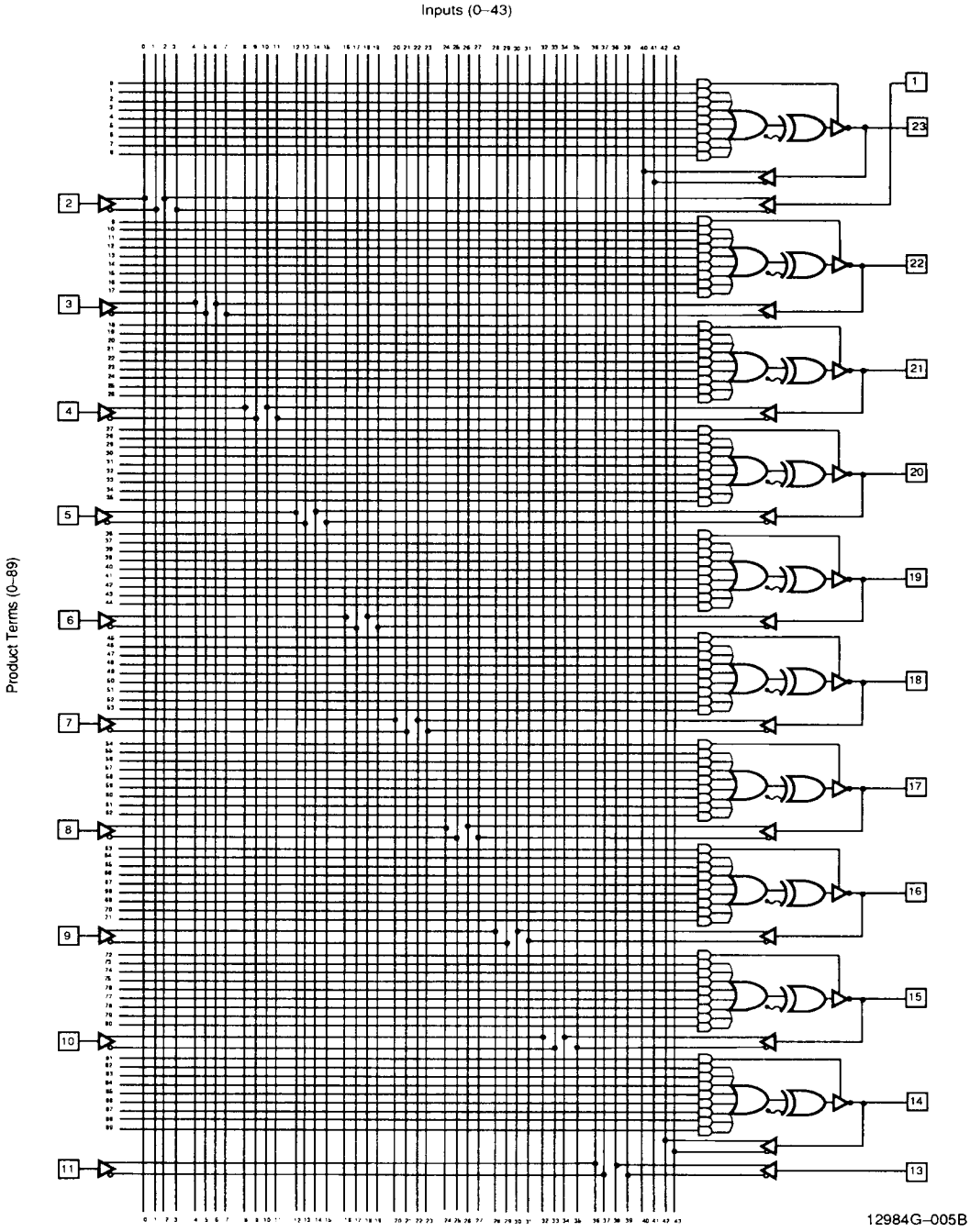
The AmPAL22P10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The AmPAL22P10 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for reliable operation.

LOGIC DIAGRAM

AmPAL22P10



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature With Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to +5.5 V
DC Input Current	−30 mA to +5 mA
DC I/O Pin Voltage	−0.5 V to V_{CC} Max.
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.			−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			−100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		−30	−90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	B, A		210	mA
			AL		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V	11	pF
		Others		T_A = +25°C	6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

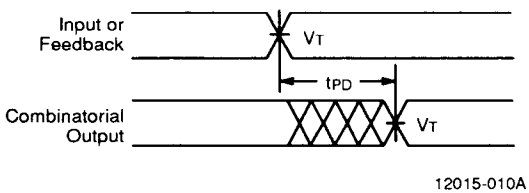
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	B		A, AL		Unit
		Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output		15		25	ns
t_{EA}	Input to Output Enable Using Product Term Control		18		25	ns
t_{ER}	Input to Output Disable Using Product Term Control		15		25	ns

Note:

2. See Switching Test Circuit for test conditions.

SWITCHING WAVEFORMS



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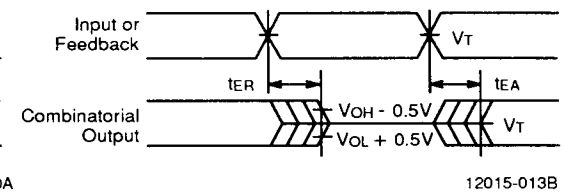
Combinatorial Output



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Input to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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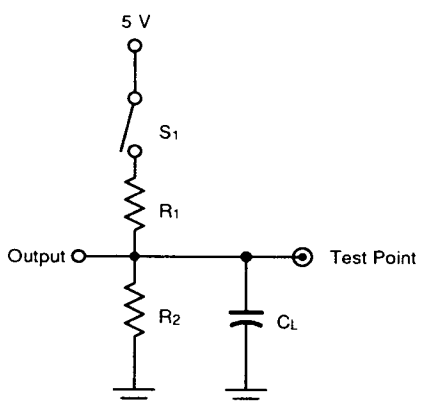
SWITCHING TEST CIRCUIT



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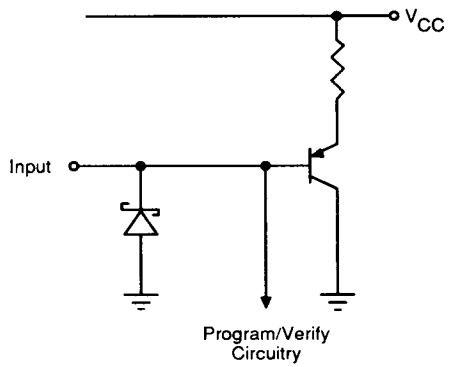
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



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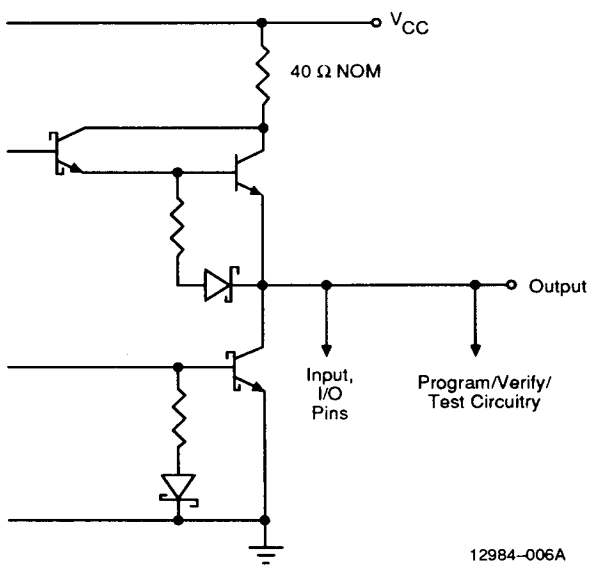
Typical Output



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