SONY

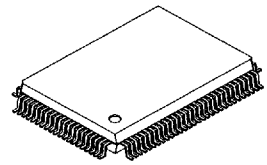
CXD1812Q/R

ATAPI I/F CD-ROM DECODER

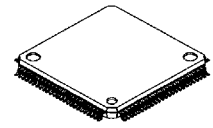
Description

The CXD1812Q/R is a CD-ROM decoder LSI with a built-in ATAPI I/F.

CXD1812Q
100 pin QFP (Plastic)



CXD1812R
100 pin LQFP (Plastic)



Features

- Compatible with CD-ROM, CD-I and CD-ROM XA formats
- Real time error correction
- Automatic multi-block transfer function
- Readable Subcode-Q data by byte from the Sub CPU
- Capable of transferring up to double speed playback and Mode2 when the 33.8688 MHz clock is used
  Transfer in Mode3 is possible when the decoder is OFF (The transfer speed depends on playback speed and clock frequency.)
- Supports PIO/single-word DMA/multiword DMA data transfer mode
- IORDY support available
- Automatic reception of PACKET commands

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	−0.5 to +7.0	V
• Input voltage	V_I	−0.5 to V_{DD} +0.5	V
• Output voltage	V_O	−0.5 to V_{DD} +0.5	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5 (+5.0 typ.)	V
• Operating temperature	Topr	−20 to +75	°C

Applications

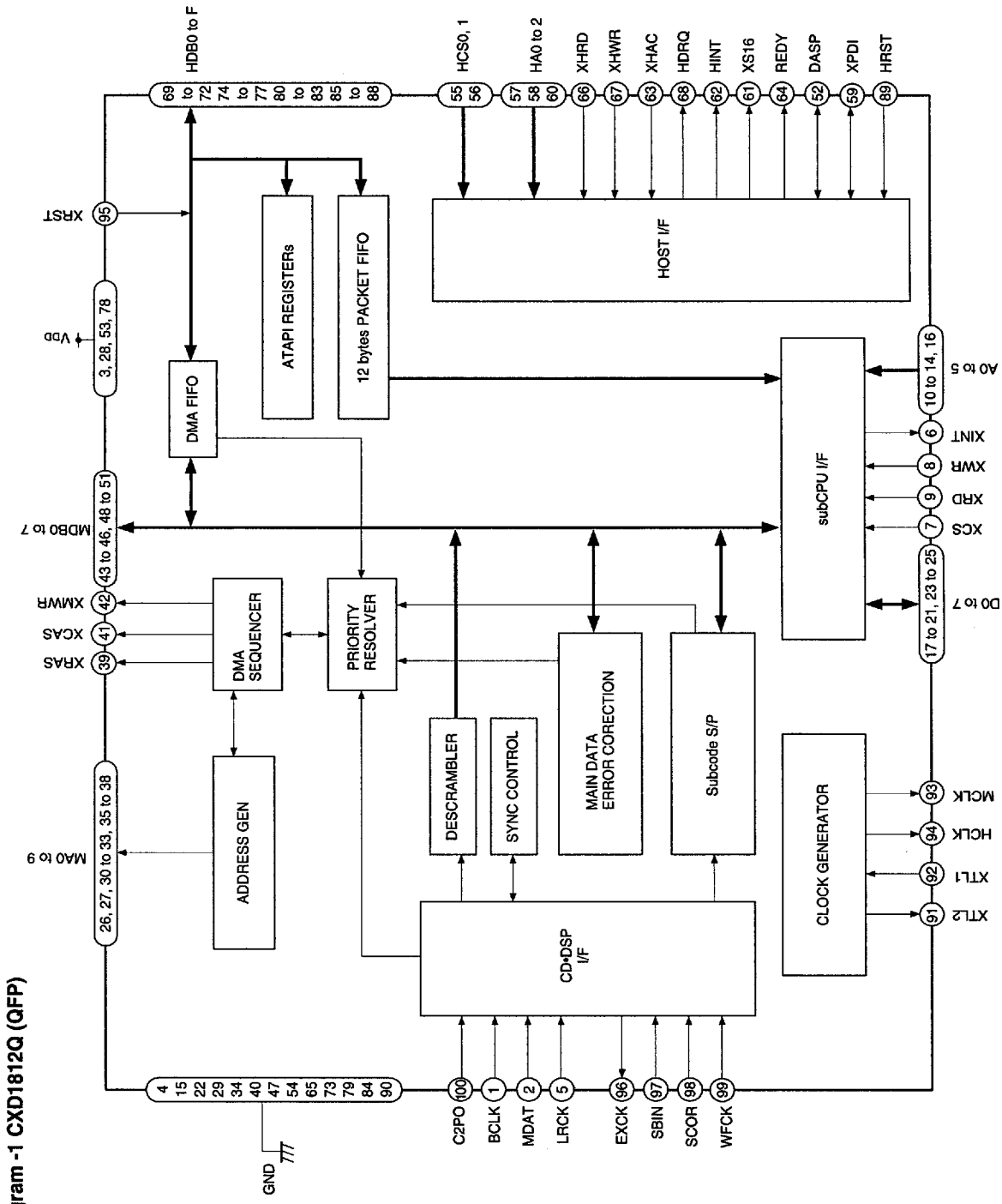
CD-ROM drives

Structure

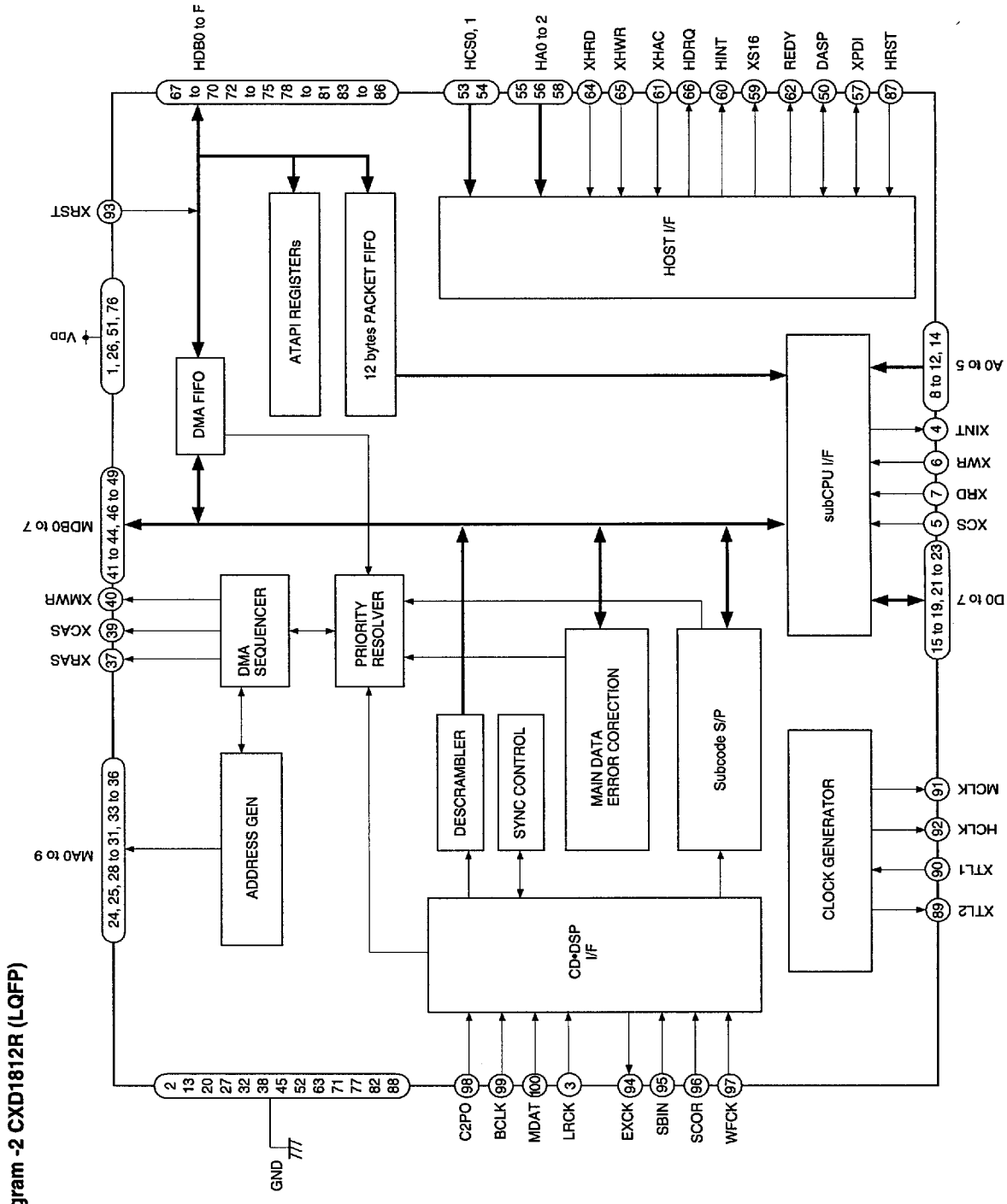
Silicon gate CMOS IC

E95233-ST

Block Diagram -1 CXD1812Q (QFP)



Block Diagram -2 CXD1812R (LQFP)



Pin Description

Pin No.		Symbol	I/O	Description
QFP	LQFP			
1	99	BCLK	I	Bit clock signal from CD DSP
2	100	MDAT	I	Data signal from CD DSP
3	1	V_{DD}	—	Power supply
4	2	GND	—	Ground
5	3	LRCK	I	LR clock signal from CD DSP
6	4	XINT	O	Interrupt request signal to CPU
7	5	XCS	I	Chip select negative logic signal from CPU
8	6	XWR	I	Strobe negative logic signal for writing data from CPU
9	7	XRD	I	Strobe negative logic signal for reading data from CPU
10	8	A5	I	CPU address (MSB)
11	9	A4	I	CPU address
12	10	A3	I	CPU address
13	11	A2	I	CPU address
14	12	A1	I	CPU address
15	13	GND	—	Ground
16	14	A0	I	CPU address (LSB)
17	15	D7	I/O	CPU data bus (MSB)
18	16	D6	I/O	CPU data bus
19	17	D5	I/O	CPU data bus
20	18	D4	I/O	CPU data bus
21	19	D3	I/O	CPU data bus
22	20	GND	—	Ground
23	21	D2	I/O	CPU data bus
24	22	D1	I/O	CPU data bus
25	23	D0	I/O	CPU data bus (LSB)
26	24	MA0	O	DRAM address (LSB)
27	25	MA1	O	DRAM address
28	26	V_{DD}	—	Power supply
29	27	GND	—	Ground
30	28	MA2	O	DRAM address
31	29	MA3	O	DRAM address
32	30	MA4	O	DRAM address
33	31	MA5	O	DRAM address
34	32	GND	—	Ground
35	33	MA6	O	DRAM address
36	34	MA7	O	DRAM address

Pin No.		Symbol	I/O	Description
QFP	LQFP			
37	35	MA8	O	DRAM address
38	36	MA9	O	DRAM address (MSB)
39	37	XRAS	O	DRAM row address strobe negative logic signal
40	38	GND	—	Ground
41	39	XCAS	O	DRAM column address strobe negative logic signal
42	40	XMWR	O	DRAM write enable negative logic signal
43	41	MDB0	I/O	DRAM data bus (LSB)
44	42	MDB1	I/O	DRAM data bus
45	43	MDB2	I/O	DRAM data bus
46	44	MDB3	I/O	DRAM data bus
47	45	GND	—	Ground
48	46	MDB4	I/O	DRAM data bus
49	47	MDB5	I/O	DRAM data bus
50	48	MDB6	I/O	DRAM data bus
51	49	MDB7	I/O	DRAM data bus (MSB)
52	50	DASP	I/O	Drive active/slave present negative logic signal; open drain output
53	51	V_{DD}	—	Power supply
54	52	GND	—	Ground
55	53	HCS1	I	Chip select negative logic signal from host
56	54	HCS0	I	Chip select negative logic signal from host
57	55	HA2	I	Host address (MSB)
58	56	HA0	I	Host address (LSB)
59	57	XPDI	I/O	Passed diagnostics negative logic signal; open drain output
60	58	HA1	I	Host address
61	59	XS16	O	16-bit I/O port select negative logic signal; open drain output
62	60	HINT	O	Interrupt request positive logic signal to host
63	61	XHAC	I	DMA acknowledge negative logic signal from host
64	62	REDY	O	I/O channel ready positive logic signal; open drain output
65	63	GND	—	Ground
66	64	XHRD	I	Strobe negative logic signal for reading data from host
67	65	XHWR	I	Strobe negative logic signal for writing data from host
68	66	HDRQ	O	DMA request positive logic signal to host
69	67	HDBF	I/O	Host data bus (MSB)
70	68	HDB0	I/O	Host data bus (LSB)
71	69	HDBE	I/O	Host data bus
72	70	HDB1	I/O	Host data bus

Pin NO.		Symbol	I/O	Description
QFP	LQFP			
73	71	GND	—	Ground
74	72	HDBD	I/O	Host data bus
75	73	HDB2	I/O	Host data bus
76	74	HDBC	I/O	Host data bus
77	75	HDB3	I/O	Host data bus
78	76	V_{DD}	—	Power supply
79	77	GND	—	Ground
80	78	HDBB	I/O	Host data bus
81	79	HDB4	I/O	Host data bus
82	80	HDBA	I/O	Host data bus
83	81	HDB5	I/O	Host data bus
84	82	GND	—	Ground
85	83	HDB9	I/O	Host data bus
86	84	HDB6	I/O	Host data bus
87	85	HDB8	I/O	Host data bus
88	86	HDB7	I/O	Host data bus
89	87	HRST	I	Chip reset negative logic signal from host
90	88	GND	—	Ground
91	89	XTL2	O	Crystal oscillation circuit output
92	90	XTL1	I	Crystal oscillation circuit input
93	91	MCLK	O	Master clock (XTL1) output
94	92	HCLK	O	Clock output with 1/2 the frequency of XTL1
95	93	XRST	I	Chip reset negative logic signal
96	94	EXCK	O	Subcode data read clock signal to CD DSP
97	95	SBIN	I	Subcode data serial input signal from CD DSP
98	96	SCOR	I	Subcode sync positive logic signal from CD DSP
99	97	WFCK	I	Write frame clock signal from CD DSP
100	98	C2PO	I	C2 pointer positive logic signal from CD DSP

Electrical Characteristics

1. DC Characteristics

(V_{DD} = 5V ±10%, V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		2.2			V
Low level input voltage (1)	V_{IL1}				0.8	V
High level input voltage (2)	V_{IH2}		0.7V_{DD}			V
Low level input voltage (2)	V_{IL2}				0.3V_{DD}	V
High level input voltage (3)	V_{t1+}		2.2			V
Low level input voltage (3)	V_{t1-}				0.8	V
TTL Schmitt hysteresis	$V_{t1+} - V_{t1-}$			0.4		V
High level input voltage (4)	V_{t2+}		0.8V_{DD}			V
Low level input voltage (4)	V_{t2-}				0.2V_{DD}	V
CMOS Schmitt hysteresis	$V_{t2+} - V_{t2-}$			0.6		V
High level output voltage (6)	V_{OH1}	I_{OH1} = –2mA	V_{DD} – 0.8			V
Low level output voltage (6)	V_{OL1}	I_{OL1} = 4mA			0.4	V
High level output voltage (7)	V_{OH2}	I_{OH2} = –6mA	V_{DD} – 0.8			V
Low level output voltage (7)	V_{OL2}	I_{OL2} = 12mA			0.4	V
High level output voltage (8)	V_{OH3}	I_{OH3} = –6mA	V_{DD} – 0.8			V
Low level output voltage (8)	V_{OL3}	I_{OL3} = 4mA			0.4	V
Input leakage current	I_{IL1}		–10		10	µA
Input leakage current*1	I_{IL2}		–40		40	µA
Input current of pull-up input	I_{IL3}	V_{IN} = 0V	–40	–100	–240	µA
Input current of pull-up input*1	I_{IL4}	V_{IN} = 0V	–90	–200	–440	µA
Output leakage current (9) (10)	I_{IZ}	High-impedance state	–40		40	µA
Oscillation cell logic threshold value	LVth			0.5V_{DD}		V
Oscillation cell high level input voltage	V_{IH}		0.7V_{DD}			V
Oscillation cell low level input voltage	V_{IL}				0.3V_{DD}	V
Oscillation cell feedback resistance	R_{FB}	V_{IN} = V_{SS} or V_{DD}	250k	1M	2.5M	Ω
Oscillation cell high level output voltage	V_{OH}	I_{OH} = –12mA	0.5V_{DD}			V
Oscillation cell low level output voltage	V_{OL}	I_{OL} = 12mA			0.5V_{DD}	V

*1 Bidirectional pin

1-1. Categories of input pins

(1) TTL input level pin:
D0 to D7, MDB0 to MDB7, HDB0 to HDBF, DASP, XPDI

(2) CMOS input level pin:
MDAT, LRCK, SBIN, SCOR, WFCK, C2PO

(3) TTL Schmitt input level pin:
XCS, XWR, XRD, A0 to A5, HA0 to HA2, XHAC, XHRD, XHWR, HCS0 to HCS1, HRST

(4) CMOS Schmitt input level pin:
BCLK, XRST

(5) Input pin with pull-up resistor:
D0 to D7, MDB0 to MDB7, HCS0 to HCS1, HRST

1-2. Categories of output pins

(6) Normal output pin:
D0 to D7, MDB0 to MDB7, XINT, MA0 to MA9, XMWR, MCLK, HCLK, EXCK

(7) Powered output pin:
HINT, HDRQ, HDB0 to HDBF, DASP, XPDI, XS16, REDY

(8) Proportional output pin:
XRAS, XCAS

(9) Tristate output pin:
XINT, HINT, HDRQ

(10) Open drain output pin:
DASP, XPDI, XS16, REDY

1-3. Bidirectional pins

D0 to D7, MDB0 to MDB7, HDB0 to HDBF, DASP, XPDI

1-4. Oscillation cell

Input: XTL1
Output: XTL2

1-5. I/O Capacitance

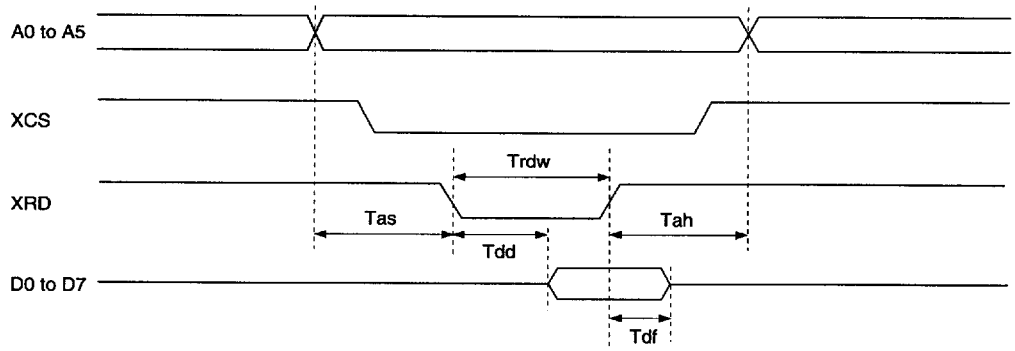
(V_{DD} = V_I = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}			9	pF
Output capacitance	C_{OUT}			11	pF
I/O capacitance	$C_{I/O}$			11	pF

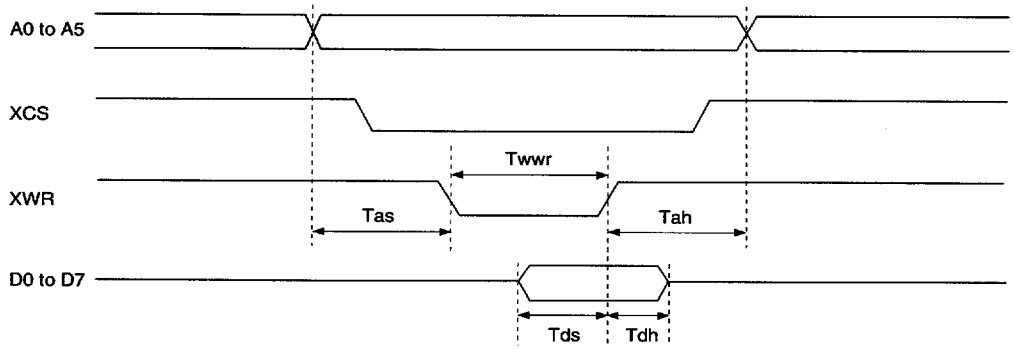
2. AC Characteristics (V_{DD} = 5V ±10%, V_{SS} = 0V, Topr = –20 to +75°C, Output Load = 50pF)

2-1. CPU Interface

(1) Read



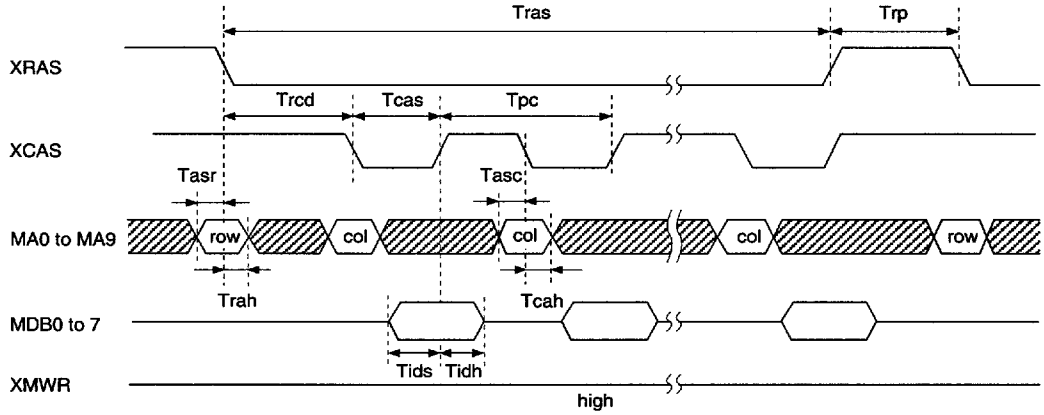
(2) Write



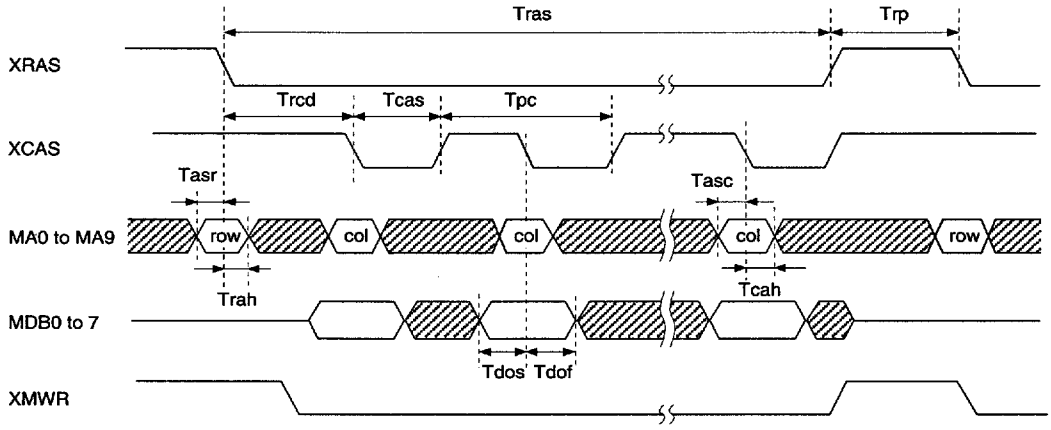
Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XCS & XRD/XWR ↓)	Tas	0			ns
Address hold time (for XCS & XRD/XWR ↑)	Tah	0			ns
XRD pulse width	Trdw	43			ns
Data delay time (for XCS & XRD ↓)	Tdd			43	ns
Data float time (for XCS & XRD ↑)	Tdf	1			ns
XWR pulse width	Twwr	21			ns
Address setup time (for XCS & XWR ↑)	Tds	7			ns
Address hold time (for XCS & XWR ↑)	Tdh	0			ns

2-2. DRAM Interface

(1) Read



(2) Write

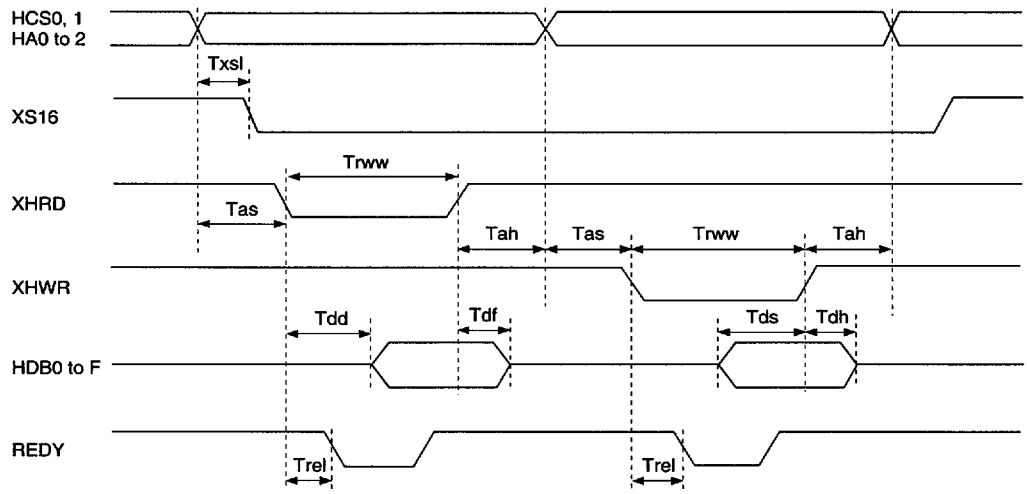


(Tw = 1/f)

Item	Symbol	Min.	Typ.	Max.	Unit
RAS pulse width	Tras	3Tw			ns
RAS precharge width	Trp		2Tw		ns
RAS – CAS delay time	Trcd		2Tw		ns
CAS pulse width	Tcas		Tw		ns
Page mode cycle time	Tpc		2Tw		ns
Row address setup time (for RAS ↓)	Tasr	Tw – 7			ns
Row address hold time (for RAS ↓)	Trah	Tw			ns
Column address setup time (for CAS ↓)	Tasc	Tw – 14			ns
Column address hold time (for CAS ↓)	Tcah	Tw + 2			ns
Input data setup time (for CAS ↑)	Tids	7			ns
Input data hold time (for CAS ↑)	Tidh	0			ns
Data output setup time (for CAS ↓)	Tdos	0			ns
Data output float time (for CAS ↓)	Tdof	Tw + 3			ns

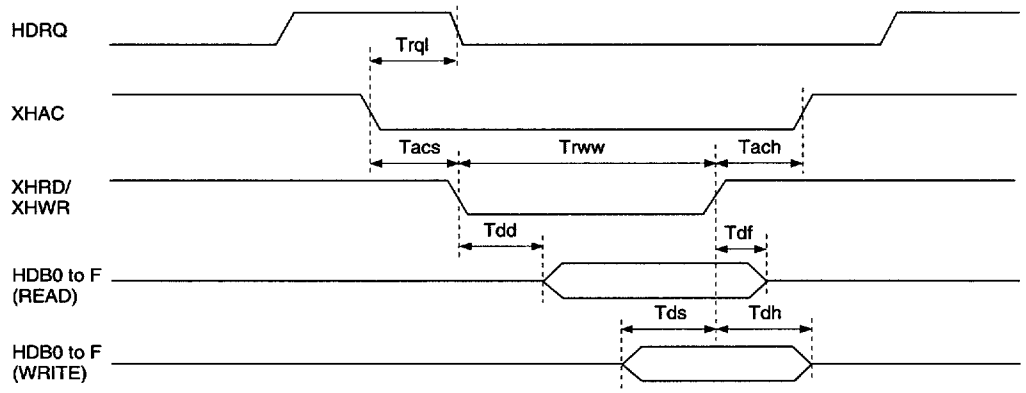
2-3. HOST Interface

(1) PIO

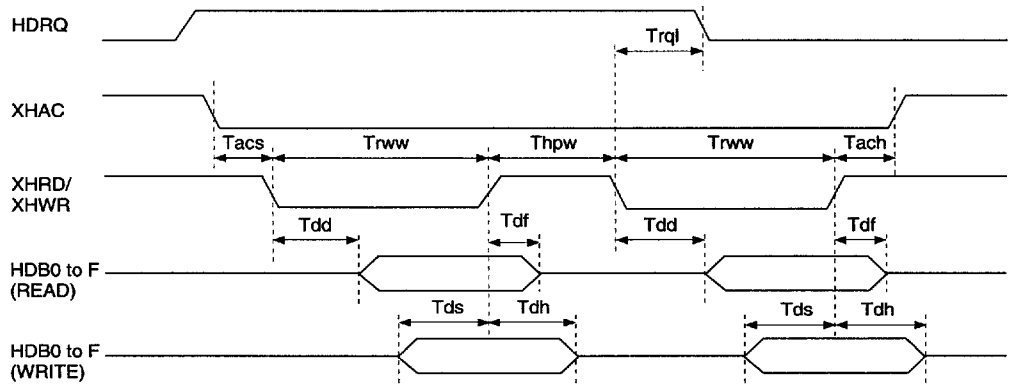


Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XHRD/XHWR ↓)	Tas	20			ns
Address hold time (for XHRD/XHWR ↑)	Tah	5			ns
XHRD/XHWR pulse width	Trww	50			ns
Data delay time (for XHRD ↓)	Tdd			26	ns
Data float time (for XHRD ↑)	Tdf	5		21	ns
Data setup time (for XHWR ↑)	Tds	20			ns
Data hold time (for XHWR ↑)	Tdh	5			ns
XS16 fall time (for Address valid)	Txsl			8	ns
REDY fall time (for XHRD/XHWR ↓)	Trel			14	ns

(2) Single-word DMA



(3) Multiword DMA

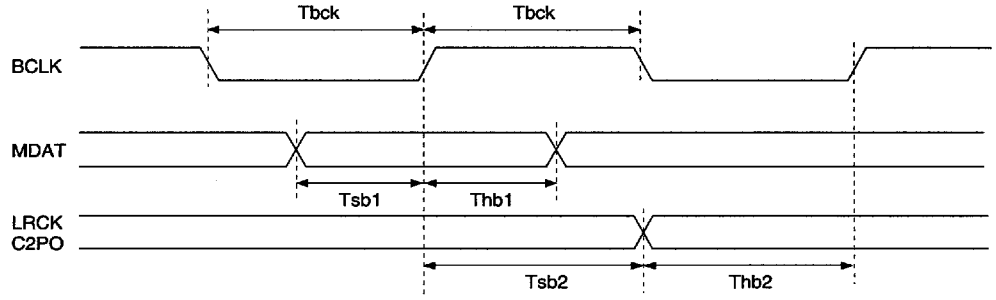


(Tw = 1/f)

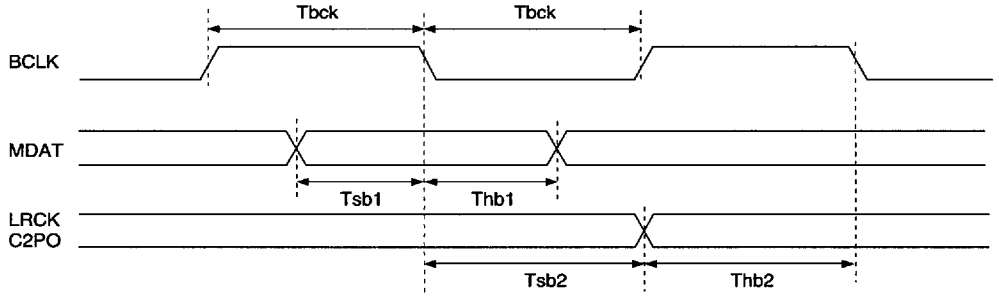
Item	Symbol	Min.	Typ.	Max.	Unit
HDRQ fall time (for XHAC/XHRD/XHWR ↓)	Trql			Tw +11	ns
XHRD/XHWR Low pulse width	Trww	50			ns
Data delay time (for XHRD ↓)	Tdd			26	ns
Data float time (for XHRD ↑)	Tdf	5		19	ns
Data setup time (for XHWR ↑)	Tds	20			ns
Data hold time (for XHWR ↑)	Tdh	5			ns
XHAC setup time (for XHRD/XHWR ↓)	Tacs	0			ns
XHAC hold time (for XHRD/XHWR ↑)	Tach	0			ns
XHRD/XHWR high pulse width	Thpw	25			ns

2-4. CD DSP Interface

(1) BCKRED = "H"

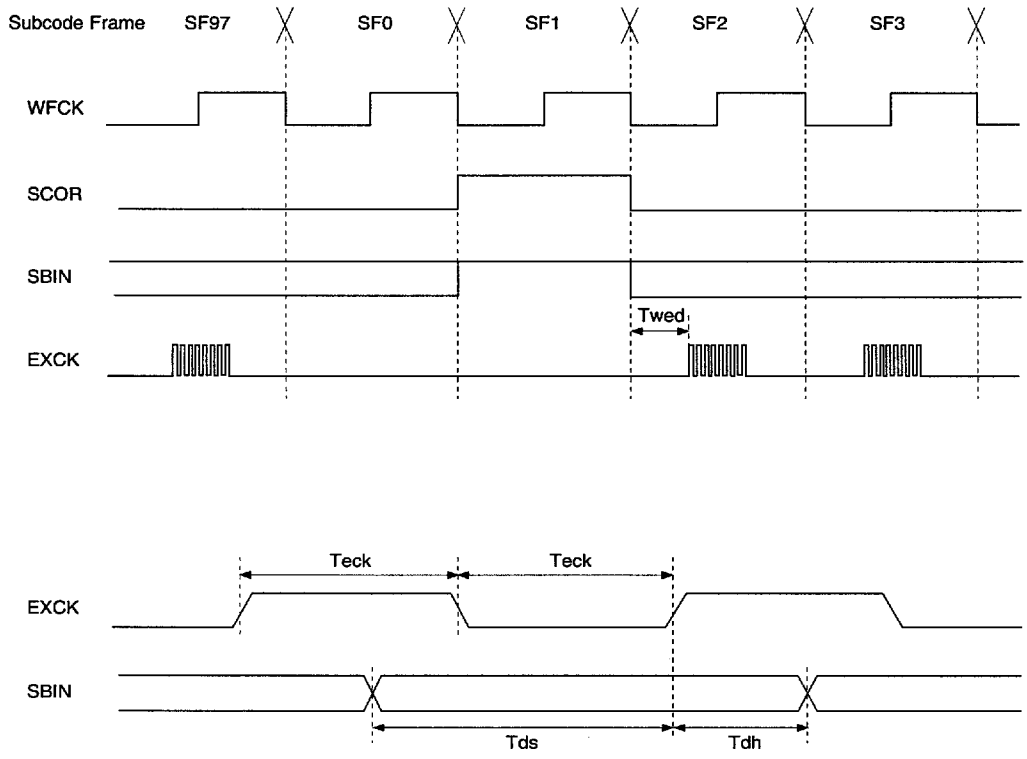


(2) BCKRED = "L"



Item	Symbol	Min.	Typ.	Max.	Unit
BCLK frequency	Fbck			20	MHz
BCLK pulse width	Tbck	25			ns
MDAT setup time (for BCLK)	Tsb1	12			ns
MDAT hold time (for BCLK)	Thb1	12			ns
LRCK, C2PO setup time (for BCLK)	Tsb2	12			ns
LRCK, C2PO hold time (for BCLK)	Thb2	12			ns

2-5. Subcode Interface



(Tw = 1/f)

Item	Symbol	Min.	Typ.	Max.	Unit
WFCK – EXCK delay time	Twed	2aTw		3aTw	ns
EXCK pulse width	Teck	1/2aTw – 2			ns
SBIN setup time (for EXCK ↑)	Tds	12			ns
SBIN hold time (for EXCK ↑)	Tdh	12			ns

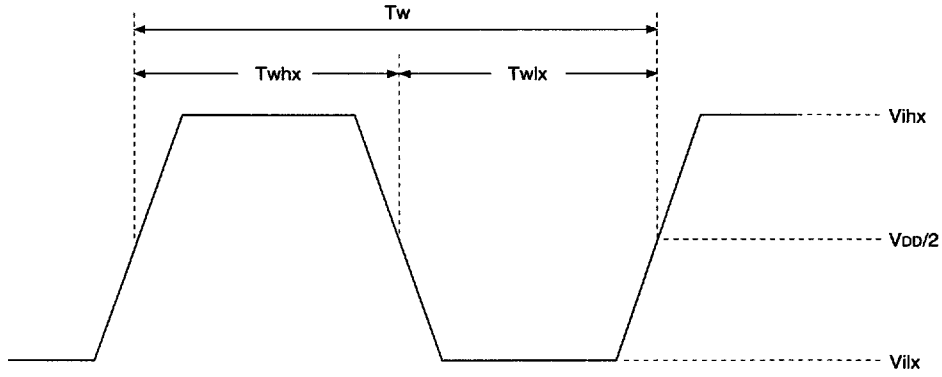
a = 48: When EXCKSL (CONFIG0 register bit 3) = High
a = 32: When EXCKSL (CONFIG0 register bit 3) = Low

2-6. XTL1 and XTL2 Pins

(1) When using self-excited oscillation

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f		33.8688	40	MHz

(2) When inputting a pulse to the XTL1 pin



Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	Twhx	10			ns
Low level pulse width	Twlx	10			ns
Pulse cycle	Tw		29		ns

Description of Functions

1. Pin Description

The pin description by function is given below.

1-1. CD player interface (8 pins)

This enables direct connection with the Sony's digital signal processor LSI for CD players. Digital signal processor LSI for CD applications are hereafter called "CD DSP."

(1) MDAT (medium data: input)
Serial data stream from CD DSP.

(2) BCLK (bit clock: input)
Bit clock signal; MDAT signal strobe.

(3) LRCK (LR clock: input)
LR clock signal; indicates left and right channels of MDAT signals.

(4) C2PO (C2 pointer: input)
C2 pointer signal; indicates that an error is contained in MDAT input.

(5) WFCK (write frame clock: input)
Write frame clock input signal.

(6) SCOR (subcode sync OR: input)
Subcode sync signal.

(7) SBIN (subcode serial input: input)
Subcode serial signal.

(8) EXCK (external clock: output)
Clock output for reading SBIN signals.

1-2. Buffer memory interface (21 pins)

This can be connected with up to a 512K-byte DRAM (4M bits).

(1) XMWR (DRAM write enable: output)
DRAM write enable negative logic output signal.

(2) XCAS (column address strobe: output)
Negative logic output signal to indicate that column addresses are valid.

(3) XRAS (row address strobe: output)
Negative logic output signal to indicate that row addresses are valid.

(4) MA0 to MA9 (DRAM address: output)
DRAM address output.

(5) MDB0 to MDB7 (DRAM data bus: input/output)
DRAM data bus signal; pulled up by a standard 25kΩ resistor.

1-3. Sub CPU interface (18 pins)

(1) XWR (sub CPU write: input)
Strobe negative logic signal for writing internal registers.

(2) XRD (sub CPU read: input)
Strobe negative logic signal for reading internal registers status.

(3) D0 to D7 (sub CPU data bus: input/output)
8-bit data bus; pulled up by a standard 25kΩ resistor.

(4) A0 to A5 (sub CPU address: input)
Address signal for selecting internal registers from sub CPU.

(5) XINT (sub CPU interrupt: output)
Interrupt request signal to sub CPU. Polarity can be controlled by sub CPU.

(6) XCS (chip select: input)
Chip select negative logic signal from sub CPU.

1-4. HOST interface (31 pins)

(1) HCS0 (host chip select: input)
Chip select negative logic signal from host; pulled up by a standard 50kΩ resistor. This is connected with the CS1FX pin of ATAPI I/F.

(2) HCS1 (host chip select: input)
Chip select negative logic signal from host; pulled up by a standard 50kΩ resistor. This is connected with the CS3FX pin of ATAPI I/F.

(3) HA0 to HA2 (host address: input)
Address signal for selecting internal registers from host.

(4) DASP (drive active/slave present: input/output)
Negative logic signal to indicate that slave drive is present or drive is active; open drain signal.

(5) HDB0 to HDBF (host data bus: input/output)
16-bit host data bus signal.

(6) XHRD (host read: input)
Data read strobe negative logic signal from host.

(7) XHWR (host write: input)
Data write strobe negative logic signal from host.

(8) XHAC (host DMA acknowledge: input)
DMA data request acknowledge negative logic signal from host.

(9) HDRQ (host DMA request: output)
DMA data request positive logic signal to host; tristate output.

(10) HINT (host interrupt: output)
Interrupt request positive logic signal to host; tristate output.

(11) XS16 (16-bit data transfer: output)
Negative logic signal to indicate that the 16-bit data port has been selected; open drain signal. This is connected with the IOCS16 pin of ATAPI I/F.

(12) REDY (I/O channel ready: output)
Positive logic signal to be negated when the drive is not ready to respond to a data transfer reguest; open drain signal. This is connected with the IORDY pin of ATAPI I/F.

(13) XPDI (passed diagnostics: input/output)
Negative logic signal that indicates diagnostics of the slave drive has been completed; open drain signal. This is connected with the PDIAG pin of ATAPI I/F.

(14) HRST (host reset: input)
Reset negative logic signal from host; pulled up by a standard 50kΩ resistor.

1-5. Others (5 pins)

(1) XRST (reset: input)
Chip reset negative logic input signal.

(2) XTL1 (crystal 1: input)

(3) XTL2 (crystal 2: output)
A crystal oscillator is connected between XTL1 and XTL2. (The capacitor value depends on the crystal oscillator.)

(4) MCLK (clock: output)
Outputs a clock signal of the same frequency as that of XTL1. The output can be set at low when this clock signal is not used.

(5) HCLK (half clock: output)
Outputs a clock signal with 1/2 the frequency of XTL1. The output can be set at low when this signal is not used.

1-6. Power supply (17 pins)

V_{DD}: 4 pins, GND: 13 pins.

2. Sub CPU Write Registers

Normally set at low for reserved registers and bits.

2-1. CONFIG0 (configuration 0) register (address 00HEX)

bit 7: CINTPOL (sub CPU interrupt polarity)
- High: The XINT pin becomes high-active. When the register is inactive, the low state is established.
- Low: The XINT pin becomes low-active. When the register is inactive, high impedance is established.

bit 6: M/S SEL (master/slave select)
This bit is valid only when M/S EN (bit 5) is high.
- High: Set this bit high when a slave drive is used.
- Low: Set this bit low when a master drive is used.

bit 5: M/S EN (master/slave mode enable)
Set this bit as follows according to the number of drives connected to ATAPI I/F.
- High: Set this bit high when two drives are connected to ATAPI I/F. One is used as the master drive and the other is the slave drive.
- Low: Set this bit low when only one drive is connected to ATAPI I/F.

bit 4: RESERVED

bit 3: EXCKSL (EXCK select)
The frequency of EXCK clock signal for picking up subcodes from CD DSP is determined by this bit. The sub CPU sets this register according to the clock frequency and the playback speed of the XTL1 pin. (Max. frequency of EXCK clock signal is 1MHz.)
- High: The EXCK frequency is 1/48 the frequency of XTL1. When the frequency of the XTL1 pin is more than 32MHz, this bit is set high.
- Low: The EXCK frequency is determined to be 1/32 the frequency of XTL1. When the frequency of the XTL1 pin is not more than 32MHz, this bit is set low.

bit 2: DISMCLK (disable MCLK output)
- High: The MCLK pin is fixed at low.
- Low: The clock signal of the same frequency as that of the XTL1 pin is output from the MCLK pin.

bit 1: DISHCLK (disable HCLK output)
- High: HCLK pin is fixed at low.
- Low: The frequency divider clock signal of half the frequency of XTL1 pin is output from HCLK pin.

bit 0: RAMSIZE (RAM size)
- High: When a 4M-bit DRAM is connected, set this bit high.
- Low: When a DRAM of up to 2M bits is connected, set this bit low.

2-2. CONFIG1 (configuration 1) register (address 01HEX)

bit 7: SWOPEN (sync window open)
- High: A window for Sync mark detection is opened. In this case, the internal Sync protection circuit is disabled.
- Low: A window for Sync mark detection is controlled by the internal Sync protection circuit.

bit 6 to 4: SYCNGC2 to 0 (sync NG count 2 to 0)
Set "010" for these bits.

bit 3: RESERVED

bit 2, 1: RFRSCTL1, 0 (refresh control 1, 0)
The refresh interval of the DRAM can be controlled by these bits. Set these bits according to the clock frequency of XTL1. The refresh interval is designed as 512 cycle/8ms.

RFRSCTL1	RFRSCTL0	
"L"	"L"	XTL1 frequency: less than 24MHz
"L"	"H"	XTL1 frequency: 24MHz or more
"H"	"L"	XTL1 frequency: 32MHz or more
"H"	"H"	XTL1 frequency: 33.8688MHz or more

bit0 RESERVED

2-3. LSTARA (last area) register (address 02HEX)

The last area is assigned by this register.
The following table shows the set values of LASTARA when the buffer memory is fully used.

ENBYTFBT	RAM size	LASTARAHEX
"L"	32KB	0C
"H"		0A
"L"	64KB	19
"H"		16
"L"	128KB	34
"H"		2E
"L"	256KB	69
"H"		5E
"L"	512KB	D3
"H"		BD

2-4. LHADR (last HADRC) register (address 03HEX)

Assigns the upper limit (upper 8 bits) of HADRC when the automatic transfer mode to the host is disabled, or the upper limit (upper 8 bits) of the address when the row subcode buffering command is executed. The lower 11 bits are assigned to 7FFHEX.

2-5. DRVIF (drive interface) register (address 04HEX)

This register controls the connection mode with the CD DSP. After the IC is reset, the sub CPU sets this register according to the CD DSP to be connected.
Any change of each bit in this register must be made in the decoder disable status. (After the IC is reset, the address is set 28HEX.)
Figs. 1-1 and 1-2 are input timing charts for Sony's typical CD DSP.

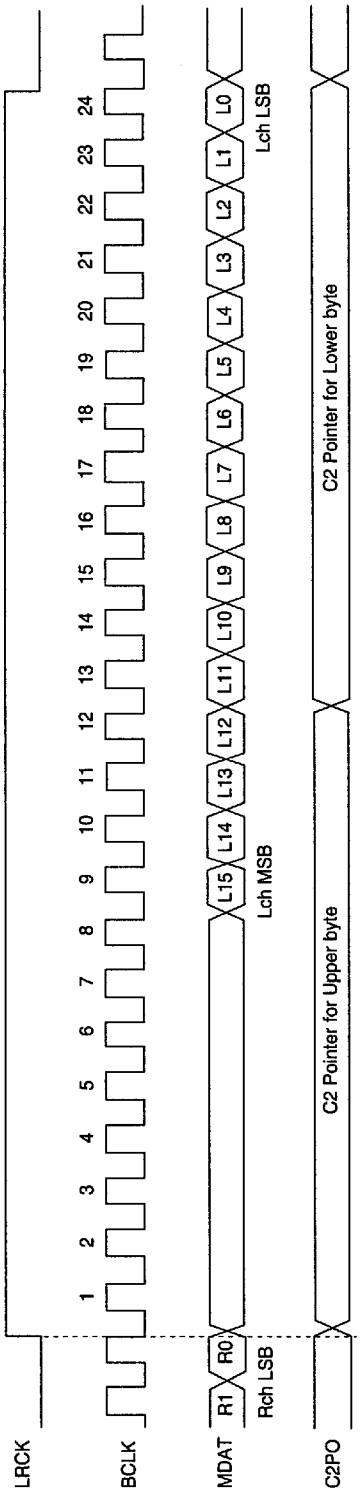


Fig. 1-1. CDL40 and 50 Series Timing Chart (48-bit slot mode)

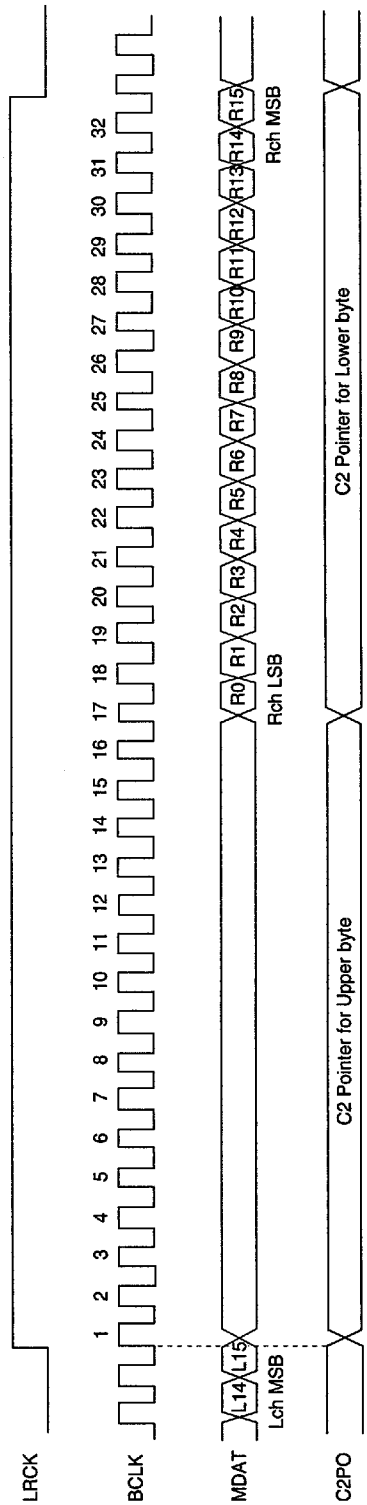


Fig. 1-2. CDL40 and 50 Series Timing Chart (64-bit slot mode)

bit 7: C2PL1ST (C2PO lower byte first)
High: When 2 bytes of MDAT are input, C2PO inputs the lower byte first followed by the upper byte.
Low: When 2 bytes of MDAT are input, C2PO inputs the upper byte first followed by the lower byte.
Here, "upper byte" means the upper 8 bits including MSB from the CD DSP and "lower byte" means the lower 8 bits including LSB from the CD DSP. For example, the Header minute byte is the lower byte and the second byte, the upper byte.

bit 6: LCHLOW (Lch low)
High: When LRCK is low, determined to be the left channel data.
Low: When LRCK is high, determined to be the left channel data.

bit 5: BCKRED (BCLK rising edge)
High: MDAT is strobed at the rising edge of BCLK.
Low: MDAT is strobed at the falling edge of BCLK.

bit 4, 3: BCKMD1, 0 (BCLK mode 1, 0)
These bits are set according to the number of clocks output for BCLK during one WCLK cycle by the CD DSP.

BCKMD1	BCKMD0	
"L"	"L"	16BCLKs/WCLK
"L"	"H"	24BCLKs/WCLK
"H"	"X"	32BCLKs/WCLK

bit 2: LSB1ST (LSB first)
High: Connected with the CD DSP which outputs MDAT with LSB first.
Low: Connected with the CD DSP which outputs MDAT with MSB first.

bit 1, 0: RESERVED

2-6. XFRFMT0 (transfer format 0) register (address 05HEX)

The transfer format for automatic data transfer is determined by this register. This IC transfers the buffer memory data to the host according to the Mode/Form value written by SCTINF register (address 1EHEX) into the internal RAM by sector and the values of XFRFMT1 and 0 registers.
The Mode/Form of bits 3 to 1 depends on the values of bits 2 and 1 of SCTINF register.
Regarding Mode 2 in Yellow Book, don't care the Form2 (bit 2) of SCTINF register.
Set bits 3 to 1 of XFRFMT0 register high to transfer 2336 bytes of user data.

bit 7, 6: RESERVED

bit 5: SYNC
High: The Sync mark is transferred to the host.
Low: The Sync mark is not transferred to the host.

bit 4: HEADER
High: The Header's 4 bytes are transferred to the host.
Low: The Header's 4 bytes are not transferred to the host.

bit 3: SUBHEADER
High: Mode1: This bit has no meaning.
Mode 2: The Sub Header's 8 bytes are transferred to the host.
Low: The bytes above are not transferred to the host.

bit 2: USERDATA (user data)
High: Mode1 and Mode2/Form1: User data (2048 bytes) are transferred to the host.
Mode2/Form2: User data (2324 bytes) are transferred to the host.
Low: The bytes above are not transferred to the host.
bit 1: PARITY
High: Mode1: The EDC, ECC parity and eight 00HEX bytes, for a total of 288 bytes, are transferred to the host.
Mode2/Form1: The EDC and ECC parity (280 bytes) are transferred to the host.
Mode2/Form2: RESERVED bytes (4 bytes) (the final ones in the sector concerned) are transferred to the host.
Low: The bytes above are not transferred to the host.
bit 0: RESERVED

Regarding CD-DA data, set bits 5 to 1 high.

2-7. XFRFMT1 (transfer format 1) register (address 06HEX)

bit 7: ENBLKEFL (enable block error flag)
High: Block error flag (1 byte + 00HEX) is transferred to the host.
Here, block error flag means operating OR by bit of the byte error flag.
Low: The bytes above are not transferred to the host.
bit 6: RESERVED
bit 5: ENBYTFBT (enable byte error flag buffering and transfer)
When this bit is set high, the following operations are performed. When this bit is set low, the following operations are not performed. This bit is valid only when the USERDATA bit (bit 2) of XFRFMT0 register is set high.
(1) When write-only, real-time correction, or CD-DA command is being executed, byte error flag is buffered.
(2) When the automatic transfer mode to the host is enabled (that is, the AUTOXFR bit of XFRCTL register (bit 7) is high), byte error flag is transferred to the host.
bit 4: RESERVED
bit 3: ENSBCBT (enable subcode buffering and transfer)
When this bit is set high, the following operations are performed. When this bit is set low, the following operations are not performed.
(1) When CD-DA command is being executed, all the subcodes or the subcode-Q are buffered.
(2) When the automatic transfer mode to the host is enabled (that is, the AUTOXFR bit of XFRCTL register (bit 7) is high), all the subcodes or the subcode-Q are transferred to the host.
bit 2: ALLSBC (all subcodes/subcode-Q)
When ENSBCBT is set high, whether all the subcodes or the subcode-Q are to be buffered or transferred to the host is determined.
High: All the subcodes
Low: Subcode-Q
bit 1: RESERVED
bit 0: ZASUBQ (zero after sub-Q)
This bit is valid only when ENSBCBT is high and ALLSBC is low.
High: 6-byte 00HEX in addition to the subcode-Q are transferred to the host.
Low: 2-byte CRC and 4-byte 00HEX in addition to the subcode-Q are transferred to the host.

2-8. DECCTL0 (decoder control 0) register (address 07HEX)

bit 7: AUTODIST (auto distinction)

High: Errors are corrected according to the Mode byte and the Form bit read by the drive.

Low: Errors are corrected according to the MODESEL and FORMSEL bits (bits 6 and 5).

bit 6: MODESEL (mode select)

bit 5: FORMSEL (form select)

When AUTODIST is set low, the sector is corrected in the Mode or Form indicated below.

MODESEL	FORMSEL	
"L"	"L"	MODE1
"H"	"L"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

bit 4: RESERVED

bit 3: ENFM2EDC (enable form 2 EDC check)

High: EDC check for Form2 is enabled.

Low: EDC check for Form2 is disabled. The EDCNG bit of DECSTS0 register is set low.

bit 2: MDBYTCTL (mode byte control)

High: Even if there are data other than 0 in the upper 6 bits of the Header's Mode byte, it is not determined to be an error. Set this bit high when a CD-DA command is executed or the disc such as CD-R is played back.

Low: If the upper 6 bits of the Header's Mode byte are not "000000," it is determined to be an error.

bit 1: ENDLA (enable drive last area (address))

High: DLAR (drive last area)/SLADR (subcode last address) is enabled. When buffering of the buffer memory area assigned by DLAR is completed while the decoder is executing the write-only, real-time correction, or CD-DA command, the DRVOVRN (drive over run) status is established. When buffering to the address assigned by SLADR is completed while the subcode buffering command is being executed, the DRVOVRN status is established. In the DRVOVRN status,data writing into the buffer is stopped.

Low: DLAR (drive last area)/SLADR (subcode last address) is disabled.

bit 0: ATDLRNEW (Auto DLARA renewal)

High: When the data transfer to host is completed for one sector, DLARA is renewed in the written area of the sector.

Low: Renewal of DLARA is executed by the sub CPU.

2-9. DECCTL1 (decoder control 1) register (address 08HEX)

bit 7: ENSBQRD (enable subcode-Q read)

CRC of subcode-Q is checked by taking in the subcode from DSP. Sub CPU can read subcode-Q data from the SUBQ register.

bit 6: RESERVED

bit 5 to 3: DECCMD2 to 0 (decoder commands 2 to 0)

DECCMD2	DECCMD1	DECCMD0	Decoder command
"L"	"L"	"L"	Decoder disable
"L"	"L"	"H"	Monitor only
"L"	"H"	"L"	Write only
"L"	"H"	"H"	Real-time correction
"H"	"L"	"H"	Raw subcode buffer
"H"	"H"	"H"	CD-DA

bit 2 to 0: RESERVED

2-10. XFRMOD (transfer mode) register (address 09HEX)

bit 7: ENHINTCT (enable auto HINT upon start of packet command transfer)

High: When packet command transfer starts, there is an interrupt request to the host.

Low: When the transfer above starts, there is no interrupt request to the host.

bit 6: ENHINTDT (enable auto HINT upon start of data transfer)

High: When data transfer with the host starts, there is an interrupt request to the host.

Low: When the transfer above starts, there is no interrupt request to the host.

bit 5: ENMDMA (enable multiword DMA)

This bit is valid for DMA transfer.

High: DMA transfer is executed in the multiword mode.

Low: DMA transfer is executed in the single-word mode.

bit 4: ENDMABIT (enable ATAPI feature register DMA bit)

bit 3: PIOSEL (PIO transfer mode select)

Transfer mode is determined as shown below from the combination of these bits and the DMA bit (bit 0) of ATAPI feature register.

PIOSEL	ENDMABIT	DMA	Transfer Mode
"H"	"X"	"X"	PIO
"L"	"H"	"H"	DMA
"L"	"H"	"L"	PIO
"L"	"L"	"X"	DMA

bit 2: AUTOWAIT (enable auto wait state)

This bit is valid for PIO transfer.

High: In the cases below, the REDY pin is set low and a wait is automatically applied to the host.

Transfer to host: When the host asserts the XHRD signal while the data FIFO is empty.

Transfer from host: When the host asserts the XHWR signal while the data FIFO is full.

Low: The wait state above does not occur.

bit 1, 0: WAITCYCL1, 0

These bits are valid for PIO transfer.

If the host asserts XHRD/XHWR during data transfer, the REDY pin is set low by the cycle number set with these bits, and a wait is applied. One cycle is XTL1 cycle.

00: Wait state does not occur.

01: Wait state of 4 to 8 cycles occurs.

10: Wait state of 8 to 12 cycles occurs.

11: Wait state of 12 to 16 cycles occurs.

2-11. XFRCTL0 (transfer control 0) register (address 0AHEX)

bit 7: AUTOXFR (auto transfer)

High: The automatic transfer mode to the host described later is enabled.

Low: The automatic transfer mode to the host above is disabled. Transfer to the host is executed by setting HADRC and HXFRC.

bit 6 to 4: RESERVED

bit 3: CPUDMAEN (sub CPU DMA enable)

The buffer memory access by sub CPU is enabled by setting this bit high. The sub CPU sets this bit high after the head addresses of buffer access have been set on the CADRC.

bit 2: CPUSRC (sub CPU source)

High: Data are transferred from sub CPU to buffer memory.

Low: Data are transferred from buffer memory to sub CPU.

bit 1 to 0: RESERVED

2-12. XFRCTL1 (transfer control 1) register (address 0BHEX)

bit 7: PFIFOCL (packet FIFO clear)

When this bit is set high, the packet FIFO is cleared. This bit is automatically set low after FIFO has been cleared.

bit 6: RESERVED

bit 5: AUTOEND (enable auto transfer termination)

The following settings are automatically made upon completion of data transfer.

High: ATAPI status register - bit 7/bit 6/bit 3: BUSY/DRDY/DRQ = Low/High/Low

ATAPI interrupt reason register - bit 1/bit 0: IO/CoD = High/High

Interrupt request signal to host: HINT = High

Low: ATAPI status register - bit 7/bit 3: BUSY/DRQ = High/Low

Interrupt request signal to host: HINT = Low

bit 4: HSTXFREN (host transfer enable)

When this bit is set high, transfer starts between the host and buffer memory. This bit is automatically set low when transfer is completed.

The following settings are automatically operated by setting this bit high.

ATAPI status register -bit 3: DRQ = High

ATAPI status register -bit 7: BUSY = Low (in the PIO mode)

bit 3, 2: RESERVED

bit 1: IO (host transfer direction)
To set this bit, the ATAPI status register -bit 7: BUSY bit must be high.
High: Data are transferred from the buffer memory to the host.
Low: Data are transferred from the host to the buffer memory.

bit 0: CoD (command or data)
To set this bit, the ATAPI status register -bit 7: BUSY bit must be high.
High: Indicates that data transferred are Command.
Low: Indicates that the data transferred are user data.

2-13. RESERVED (address 0CHEX)

2-14. CHPCTL0 (chip control 0) register (address 0DHEX)

bit 7: CHIPRST (chip reset)
This IC is reset by setting this bit high.

bit 6: TGTMET (target met)
(1) If the target sector is found while the write-only or real-time correction command is being executed, the sub CPU sets TGTMET high.
(2) TGTMET bit is sampled at the 3/4 sector (variable depending on playback speed) after the decoder interrupt. Therefore, if the target sector has been found, the sub CPU must set the TGTMET bit high within this time after DECINT.
(3) Once the TGTMET bit is set high, the high state is held until the decoder is disabled.
(4) When the sampled TGTMET is low, while write-only or real-time correction is executed,
•the buffering area of main data or subcode is not renewed.
• main data are not corrected.

bit 5: INCTGT (increment target register)
When this bit is set high, TARGET registers (TGTMIN, TGTSEC, TGTBLK) are incremented. TARGET registers use the BCD code.
TGTMIN, TGTSEC, and TGTBLK are connected in cascading fashion, and are incremented as follows:
(1) The TGTBLK register value is always incremented by this bit. The address number 0 follows 74.
(2) The TGTSEC register value is incremented when this bit is high while the TGTBLK register value is 74. The address number 0 follows 59.
(3) The TGTMIN register value is incremented when this bit is high, while the TGTBLK register value is 74 and the TGTSEC register value 59. The address number 0 follows 99.

bit 4: RPCORTRG (repeat correction trigger)
When this bit is set high with the decoder disabled, error correction for the CD-ROM sector starts. The sector to be corrected is assigned by the BFARA# register.

bit 3 to 0: RESERVED

2-15. CHPCTL1 (chip control 1) register (address 0EHEX)

bit 7 to 3: RESERVED

bit 2: DASP (DASP pin control)
When this bit is set high, the DASP signal is asserted.

bit 1: PDIAG (XPDI pin control)
When this bit is set high, the XPDI signal is asserted.

bit 0: CLRHINT (clear HINT)
HINT is cleared by setting this bit high. This bit is automatically set low when HINT has been cleared.

2-16. Diskette change/drive address register (address 0FHEX)

bit 7: RESERVED

bit 6 to 2: Optional values can be set by sub CPU.
These values can be read from bits 6 to 2 of the diskette change/drive address register of the host.

bit 1 to 0: RESERVED

2-17. ATAPI error register (address 10HEX)

This register corresponds to the ATAPI error register of the host. The sub CPU can set any optional values.

bit 7 to 4: SENSE KEY

bit 3: MCR (Media Change Requested)

bit 2: ABRT (Aborted Command)

bit 1: EOM (End Of Media Detected)

bit 0: ILI (Illegal Length Indication)

2-18. ATAPI feature register (address 11HEX)

This register corresponds to the ATAPI feature register of the host.
The sub CPU can set any optional values in this register when the ATAPI status register -bit 7: BUSY bit is high.

bit 0: DMA

2-19. ATAPI interrupt reason register (address 12HEX)

This register corresponds to the ATAPI interrupt reason register of the host.
The sub CPU can set any optional values in this register when the ATAPI status register -bit 7: BUSY bit is high.

bit 1: IO
This bit is equivalent to the XFRCTL1 (address 0BHEX) register -bit 1.

bit 0: CoD
This bit is equivalent to the XFRCTL1 (address 0BHEX) register -bit 0.

2-20. ATA sector number register (address 13HEX)

This register corresponds to the ATA sector number register of the host.
The sub CPU can set any optional values in this register when the ATAPI status register -bit 7: BUSY bit is high.

2-21. ATAPI byte count high/low register (address 14, 15HEX)

This register corresponds to the ATAPI byte count high/low register of the host.
The number of bytes to be transferred is set.
The sub CPU can set any optional values in this register when the ATAPI status register -bit 7: BUSY bit is high.

2-22. ATAPI drive select register (address 16HEX)

This register corresponds to the ATAPI drive select register of the host.
The sub CPU can set any optional values in this register when the ATAPI status register -bit 7: BUSY bit is high.

bit 4: DRV

2-23. ATA command register (address 17HEX)

This register corresponds to the ATA command register of the host.
The sub CPU can set any optional values in this register when the ATAPI status register -bit 7: BUSY bit is high. However, the ATAPI soft reset command (08HEX) can be set regardless of the value of the BUSY bit.

2-24. RESERVED (address 18HEX)

2-25. ATAPI status 1 register (address 19HEX)

bit 7, 6: RESERVED

bit 5: DRDY1 (drive 1 ready)
This bit corresponds to the ATAPI status register -bit 6: DRDY bit of the host.
The DRDY status of the slave drive is set.

bit 4: DSC1 (drive 1 seek complete)
This bit corresponds to the ATAPI status register -bit 4: DSC bit of the host.
The DSC status of the slave drive is set.

bit 3: HST5
This bit corresponds to the ATAPI status register -bit 5 of the host.

bit 2: HST1
This bit corresponds to the ATAPI status register -bit 1 of the host.

bit 1: DRDY0 (drive 0 ready)
This bit corresponds to the ATAPI status register -bit 6: DRDY bit of the host. The DRDY status of the master drive is set.

bit 0: DSC0 (drive 0 seek complete)
This bit corresponds to the ATAPI status register -bit 4: DSC bit of the host.
The DSC status of the master drive is set.

2-26. ATAPI status 2/drive control register (address 1AHEX)

bit 7: BUSY
This bit corresponds to the ATAPI status register -bit 7 of the host.
This bit must be set high when the sub CPU accesses the group of command block registers.

bit 6: RESERVED

bit 5: CORR
This bit corresponds to the ATAPI status register -bit 2 of the host.

bit 4: ENHINT (enable HINT)
An interrupt to the host can be made by setting this bit high.

bit 3 to 1: RESERVED

bit 0: CHECK
This bit corresponds to the ATAPI status register -bit 0 of the host.

2-27. UNLOCK (release lock mode) register (address 1BHEX)

The bits 5 to 0 of ATAPI status 1 register (address 19HEX), the bits 1 and 0 of XFRCTL1 register (address 0BHEX), and ATAPI interrupt reason register (address 12HEX) are locked in the cases below, making setting from sub CPU impossible.

- When an ATAPI packet command (A0HEX) is detected.
- When data transfer with the host is completed while the XFRCTL1 register (address 0BHEX) bit 5: AUTOEND is high.

The sub CPU can release the lock mode above by accessing this register.

2-28. CPUBWDT (CPU buffer write data) register (address 1CHEX)

The sub CPU writes data to be written in the buffer memory into this register.

2-29. RESERVED (address 1DHEX)

2-30. SCTINF (sector information) register (address 1EHEX)

The current sector information is written into this register at DECINT. For automatic transfer of information to the host, make sure this register is set for each DECINT. The value of this register is written into the internal RAM.

bit 7 to 3: RESERVED

bit 2: Mode2

High: This sector is in Mode2.

Low: This sector is in Mode1 or CD-DA.

bit 1: Form2

This bit is valid only when the Mode2 bit is high.

High: This sector is in Form2.

Low: This sector is in Form1.

Both low and high are available for this bit in the Mode2 for Yellow Book.

MODE2	FORM2	
"L"	"L"	MODE1
"H"	"L"	MODE2/FORM1
"H"	"H"	MODE2/FORM2
"L"	"X"	CD-DA

bit 0: RESERVED

2-31. RESERVED register (address 1F, 20HEX)

2-32. TGTMIN (target minute) register (address 21HEX)

0 to 99

2-33. TGTSEC (target sector) register (address 22HEX)

0 to 59

2-34. TGTBLK (target block) register (address 23HEX)

0 to 74

When the monitor-only, write-only, or real-time correction command is executed, set the addresses of the target sector in three target registers. This address is compared with the read sector address, and if they do not match, the TGTNTMET (target not met) status (DECSTS0 register: bit 0) is established.

2-35. XFRCNT (transfer block counter) register (address 24HEX)

This 8-bit register indicates the remaining number of blocks to be transferred. The sub CPU sets the total number of blocks to be transferred before transfer starts. This register value is decremented after one block has been transferred.

The sub CPU can read the value of XFRCNT at any time. However, take care over ±1 error between the read value and actual one, because the reading from sub CPU does not synchronize with variations of XFRCNT.

2-36. BFARA# (buffering area number) register (address 25HEX)

The buffer area is indicated by this register when write-only, real-time correction, or CD-DA command is executed. The sub CPU, first assigns the area to start buffering before any of these commands is executed. The register value is incremented after one sector is buffered.

Buffering starts from the address 0 when the subcode buffering command is executed.

2-37. DLARA (drive last area) register (address 26HEX)

While the decoder is executing the write-only, real-time correction, or CD-DA command, the last area for buffering is assigned by this register. When the ENDLA (bit 1) of the DECCTL0 register is set high and data from the drive (CD DSP) are written into the area assigned by DLARA while the decoder is executing any of the above commands, all subsequent buffering is prohibited.

2-38. XFRARA (transfer area) register (address 27HEX)

The first area for starting transfer is assigned in the automatic transfer mode. The register value is incremented after one block is transferred.

The sub CPU can read the value of XFRARA at any time. However, take care over ±1 error between the read value and actual one, because the reading from sub CPU does not synchronize with the variation of XFRARA.

2-39. RESERVED (address 28HEX)

2-40. HXFRC-H, M, L (host transfer counter - high, middle, low) register (address 29 to 2BHEX)

The number of bytes to be transferred is set in the manual transfer mode. (19 bits)

2-41. RESERVED (address 2CHEX)

2-42. HADRC-H, M, L (host address counter - high, middle, low) register (address 2D to 2FHEX)

The head address to start transfer is assigned in the manual transfer mode.

2-43. RESERVED (address 30HEX)

2-44. SLADR-H, M, L (subcode last address - high, middle, low) register (address 31 to 33HEX)

While the subcode buffering command is being executed, the last address for buffering is set. When the ENDLA (bit 1) of the DECCTL0 register is set high and data are written into the buffer address assigned by SLADR while the decoder is executing the subcode buffering command, all subsequent buffering is prohibited.

2-45. RESERVED (address 34HEX)

2-46. CADRC-H, M, L (sub CPU address counter - high, middle, low) register (address 35 to 37HEX)

The addresses are set by this register when the sub CPU accesses the buffer memory. The register value is incremented if the data concerned are read from the buffer memory or are written into it.

2-47. RESERVED (address 38 to 3BHEX)

2-48. CLRINT0 (clear interrupt status 0) register (address 3CHEX)

When each bit of this register is set high, the corresponding interrupt status is cleared. The bit is automatically set low after its interrupt status has been cleared. Therefore, there is no need for the sub CPU to reset to low.

bit 7: DECINT (Decoder Interrupt)
bit 6: DECTOUT (Decoder Timeout)
bit 5: DRVOVRN (Drive Overrun)
bit 4: SUBCSYNC (Subcode Sync)
bit 3, 2: RESERVED
bit 1: SOFTRST (SRST Detected)
bit 0: HARDRST (HRST Detected)

2-49. CLRINT1 (clear interrupt status 1) register (address 3DHEX)

When each bit of this register is set high, the corresponding interrupt status is cleared. The bit is automatically set low after its interrupt status has been cleared. Therefore, there is no need for the sub CPU to reset to low.

bit 7: PFIFOFUL (Packet FIFO Full)
bit 6: RESERVED
bit 5: RSTCMD (Reset Command)
bit 4: STSREAD (Host Status Read)
bit 3: HSTCMD (Host Command)
bit 2: PIONG (PIO Transfer NG)
bit 1: XFRSTOP (Transfer Stop)
bit 0: BLXFRCMP (Block Transfer Complete)

2-50. INTEN0 (interrupt enable 0) register (address 3EHEX)

When each bit of this register is set high, the interrupt request to the sub CPU by the corresponding interrupt status is enabled. (That is, the XINT pin becomes active in the interrupt status.) Each bit value of this register has no effect on the corresponding interrupt status.

bit 7: DECINT (Decoder Interrupt)
bit 6: DECTOUT (Decoder Timeout)
bit 5: DRVOVRN (Drive Overrun)
bit 4: SUBCSYNC (Subcode Sync)
bit 3, 2: RESERVED
bit 1: SOFTRST (SRST Detected)
bit 0: HARDRST (HRST Detected)

2-51. INTEN1 (interrupt enable 1) register (address 3FHEX)

When each bit of this register is set high, the interrupt request to the sub CPU by the corresponding interrupt status is enabled. (That is, the XINT pin becomes active in the interrupt status.) Each bit value of this register has no effect on the corresponding interrupt status.

bit 7: PFIFOFUL (Packet FIFO Full)
bit 6: RESERVED
bit 5: RSTCMD (Reset Command)
bit 4: STSREAD (Host Status Read)
bit 3: HSTCMD (Host Command)
bit 2: PIONG (PIO Transfer NG)
bit 1: XFRSTOP (Transfer Stop)
bit 0: BLXFRCMP (Block Transfer Complete)

3. Sub CPU Read Registers

Descriptions that are identical with those for the write registers are omitted here.

3-1. DRVSTS (drive status) register (address 00HEX)

The values set by the sub CPU can be read by this register.

bit 7: CINTPOL (subCPU Interrupt Polarity)
bit 6: M/S SEL (Master/Slave select)
bit 5: M/S EN (Master/Slave mode Enable)
bit 4, 3: RESERVED
bit 2, 1: RFRSCTL1, 0 (Refresh Control1, 0)
bit 1: RESERVED

3-2. RAWHDR (raw header) register (address 01HEX)

The Header bytes of the sector sent from the CD DSP can be read by this register at DECINT.

3-3. BFHDR (buffer header) register (address 02HEX)

The Header bytes of the current sector can be read when the write-only or real-time correction command is executed, or after repeat correction has been executed. This register is invalid when the decoder is executing the disable or the monitor-only command.

3-4. BFSHDR (buffer sub header) register (address 03HEX)

The Sub Header bytes of the current sector can be read when the write-only or real-time correction command is executed, or after repeat correction has been executed. This register is invalid when the decoder is executing the disable or the monitor-only command.

3-5. RAWHDRFLG (raw header flag) register (address 04HEX)

Indicates the C2PO value in the RAWHDR register.

bit 7: Minute
bit 6: Second
bit 5: Block
bit 4: Mode
bit 3 to 0: RESERVED

3-6. BFHDRFLG (buffer header flag) (address 05HEX)

Indicates the error state of each byte of BFHDR and BFSHDR registers. High means an error.

bit 7: Minute
bit 6: Second
bit 5: Block
bit 4: Mode
bit 3: File
bit 2: Channel
bit 1: Submode
bit 0: Data Type

3-7. RESERVED (address 06HEX)

3-8. DECSTS0 (decoder status 0) register (address 07HEX)

bit 7: SHRTSCT (short sector)
Indicates that the Sync mark interval was not more than 2351 bytes. This sector does not remain in the buffer memory.

bit 6: NOSYNC
Indicates that the Sync mark was inserted, because one was not detected at the prescribed position.

bit 5: CORINH (correction inhibit)
This is high if the current sector Mode and Form cannot be determined when the AUTODIST bit of the DECCTL register is set high. ECC or EDC is not executed in this sector. The CORINH bit is invalid when AUTODIST is set low. It is high under any of the conditions below when the AUTODIST bit is set high.
(1) When there is an error in the Mode byte.
(2) When the Mode byte is a value other than 01HEX or 02HEX.
(3) When the Mode byte is 02HEX and the C2 pointer is high in the submode byte.

bit 4: ERINBLK (erasure in block)
When the decoder is operating in the monitor-only, write-only, or real-time correction mode, this indicates that at least a 1-byte error flag (C2PO) has been raised in the data, excluding the Sync mark from the current sector CD DSP.
When the decoder is operating in the CD-DA mode, this indicates that at least a 1-byte error flag (C2PO) has been raised in the data from one sector (2352 bytes).

bit 3: CORDONE (correction done)
Indicates that there is an error-corrected byte in the current sector.

bit 2: EDCNG
Indicates that an error was found by the EDC check in the current sector.

bit 1: ECCNG
Indicates that there was an uncorrectable error from the Header byte to the P parity byte in the current sector. (ECCNG = don't care in the Mode2, Form2 sectors.)

bit 0: TGTNTMET (target not met)
Indicates that the target addresses in the TGTMNT, TGTSEC, and TGTBLK registers do not correspond with that of the read sector.

3-9. DECSTS1 (decoder status 1) register (address 08HEX)

bit 7 to 3: RESERVED

bit 2: EDCALL0 (EDC all 0)
This bit is high if there are no errors in the 4-EDC parity bytes of the current sector and the value is 00HEX.

bit 1: CMODE (correction mode)

bit 0: CFORM (correction form)
Indicates the Mode and Form the decoder has discriminated to correct errors of the current sector when the decoder is operating in the real-time correction or repeat correction mode.

CMODE	CFORM	
"L"	"X"	MODE1
"H"	"L"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

3-10. XFRMOD (transfer mode) register (address 09HEX)

The values set by sub CPU can be read by this register.

bit 7: ENHINTCT (Enable Auto HINT upon Start of Packet Command Transfer)
bit 6: ENHINTDT (Enable Auto HINT upon Start of Data Transfer)
bit 5: ENMDMA (Enable Multiword DMA)
bit 4: ENDMABIT (Enable ATAPI Feature resister DMA bit)
bit 3: PIOSEL (PIO Transfer Mode Select)
bit 2: AUTOWAIT (Enable Auto Wait State)
bit 1, 0: WAITCYCL1, 0 (Wait Cycle 1, 0)

3-11. XFRSTS0 (data transfer status 0) register (address 0AHEX)

bit 7 to 2: RESERVED
bit 1: CBFWRRDY (sub CPU buffer write ready)
The sub CPU can write in the CPUBWDT register when this bit is high.
bit 0: CBFRDRDY (sub CPU buffer read ready)
The sub CPU can read the CPUBWDT register when this bit is high.

3-12. XFRSTS1 (data transfer status 1) register (address 0BHEX)

bit 7, 6: RESERVED
bit 5: AUTOEND (enable auto transfer termination)
Value set by sub CPU can be read.
bit 4: RESERVED
bit 3: PFIFOFUL (packet FIFO full status)
When a 12-byte packet command is written to the packet FIFO from the host, this bit is set high.
bit 2: PFIFOEMP (packet FIFO empty status)
When 12-byte data are read by sub CPU from the packet FIFO, this bit is set high.

These bits are automatically cleared when an ATAPI packet command (A0HEX) or an ATAPI soft reset command (08HEX) is issued.

bit 1: IO (HOST transfer direction)
This bit can be set by both sub CPU and host.
In the cases below, the bit is automatically set.
High: When the XFRCTL1 register (0BHEX) -bit 5: AUTOEND is high and the data transfer has been completed.
Low: When an ATAPI packet command (A0HEX) is issued.
bit 0: CoD (command or data)
This bit can be set by both sub CPU and host.
In the cases below, this bit is automatically set.
High: When an ATAPI packet command (A0HEX) is issued.
Low: When the XFRCTL1 register (0BHEX) -bit 5: AUTOEND is high and the data transfer has been completed.

3-13. RESERVED (address 0C, 0DHEX)

3-14. CHPSTS (chip status) register (address 0EHEX)

bit 7 to 3: RESERVED
bit 2: DASP
bit 1: PDIAG
The DASP and XPDI pins can be monitored from these bits.
Positive logic.
bit 0: RESERVED

3-15. REV (revision number) register (address 0FHEX)

The revision number of this IC is 83HEX.

3-16. ATAPI error register (address 10HEX)

This register corresponds to the ATAPI error register of the host. The values set by sub CPU can be read.
bit 7 to 4: SENSE KEY
bit 3: MCR (Media Change Requested)
bit 2: ABRT (Aborted Command)
bit 1: EOM (End Of Media Detected)
bit 0: ILI (Illegal Length Indication)

3-17. ATAPI feature register (address 11HEX)

This register corresponds to the ATAPI feature register of the host. The values set by sub CPU or host can be read.
bit 0: DMA

3-18. ATA sector count register (address 12HEX)

This register corresponds to the ATA sector count/ATAPI interrupt reason register of the host.
The values set by sub CPU or host can be read.

3-19. ATAPI sector number register (address 13HEX)

This register corresponds to the ATA sector number register of the host. The values set by sub CPU or host can be read.

3-20. ATAPI byte count high/low register (address 14, 15HEX)

This register corresponds to the byte count high/low register of the host. The values set by sub CPU or host can be read.

3-21. ATAPI drive select register (address 16HEX)

This register corresponds to the ATAPI drive select register of the host. The values set by sub CPU or host can be read.
bit 4: DRV

3-22. ATA command register (address 17HEX)

This register corresponds to the ATA command register of the host. The values set by sub CPU or host can be read.

3-23. ATAPI packet command register (address 18HEX)

This register is a 12-bytes FIFO.
The ATAPI packet command issued from the host can be read by reading this register 12 times.

3-24. ATAPI status 1 register (address 19HEX)

The values set by sub CPU can be read.

bit 7, 6: RESERVED
bit 5: DRDY1 (Drive1 Ready)
bit 4: DSC1 (Drive1 Seek Complete)
bit 3: HST5
bit 2: HST1
bit 1: DRDY0 (Drive0 Ready)
bit 0: DSC0 (Drive0 Seek Complete)

3-25. ATAPI status 2 register (address 1AHEX)

bit 7: BUSY

In the cases below, the bit is set automatically. The bit can also be set directly by the sub CPU.

High: When the host writes a command into the ATAPI command register.
High: When the transfer of a 6-words (12-bytes) packet command from the host has been completed.
High: When the XFRCTL1 register (0BHEX) -bit 5: AUTOEND is low and the data transfer with the host has been completed.
High: When various reset signals have been asserted.
Low: When an ATAPI packet command (A0HEX) is issued and the setting of packet command transfer has been completed.
Low: When the data transfer with the host is activated in the PIO mode.
Low: When the XFRCTL1 register (0BHEX) -bit 5: AUTOEND is high and the data transfer with the host has been completed.

bit 6: RESERVED
bit 5: CORR

The values set by sub CPU can be read.

bit 4: HINT

The HINT signal can be monitored.
In the cases below, this bit is set automatically.

- When the XFRMOD register (09HEX) -bit 7: ENHINTCT is high and the setting of packet command transfer is completed.
- When the XFRMOD register (09HEX) -bit 6: ENHINTDT is high and the data transfer with the host is activated.
- When the XFRCTL1 register (0BHEX) -bit 5: AUTOEND is high and the data transfer with the host is completed.

The bit is reset in the cases below.

- When the host has read the ATAPI status register.
- When the transfer of 12-bytes packet command has been completed before the host reads the ATAPI status register.
- When the XFRCTL1 register (0BHEX) -bit 5: AUTOEND is low and the data transfer with the host has been completed before the host reads the ATAPI status register.

bit 3: HRST

The HRST pin can be monitored.

bit 2: SRST
bit 1: XHINEN

This bit corresponds to the ATAPI device control register - bit 2, 1 of the host.
The values set by the host can be read.

bit 0: CHECK

The values set by sub CPU can be read.

3-26. CSCTARA (current sector area) (address 1BHEX)
Indicates the area number being written in the current sector.

3-27. CPUBRDT (CPU buffer read data) register (address 1CHEX)
The sub CPU reads data from the buffer memory via this register.

3-28. SBCSTS (subcode status) register (address 1DHEX)
The error status of the subcode written to the buffer while the CD-DA command is executed is indicated by this register.
The period of validity is from a DECINT to the next DECINT.

bit 7: SBCOVRN (subcode overrun)
The SBCOVRN status is established when the ENSBCBT (bit 3) of the XFRFMT1 register is set high and subcode buffering to the area assigned by DLARA is completed while the decoder is executing the CD-DA command. Establishment of DRVOVRN and SBCOVRN states involves a time difference.

bit 6: OVERFLOW
Indicates that the FIFO of SBCSTS has overflowed with frequent occurrences of the subcode short sync. Subcode buffering is stopped by this overflow. Subcode has not been buffered in sectors obtained by subsequent interrupts of the decoder.

bit 5: BFNTVAL (buffer not valid)
Indicates that valid data have not been written to the buffer due to the short subcode sector.

bit 4: NOSYNC0
Indicates that the Sync mark was inserted because subcode Sync mark was not detected at the prescribed position.

bit 3 to 1: RESERVED

bit 0: SUBQERR0 (subcode-Q error 0)
Indicates that the subcode-Q was determined to be an error by the CRC check when ALLSBC is low.

3-29. SBQSTS (subcode-Q status) register (address 1EHEX)
This register indicates the error status of the subcode-Q taken from CD DSP.
The period of validity is from a SBCSYNC to the next SBCSYNC.

bit 7 to 3: RESERVED

bit 2: SHTSBCS1 (short subcode sector 1)
Indicates that the subcode Sync mark interval after the previous SBCSYNC interrupt occurred was less than 98WFCK.

bit 1: NOSYNC1
Indicates that the Sync mark was inserted because subcode Sync mark was not detected at the prescribed position.

bit 0: SUBQERR1 (subcode-Q error 1)
Indicates that the subcode-Q was determined to be an error by the CRC check.

3-30. SBQDT (subcode-Q DATA) register (address 1FHEX)
The subcode-Q value can be read by reading this register 10 times. The read subcode-Q is data just before the SBCSYNC interrupt.

3-31. RESERVED (address 20HEX)

3-32. TGTMIN (target minute) register (address 21HEX)

3-33. TGTSEC (target second) register (address 22HEX)

3-34. TGTBLK (target block) register (address 23HEX)

3-35. XFRCNT (transfer block counter) register (address 24HEX)

3-36. BFARA# (buffering area number) register (address 25HEX)

3-37. DLARA (drive last area) register (address 26HEX)

3-38. XFRARA (transfer area) register (address 27HEX)

3-39. RESERVED (address 28HEX)

3-40. HXFRC-H, M, L (host transfer counter - high, middle, low) register (address 29 to 2BHEX)

3-41. RESERVED (address 2CHEX)

3-42. HADRC-H, M, L (host address counter - high, middle, low) register (address 2D to 2FHEX)

3-43. RESERVED (address 30HEX)

3-44. SLDR-H, M, L (subcode last address - high, middle, low) register (address 31 to 33HEX)

3-45. RESERVED (address 34HEX)

3-46. CADRC-H, M, L (sub CPU address counter - high, middle, low) register (address 35 to 37HEX)

3-47. RESERVED (address 38HEX)

3-48. SADRC-H, M, L (subcode address counter - high, middle, low) register (address 39 to 3BHEX)
The buffer address can be read in the subcode buffering command.

3-49. INTSTS0 (interrupt status 0) register (address 3CHEX)

The value of each bit in this register is the value of corresponding interrupt status. These bits are not affected by the values of the INTEN0 register bits.

bit 7: DECINT (decoder interrupt)

This interrupt occurs when the decoder is operating a command.

(1) The DECINT status is established if the Header byte is received from CD DSP when the Sync mark is detected or inserted while the decoder is executing the write-only, monitor-only, or real-time correction command. However, it is not established if the Sync mark interval is less than 2352 bytes when its detection window is open.

(2) The DECINT status is established each time one correction is completed when the decoder is in the repeat correction mode.

(3) The DECINT status is established each time 2352 bytes of data are written while the decoder is executing the CD-DA command.

(4) The DECINT status is established when the subcode Sync mark is detected or is inserted when the decoder is executing subcode buffering. However, it is not established if the interval from the DECINT to the next subcode Sync mark detected is less than 98WFCK.

bit 6: DECTOUT (decoder timeout)

The DECTOUT status is established when the Sync mark is not detected even after the time it takes to search three sectors (40.6ms at normal speed playback) has elapsed after the decoder has been set to the monitor-only, write-only or real-time correction mode.

bit 5: DRVOVRN (drive overrun)

The DRVOVRN status is established when the buffering into the area assigned by DLARA is completed while the decoder is executing the write-only, real-time correction or CD-DA command.

The DRVOVRN status is also established when the buffering into the address assigned by SLADR is completed while the decoder is executing the subcode buffering command.

bit 4: SUBCSYNC (subcode sync)

The SUBCSYNC status is established when the subcode Sync mark is detected or inserted while taking-in of subcode is enabled. However, it is not established if the interval from the SUBCSYNC to the next subcode Sync mark detected is less than 98WFCK.

If the SUBCSYNC interrupt is not cleared within 95WFCK from the interrupt, the SUBCSYNC status is not established when the next subcode Sync mark is detected or inserted. In this case, the subcode-Q read from the SBQDT register is not renewed.

bit 3, 2: RESERVED

bit 1: SOFTRST (SRST detected)

The SOFTRST status is established when the host asserts the ATAPI device control register -bit 2: SRST.

bit 0: HARDRST (HRST detected)

The HARDRST status is established when the host asserts the HRST pin.

3-50. INSTS1 (interrupt status 1) register (address 3DHEX)

The value of each bit in this register is that of the corresponding interrupt status. These bits are not affected by the values of the INTEN1 register bits.

bit 7: PFIFOFUL (packet FIFO full)
The PFIFOFUL status is established when the transfer of a 6-words (12 bytes) packet command from the host is completed.

bit 6: RESERVED

bit 5: RSTCMD (reset command)
The RSTCMD status is established when an ATAPI soft reset command (08HEX) is issued from the host.

bit 4: STSREAD (HOST status read)
The STSREAD status is established when the ATAPI status register is read by the host after data transfer with the host has been completed.

bit 3: HSTCMD (host command)
The HSTCMD status is established when the command is written into the ATA command register from the host.

bit 2: PIONG (PIO transfer NG)
The PIONG status is established if a read/write operation is executed by the host when the IO channel ready signal: REDY is low (not ready) during data transfer in the PIO mode.

bit 1: XFRSTOP (transfer stop)
The XFRSTOP status is established when all transfers are completed when the automatic transfer mode to the host is enabled.
The XFRSTOP status is also established after transfer to the host is completed by HXFRC when the automatic transfer mode to the host is disabled.

bit 0: BLXFRCMP (block transfer complete)
The BLXFRCMP status is established after one block transfer is completed when the automatic transfer mode to the host is enabled.

3-51. INTEN0 (interrupt enable 0) register (address 3EHEX)

The values written to the INTEN0 register can be read as they are.

3-52. INTEN1 (interrupt enable 1) register (address 3FHEX)

The values written to the INTEN1 register can be read as they are.

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CONFIG0	00	CINT POL	M/S SEL	M/S EN	"L"	EXCK SEL	DIS MCLK	DIS HCLK	RAM SIZE
CONFIG1	01	SW OPEN	"L"	"H"	"L"	"L"	RFRS CTL1	RFRS CTL0	"L"
LSTARA	02	b7	b6	b5	b4	b3	b2	b1	b0
LHADR	03	b7	b6	b5	b4	b3	b2	b1	b0
DRVIF	04	C2PO L1st	LCH LOW	BCLK RED	BCLK MD1	BCLK MD0	LSB 1st	"L"	"L"
XFRFMT0	05	"L"	"L"	SYNC	HEAD ER	SBHE ADER	USER DATA	PARI TY	"L"
XFRFMT1	06	BLKE FLAG	"L"	ENBY TFBT	"L"	ENSB CBT	ALL SBC	"L"	ZA SUBQ
DECCTL0	07	AUTO DIST	MODE SEL	FORM SEL	"L"	ENFM 2EDC	MDBY TCTL	EN DLA	ATDL RNEW
DECCTL1	08	ENSB QRD	"L"	DEC CMD2	DEC CMD1	DEC CMD0	"L"	"L"	"L"
XFRMOD	09	ENHI NTCT	ENHI NTDT	EN MDMA	ENDM ABIT	PIO SEL	AUTO WAIT	WAIT CYCL1	WAIT CYCL0
XFRCTL0	0A	AUTO XFR	"L"	"L"	"L"	CPUD MAEN	CPU SRC	"L"	"L"
XFRCTL1	0B	PFIF O CL	"L"	AUTO END	HSTX FREN	"L"	"L"	IO	CoD
	0C	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
CHPCTL0	0D	CHIP RST	TGT MET	INC TGT	RPCO RTRG	"L"	"L"	"L"	"L"
CHPCTL1	0E	"L"	"L"	"L"	"L"	"L"	DASP	PDIAG	CLR HINT
DISCHG DRVADR	0F	"L"	b6	b5	b4	b3	b2	"L"	"L"
ERROR	10	SENSE KEY				MCR	ABRT	EOM	ILI
FEATUR	11	b7	b6	b5	b4	b3	b2	b1	DMA
INT REASON	12	b7	b6	b5	b4	b3	b2	IO	CoD
SECTOR NUMBER	13	b7	b6	b5	b4	b3	b2	b1	b0
BYTE CNT-H	14	b15	b14	b13	b12	b11	b10	b9	b8
BYTE CNT-L	15	b7	b6	b5	b4	b3	b2	b1	b0

Sub CPU write registers (1)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DRIVE SELECT	16	b7	b6	b5	DRV	b3	b2	b1	b0
HOST CMD	17	b7	b6	b5	b4	b3	b2	b1	b0
	18	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
ATAPI STS 1	19	"L"	"L"	DRDY1	DSC1	HST5	HST1	DRDY0	DSC0
ATAPI STS 2	1A	BUSY	"L"	CORR	EN HINT	"L"	"L"	"L"	CHECK
UN LOCK	1B								
CPUBW DT	1C	b7	b6	b5	b4	b3	b2	b1	b0
	1D	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
SCTINF	1E	"L"	"L"	"L"	"L"	"L"	MODE2	FORM2	"L"
	1F	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
	20	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
TGTMIN	21	b7	b6	b5	b4	b3	b2	b1	b0
TGTSEC	22	b7	b6	b5	b4	b3	b2	b1	b0
TGTBLK	23	b7	b6	b5	b4	b3	b2	b1	b0
XFRCNT	24	b7	b6	b5	b4	b3	b2	b1	b0
BFARA#	25	b7	b6	b5	b4	b3	b2	b1	b0
DLARA	26	b7	b6	b5	b4	b3	b2	b1	b0
XFRARA	27	b7	b6	b5	b4	b3	b2	b1	b0
	28	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
HXFRC -H	29	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
HXFRC -M	2A	b15	b14	b13	b12	b11	b10	b9	b8
HXFRC -L	2B	b7	b6	b5	b4	b3	b2	b1	b0

Sub CPU write registers (2)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	2C	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
HADRC -H	2D	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
HADRC -M	2E	b15	b14	b13	b12	b11	b10	b9	b8
HADRC -L	2F	b7	b6	b5	b4	b3	b2	b1	b0
	30	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
SLADR -H	31	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
SLADR -M	32	b15	b14	b13	b12	b11	b10	b9	b8
SLADR -L	33	b7	b6	b5	b4	b3	b2	b1	b0
	34	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
CADRC -H	35	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
CADRC -M	36	b15	b14	b13	b12	b11	b10	b9	b8
CADRC -L	37	b7	b6	b5	b4	b3	b2	b1	b0
	38	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
	39	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
	3A	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
	3B	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
CLRINT0	3C	DEC INT	DEC TOUT	DRV OVRN	SUBC SYNC	"L"	"L"	SOFT RST	HARD RST
CLRINT1	3D	PFIF OFUL	"L"	RST CMD	STS READ	HST CMD	PIO NG	XFR STOP	BLXF RCMP
INTEN0	3E	DEC INT	DEC TOUT	DRV OVRN	SUBC SYNC	"L"	"L"	SOFT RST	HARD RST
INTEN1	3F	PFIF OFUL	"L"	RST CMD	STS READ	HST CMD	PIO NG	XFR STOP	BLXF RCMP

Sub CPU write registers (3)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DRVSTS	00	CINT POL	M/S SEL	M/S EN	"L"	"L"	RFRS CTL1	RFRS CTL0	"L"
RAWHDR	01	b7	b6	b5	b4	b3	b2	b1	b0
BFHDR	02	b7	b6	b5	b4	b3	b2	b1	b0
BFSHDR	03	b7	b6	b5	b4	b3	b2	b1	b0
RAWHDR FLG	04	MIN UTE	SEC OND	BLO CK	MODE	"H"	"H"	"H"	"H"
BFHDR FLG	05	MIN UTE	SEC OND	BLO CK	MODE	FILE	CHAN NEL	SUB MODE	DATA TYPE
	06								
DECSTS0	07	SHRT SCT	NO SYNC	COR INH	ERIN BLK	COR DONE	EDC NG	ECC NG	TGTN TMET
DECSTS1	08	"Z"	"Z"	"Z"	"Z"	"Z"	EDC ALL0	C MODE	C FORM
XFRMOD	09	ENHI NTCT	ENHI NTDT	EN MDMA	ENDM ABIT	PIO SEL	AUTO WAIT	WAIT CYCL1	WAIT CYCL0
XFRSTS0	0A	"H"	"H"	"H"	"H"	"H"	"H"	CBFW RRDY	CBFR DRDY
XFRSTS1	0B	"L"	"L"	AUTO END	"L"	PFIF OFUL	PFIF OEMP	IO	CoD
	0C								
	0D								
CHPSTS	0E	"L"	"L"	"L"	"L"	"L"	DASP	PDIAG	"L"
REV	0F	"H"	"L"	"L"	"L"	"L"	"L"	"H"	"H"
ERROR	10	SENSE KEY				MCR	ABRT	EOM	ILI
FEATUR	11	b7	b6	b5	b4	b3	b2	b1	DMA
SECTOR COUNT	12	b7	b6	b5	b4	b3	b2	b1	b0
SECTOR NUMBER	13	b7	b6	b5	b4	b3	b2	b1	b0
BYTE CNT-H	14	b15	b14	b13	b12	b11	b10	b9	b8
BYTE CNT-L	15	b7	b6	b5	b4	b3	b2	b1	b0

Sub CPU read registers (1)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DRIVE SELECT	16	b7	LBA	b5	DRV	b3	b2	b1	b0
HOST CMD	17	b7	b6	b5	b4	b3	b2	b1	b0
PACKET CMD	18	b7	b6	b5	b4	b3	b2	b1	b0
ATAPI STS 1	19	"L"	"L"	DRDY1	DSC1	HST5	HST1	DRDY0	DSC0
ATAPI STS 2	1A	BUSY	"L"	CORR	HINT	HRST	SRST	XHIN TEN	CHECK
CSCT ARA	1B	b7	b6	b5	b4	b3	b2	b1	b0
CPUBR DT	1C	b7	b6	b5	b4	b3	b2	b1	b0
SBCSTS	1D	SBC OVRN	OVER FLOW	BFNT VAL	NOSY NC0	"H"	"H"	"H"	SUBQ ERR0
SBQSTS	1E	"H"	"H"	"H"	"H"	"H"	SHTS BCS1	NOSY NC1	SUBQ ERR1
SUBQDT	1F	b7	b6	b5	b4	b3	b2	b1	b0
	20								
TGTMIN	21	b7	b6	b5	b4	b3	b2	b1	b0
TGTSEC	22	"L"	b6	b5	b4	b3	b2	b1	b0
TGTBLK	23	"L"	b6	b5	b4	b3	b2	b1	b0
XFRCNT	24	b7	b6	b5	b4	b3	b2	b1	b0
BFARA#	25	b7	b6	b5	b4	b3	b2	b1	b0
DLARA	26	b7	b6	b5	b4	b3	b2	b1	b0
XFRARA	27	b7	b6	b5	b4	b3	b2	b1	b0
	28								
HXFRC -H	29	"Z"	"Z"	"Z"	"Z"	"Z"	b18	b17	b16
HXFRC -M	2A	b15	b14	b13	b12	b11	b10	b9	b8
HXFRC -L	2B	b7	b6	b5	b12	b3	b2	b1	b0

Sub CPU read registers (2)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	2C								
HADRC -H	2D	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
HADRC -M	2E	b15	b14	b13	b12	b11	b10	b9	b8
HADRC -L	2F	b7	b6	b5	b4	b3	b2	b1	b0
	30								
SLADR -H	31	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
SLADR -M	32	b15	b14	b13	b12	b11	b10	b9	b8
SLADR -L	33	b7	b6	b5	b4	b3	b2	b1	b0
	34								
CADRC -H	35	"H"	"H"	"H"	"H"	"H"	b18	b17	b16
CADRC -M	36	b15	b14	b13	b12	b11	b10	b9	b8
CADRC -L	37	b7	b6	b5	b4	b3	b2	b1	b0
	38								
SADRC -H	39	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
SADRC -M	3A	b15	b14	b13	b12	b11	b10	b9	b8
SADRC -L	3B	b7	b6	b6	b4	b3	b2	b1	b0
INTSTS0	3C	DEC INT	DEC TOUT	DRV OVRN	SUBC SYNC	"L"	"L"	SOFT RST	HARD RST
INTSTS1	3D	PFIF OFUL	"L"	RST CMD	STS READ	HST CMD	PIO NG	XFR STOP	BLXF RCMP
INTEN0	3E	DEC INT	DEC TOUT	DRV OVRN	SUBC SYNC	"L"	"L"	SOFT RST	HARD RST
INTEN1	3F	PFIF OFUL	"L"	RST CMD	STS READ	HST CMD	PIO NG	XFR STOP	BLXF RCMP

Sub CPU read registers (3)

4. HOST Interface

The following ATAPI registers are supported.

Address					Register	
HCS0	HCS1	HA2	HA1	HA0	Read (XHRD)	Write (XHWR)
					Control block registers	
1	0	1	1	0	Alternate ATAPI Status	ATAPI Device Control
1	0	1	1	1	Diskette Change/Drive Address	Unused
					Command block registers	
0	1	0	0	0	Data	
0	1	0	0	1	ATAPI Error	ATAPI Feature
0	1	0	1	0	ATAPI Interrupt Reason	ATA Sector Count
0	1	0	1	1	ATA Sector Number	
0	1	1	0	0	ATAPI Byte Count Low	
0	1	1	0	1	ATAPI Byte Count High	
0	1	1	1	0	ATAPI Drive Select	
0	1	1	1	1	ATAPI Status	ATA Command

The bit width of all registers excluding the data register is 8 bits. The bit width of the data register is 16 bits.

Command block registers

The host can read/write to the command block registers only when the BUSY bit (ATAPI status register -bit 7) is low. When the BUSY bit is high, the value of the alternate ATAPI status register is read.

4-1. Data register (read/write)

This register is valid only when the DRQ bit (ATAPI status register -bit 3) is high.
The bit width of this register is 16 bits.

4-2. ATAPI error register (read)

The error status of the command finally executed by the drive is read by this register.

bit 7 to 4: SENSE KEY
bit 3: MCR (Media Change Requested)
bit 2: ABRT (Aborted Command)
bit 1: EOM (End Of Media Detected)
bit 0: ILI (Illegal Length Indication)

4-3. ATAPI feature register (write)

bit 7 to 1: Optional values can be set.
bit 0: DMA (optional)
Set this bit high for data transfer in the DMA mode.
However, the transfer mode is determined by the combination of this bit and the ENDMABIT (bit 4) and PIOSEL (bit 3) bits of the sub CPU transfer mode register (address 09HEX).

4-4. ATAPI interrupt reason (read)/ATA sector count (write) register

This 8-bytes register can be read/written by both host and sub CPU.

bit 1: IO (In or Out)

bit 0: CoD (Command or Data)

The direction and type of data transfer are determined by the three bits: IO, CoD, and DRQ (ATAPI status register -bit 3).

DRQ	IO	CoD	Status of transfer
"H"	"L"	"L"	Data transfer from host
"H"	"L"	"H"	Packet command transfer from host
"H"	"H"	"L"	Data transfer to host
"H"	"H"	"H"	RESERVED
"L"	"H"	"H"	Data transfer termination status

4-5. ATA sector number register (read/write)

This 8-bytes register can be read/written by both host and sub CPU.

4-6. ATAPI byte count low/high register (read/write)

This register sets the number of bytes transferred by one data transfer request (DRQ). (16 bits)

This register can be read/written by both host and sub CPU.

4-7. ATAPI drive select register (read/write)

This 8-bytes register can be read/written by both host and sub CPU.

bit 4: DRV

This bit allows the host to select the drive.

High: Selects the slave drive.

Low: Selects the master drive.

4-8. ATAPI status register (read)

This register allows the host to read the drive status. The interrupt request signal: HINT to the host is cleared by reading this register.

bit 7 BUSY

bit 6 DRDY (Drive Ready)

bit 4 DSC (Drive Seek Complete)

bit 3 DRQ (Data Request)

bit 2 CORR (Corrected Data)

bit 0 CHECK

bit 5, 1: The values set by sub CPU can be read.

4-9. ATA command register (write)

This register allows the host to write the ATA command.

The interrupt request is applied to sub CPU by writing a command to this register.

Control Block Registers

4-10. Alternate ATAPI status register (read)

This register is identical to the ATAPI status register.
However, the interrupt request signal: HINT to the host is not cleared by reading this register.

4-11. ATAPI device control register (write)

bit 7 to 3: RESERVED

bit 2: SRST
This bit is the ATA soft reset bit. (See appendix.)

bit 1: nIEN
When this bit is set low while a drive is selected, the interrupt request signal: HINT to the host is enabled. When this bit is high or the drive is not selected, the HINT pin generates a high impedance.

bit 0: RESERVED

4-12. Diskette change/drive address register (read)

bit 7: Hi-Z

bit 6 to 2: The values set by sub CPU can be read.

bit 1: nDS1
This is low when the slave drive is selected.

bit 0: nDS0
This is low when the master drive is selected.

Appendix: Reset Condition

XRST: XRST pin
CRST: CHPCTL0 register (0D$_{HEX}$) -bit 7
HRST: HRST pin
RCMD: ATAPI soft reset command (08$_{HEX}$)
SRST: ATAPI software reset

1. Sub CPU write registers

REG	ADR	XRST	CRST	HRST	RCMD	SRST	Bit 7	6	5	4	3	2	1	0
CONFIG0	00h	O	O				0	0	0	X	0	0	0	0
CONFIG1	01h	O					0	0	1	0	X	0	1	X
			O				X	X	X	X	X	0	1	X
LSTARA	02h	O	O				0	0	0	0	0	0	0	0
LHADR	03h	O	O				0	0	0	0	0	0	0	0
DRVIF	04h	O					0	0	1	0	1	0	X	0
XFRFMT0	05h	O	O				X	X	0	0	0	0	0	X
XFRFMT1	06h	O	O				0	X	0	X	0	0	X	0
DECCTL0	07h	O	O				1	0	0	X	0	1	0	1
DECCTL1	08h	O	O				0	X	0	0	0	X	X	X
XFRMOD	09h	O	O				0	1	0	0	1	0	0	0
				O	O		X	X	0	X	X	X	X	X
XFRCTL0	0Ah	O	O				1	X	X	X	0	0	X	X
XFRCTL1	0Bh	O	O				0	X	0	0	X	X	0	0
				O	O		X	X	0	0	X	X	0	0
CHPCTL0	0Dh	O					0	0	0	0	X	X	X	X
CHPCTL1	0Eh	O	O	O	O	O	X	X	X	X	X	1	0	X
DISCHG	0Fh	O	O				X	0	0	0	0	0	X	X
ERROR	10h	O	O				0	0	0	0	0	0	0	0
FEATUR	11h	O	O				0	0	0	0	0	0	0	0
IREASON	12h	O	O	O	O		0	0	0	0	0	0	0	0
SECTNO.	13h	O	O				0	0	0	0	0	0	0	0
BYTCNT-H	14h	O	O				0	0	0	0	0	0	0	0
BYTCNT-L	15h	O	O				0	0	0	0	0	0	0	0
DRVSEL	16h	O	O	O	O	O	0	0	0	0	0	0	0	0
HSTCMD	17h	O	O				0	0	0	0	0	0	0	0
ASTS1	19h	O	O				X	X	0	0	0	0	0	0
ASTS2	1Ah	O	O	O	O		1	X	0	0	X	X	X	0
						O	1	X	X	X	X	X	X	X
UNLOCK	1Bh													
CPUBWDT	1Ch	O	O				0	0	0	0	0	0	0	0
SCTINF	1Eh	O	O				X	X	X	X	X	0	0	X

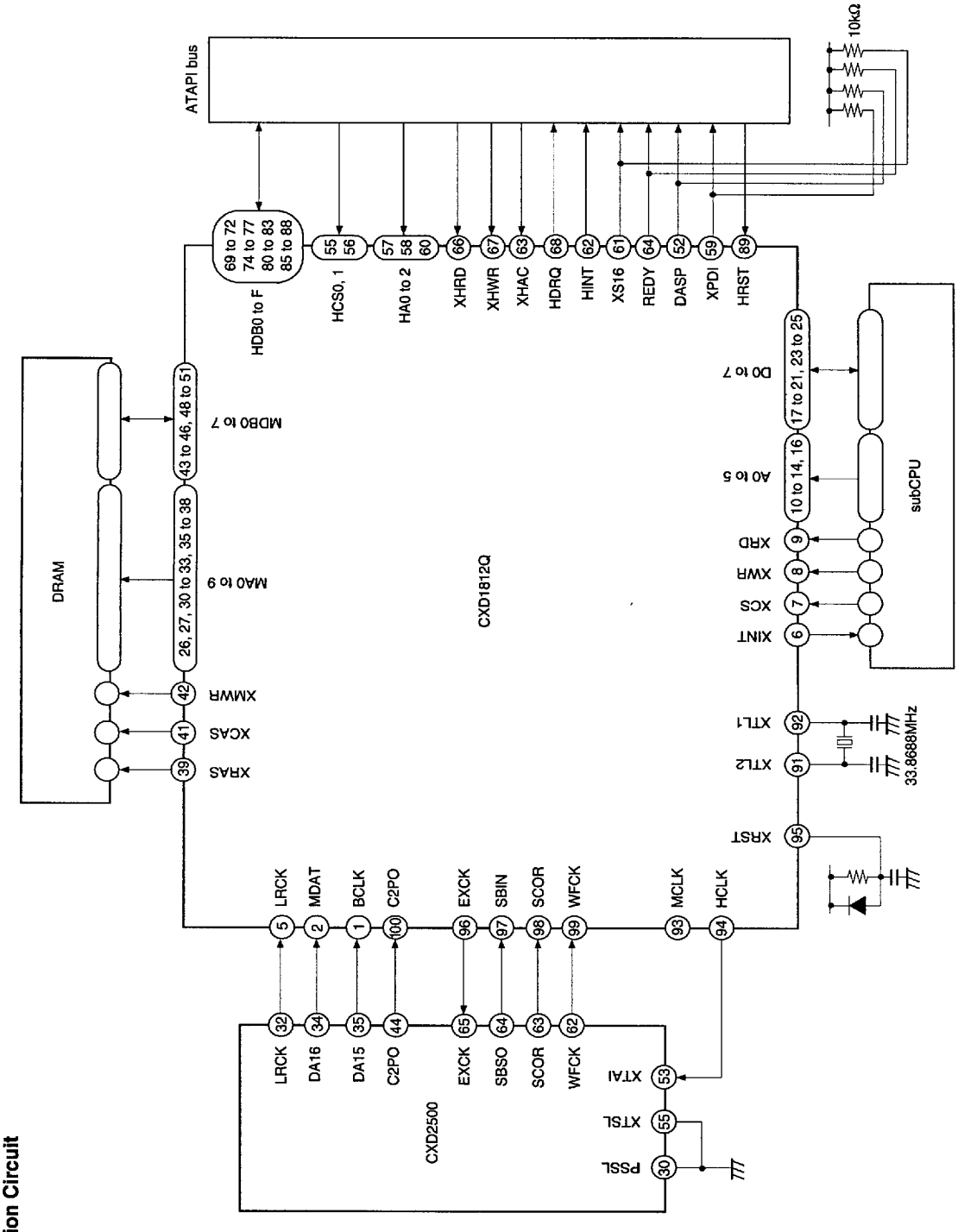
REG	ADR	XRST	CRST	HRST	RCMD	SRST	Bit	7	6	5	4	3	2	1	0
TGTMIN	21h	O	O					0	0	0	0	0	0	0	0
TGTSEC	22h	O	O					0	0	0	0	0	0	0	0
TGTBLK	23h	O	O					0	0	0	0	0	0	0	0
XFRCNT	24h	O	O					0	0	0	0	0	0	0	0
BFARA	25h	O	O					0	0	0	0	0	0	0	0
DLARA	26h	O	O					0	0	0	0	0	0	0	0
XFRARA	27h	O	O					0	0	0	0	0	0	0	0
HXFRC-H	29h	O	O					X	X	X	X	X	0	0	0
HXFRC-M	2Ah	O	O					0	0	0	0	0	0	0	0
HXFRC-L	2Bh	O	O					0	0	0	0	0	0	0	0
HADRC-H	2Dh	O	O					X	X	X	X	X	0	0	0
HADRC-M	2Eh	O	O					0	0	0	0	0	0	0	0
HADRC-L	2Fh	O	O					0	0	0	0	0	0	0	0
SLADR-H	31h	O	O					X	X	X	X	X	0	0	0
SLADR-M	32h	O	O					0	0	0	0	0	0	0	0
SLADR-L	33h	O	O					0	0	0	0	0	0	0	0
CADRC-H	35h	O	O					X	X	X	X	X	0	0	0
CADRC-M	36h	O	O					0	0	0	0	0	0	0	0
CADRC-L	37h	O	O					0	0	0	0	0	0	0	0
CLRINT0	3Ch	O	O					0	0	0	0	X	X	0	0
CLRINT1	3Dh	O	O					0	X	0	0	0	0	0	0
INTEN0	3Eh	O	O					0	0	0	0	X	X	0	0
INTEN1	3Fh	O	O					0	X	0	0	0	0	0	0

2. Sub CPU read registers

REG	ADR	XRST	CRST	HRST	RCMD	SRST	Bit 7	6	5	4	3	2	1	0
DRVSTS	00h	O	O				0	0	0	0	0	0	1	0
RAWHDR	01h	O	O				0	0	0	0	0	0	0	0
BFHDR	02h	O	O				0	0	0	0	0	0	0	0
BFSHDR	03h	O	O				0	0	0	0	0	0	0	0
RAWHDFG	04h	O	O				0	0	0	0	1	1	1	1
BFHDRFG	05h	O	O				0	0	0	0	0	0	0	0
DECSTS0	07h	O	O				0	0	0	0	0	1	0	0
DECSTS1	08h	O	O				X	X	X	X	X	0	0	0
XFRMOD	09h	O	O				0	1	0	0	1	0	0	0
				O	O		X	X	0	X	X	X	X	X
XFRSTS0	0Ah	O	O				1	1	1	1	1	1	0	0
XFRSTS1	0Bh	O	O	O	O		0	0	0	0	0	1	0	0
CHPSTS	0Eh	O	O	O	O	O	0	0	0	0	0	1	X	0
REV	0Fh						1	0	0	0	0	0	1	1
ERROR	10h	O	O				0	0	0	0	0	0	0	0
FEATUR	11h	O	O				0	0	0	0	0	0	0	0
IREASON	12h	O	O	O	O		0	0	0	0	0	0	0	0
SECTNO.	13h	O	O				0	0	0	0	0	0	0	0
BYTCNT-H	14h	O	O				0	0	0	0	0	0	0	0
BYTCNT-L	15h	O	O				0	0	0	0	0	0	0	0
DRVSEL	16h	O	O	O	O	O	0	0	0	0	0	0	0	0
HSTCMD	17h	O	O				0	0	0	0	0	0	0	0
PACCMD	18h	O	O	O	O		0	0	0	0	0	0	0	0
ASTS1	19h	O	O				0	0	0	0	0	0	0	0
ASTS2	1Ah	O	O				1	0	0	0	X	0	1	0
				O			1	0	0	0	1	0	1	0
					O		1	0	0	0	X	X	X	0
						O	1	0	X	X	X	1	X	X
CSCTARA	1Bh	O	O				0	0	0	0	0	0	0	0
CPUBRDT	1Ch	O	O				0	0	0	0	0	0	0	0
SBCSTS	1Dh						X	X	X	X	X	X	X	X
SBQSTS	1Eh	O	O				1	1	1	1	1	0	0	0
SBQDT	1Fh						X	X	X	X	X	X	X	X
TGTMIN	21h	O	O				0	0	0	0	0	0	0	0
TGTSEC	22h	O	O				0	0	0	0	0	0	0	0
TGTBLK	23h	O	O				0	0	0	0	0	0	0	0
XFRCNT	24h	O	O				0	0	0	0	0	0	0	0

REG	ADR	XRST	CRST	HRST	RCMD	SRST	Bit	7	6	5	4	3	2	1	0
BFARA	25h	O	O					0	0	0	0	0	0	0	0
DLARA	26h	O	O					0	0	0	0	0	0	0	0
XFRARA	27h	O	O					0	0	0	0	0	0	0	0
HXFRC-H	29h	O	O					X	X	X	X	X	0	0	0
HXFRC-M	2Ah	O	O					0	0	0	0	0	0	0	0
HXFRC-L	2Bh	O	O					0	0	0	0	0	0	0	0
HADRC-H	2Dh	O	O					0	0	0	0	0	0	0	0
HADRC-M	2Eh	O	O					0	0	0	0	0	0	0	0
HADRC-L	2Fh	O	O					0	0	0	0	0	0	0	0
SLADR-H	31h	O	O					0	0	0	0	0	0	0	0
SLADR-M	32h	O	O					0	0	0	0	0	0	0	0
SLADR-L	33h	O	O					0	0	0	0	0	0	0	0
CADRC-H	35h	O	O					1	1	1	1	1	0	0	0
CADRC-M	36h	O	O					0	0	0	0	0	0	0	0
CADRC-L	37h	O	O					0	0	0	0	0	0	0	0
SADRC-H	39h	O	O					0	0	0	0	0	0	0	0
SADRC-M	3Ah	O	O					0	0	0	0	0	0	0	0
SADRC-L	3Bh	O	O					0	0	0	0	0	0	0	0
INTSTS0	3Ch	O	O					0	0	0	0	0	0	0	0
				O				X	X	X	X	0	0	X	1
						O		X	X	X	X	0	0	1	X
INTSTS1	3Dh	O	O					0	0	0	0	0	0	0	0
				O				0	0	X	0	0	0	X	X
					O			0	0	1	0	0	0	X	X
INTEN0	3Eh	O	O					0	0	0	0	0	0	0	0
INTEN1	3Fh	O	O					0	0	0	0	0	0	0	0

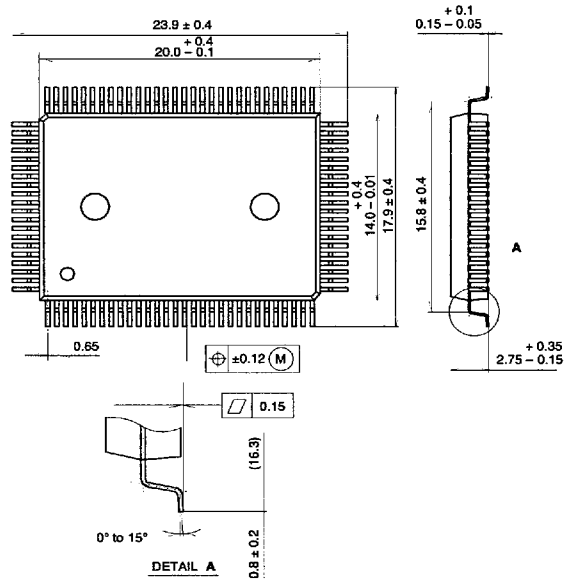
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

100PIN QFP (PLASTIC)

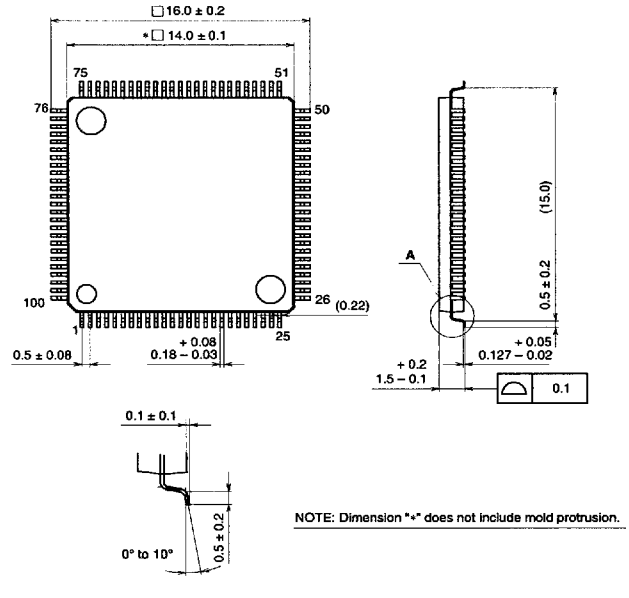


SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	*QFP100-P-1414-A
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	———