CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C108
CY7C109

131,072 x 8 Static R/W RAM

Features

- **High speed**
  - **— t_{AA} = 25 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 825 mW**
- **Low standby power**
  - **— 165 mW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY7C108 and CY7C109 are high-performance CMOS static RAMs organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. Both devices have an automatic power-down feature that reduces power consumption by more than 70% when deselected.

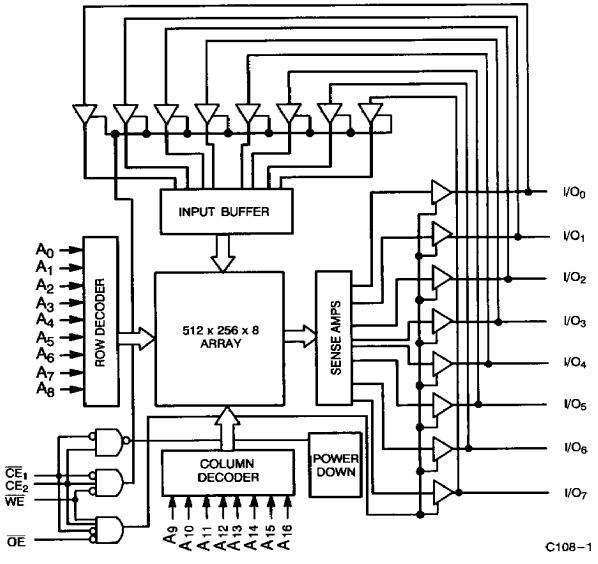
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C108 is available in a 32-pin rectangular leadless chip carrier and standard 600-mil-wide cerDIPs. The CY7C109 is available in standard 400-mil-wide DIPs and SOJs.

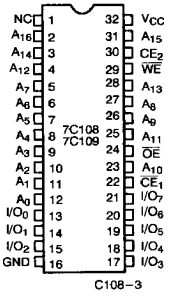
Logic Block Diagram



C108–1

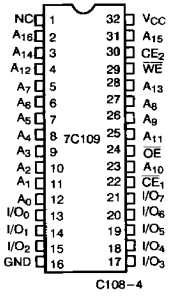
Pin Configurations

DIP
Top View



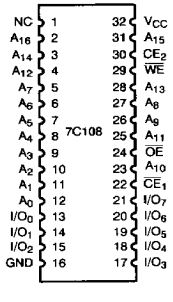
C108–3

SOJ
Top View



C108–4

LCC
Top View



C108–2

Selection Guide

		7C108–25 7C109–25	7C108–35 7C109–35	7C108–45 7C109–45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	150	125	115
	Military	150	125	115
Maximum Standby Current (mA)	Commercial	30	25	25
	Military	35	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage on V_{CC} Relative to GND[1] – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to + 7.0V

DC Input Voltage[1] ..... – 0.5V to + 7.0V

Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions		7C108–25 7C109–25 Min.	7C108–25 7C109–25 Max.	7C108–35 7C109–35 Min.	7C108–35 7C109–35 Max.	7C108–45 7C109–45 Min.	7C108–45 7C109–45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–300		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		150		125		115	mA
			Mil		150		125		115	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $CE_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Com'l		30		25		25	mA
			Mil		35		30		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $CE_1 \geq V_{CC}$ – 0.3V or $CE_2 \leq$ 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V or $V_{IN} \leq$ 0.3V, f=0	Com'l		10		10		10	mA
			Mil		10		10		10	

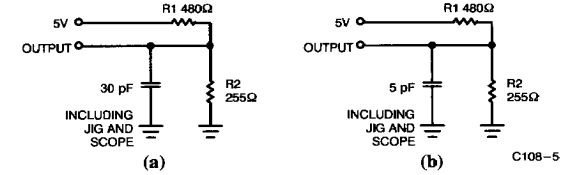
Capacitance[5]

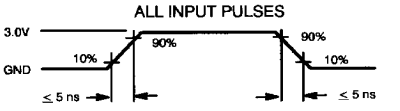
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

Notes:

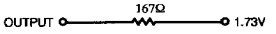
1. $V_{IL\,(min.)}$ = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics[2,6] Over the Operating Range

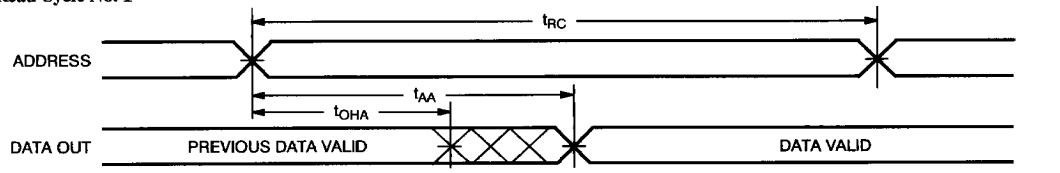
Parameters	Description	7C108–25 7C109–25 Min.	7C108–25 7C109–25 Max.	7C108–35 7C109–35 Min.	7C108–35 7C109–35 Max.	7C108–45 7C109–45 Min.	7C108–45 7C109–45 Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		10		15		20	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[8]	5		5		5		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[7,8]		10		15		20	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to Power-Down		25		35		45	ns
WRITE CYCLE[9,10]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7,8]		10		15		20	ns

Notes:

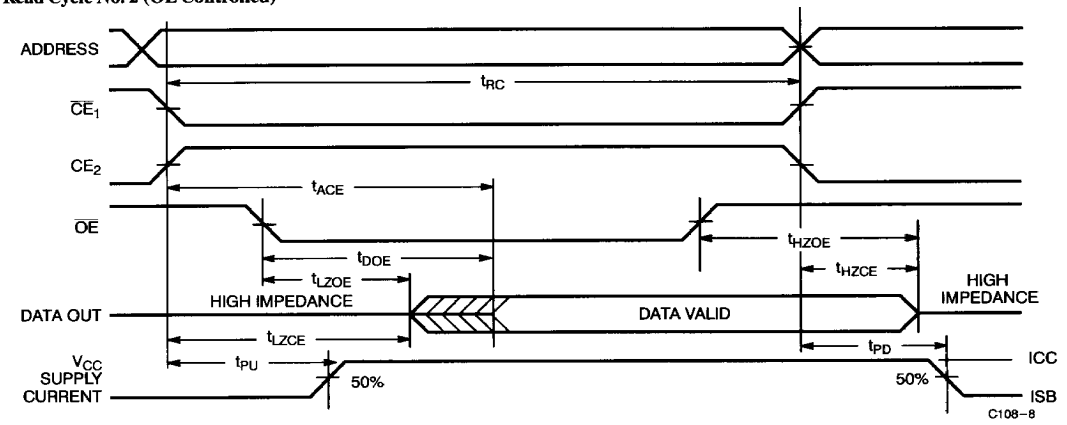
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

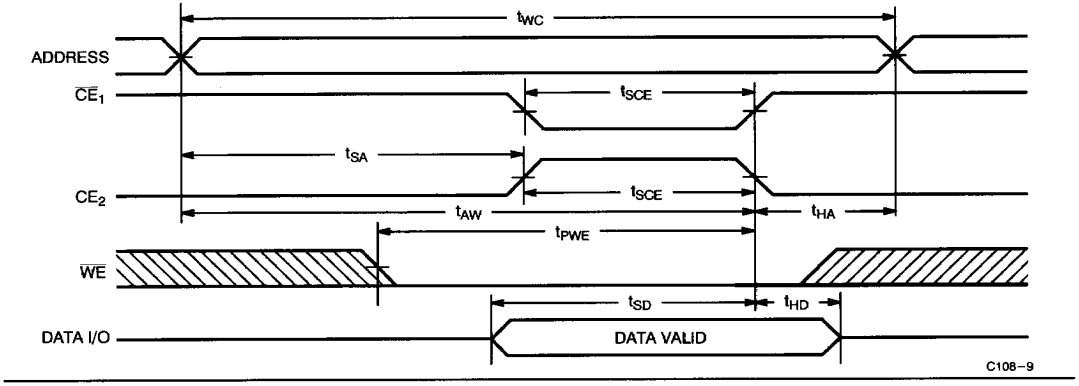
Read Cycle No. 1[11, 12]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[11, 13]



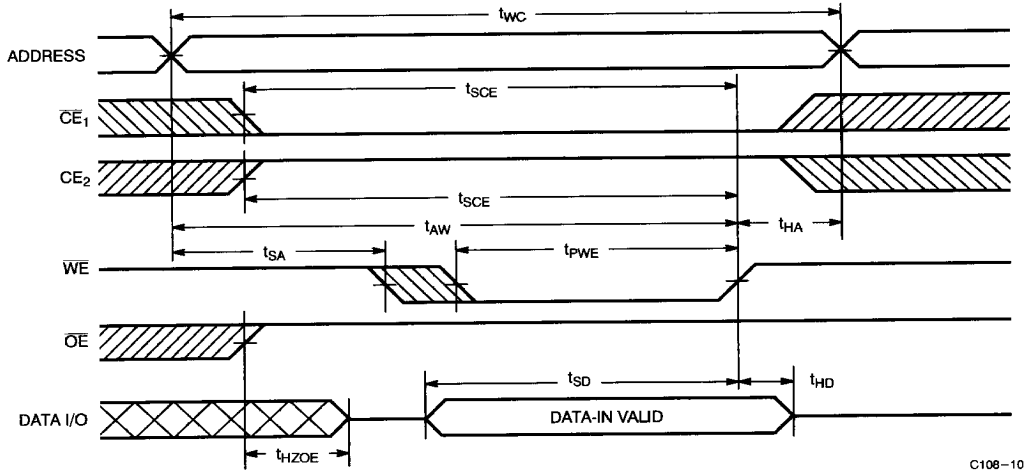
Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)[14, 15]



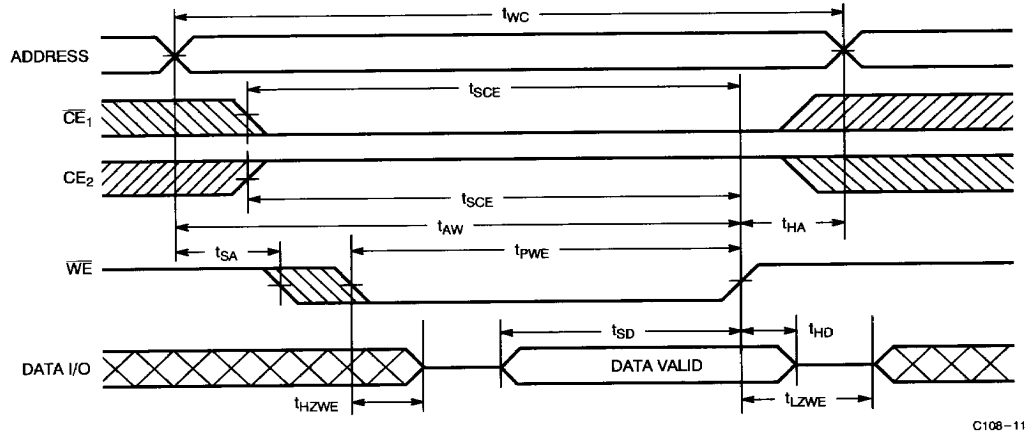
Notes:
11. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[14,15]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 15]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C108–25DC	D50	Commercial
	CY7C108–25LC	L75	
	CY7C108–25DMB	D50	Military
	CY7C108–25LMB	L75	
35	CY7C108–35DC	D50	Commercial
	CY7C108–35LC	L75	
	CY7C108–35DMB	D50	Military
	CY7C108–35LMB	L75	
45	CY7C108–45DC	D50	Commercial
	CY7C108–45LC	L75	
	CY7C108–45DMB	D50	Military
	CY7C108–45LMB	L75	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C109–25DC	D46	Commercial
	CY7C109–25PC	P43	
	CY7C109–25VC	V33	
	CY7C109–25DMB	D46	Military
35	CY7C109–35DC	D46	Commercial
	CY7C109–35PC	P43	
	CY7C109–35VC	V33	
	CY7C109–35DMB	D46	Military
45	CY7C109–45DC	D46	Commercial
	CY7C109–45PC	P43	
	CY7C109–45VC	V33	
	CY7C109–45DMB	D46	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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