

E10040VHM

ECL Gate Array with RAM

PRELIMINARY

DESCRIPTION

Fujitsu's E10040VHM array utilizes advanced technology to produce an array with high I/O capability, high density, high speed, and excellent power dissipation combined with an on-chip RAM of 40K bits. The internal structure allows up to 13,440 gates, including high-drive and I/O macrocells. High-drive internal macrocells allow a maximum fanout of 40. Interconnection is implemented with four layers of metallization. The E10040VHM is especially well suited for such high-performance applications as mainframe and supermini computers, high-end workstations, telecommunications, and instrumentation where RAM and logic are used in close proximity.

VH series ECL arrays are designed using Fujitsu's integrated design system software in conjunction with either an Amdahl 5860 or Fujitsu M-780 mainframe supercomputer. The VH series has an extensive cell library.

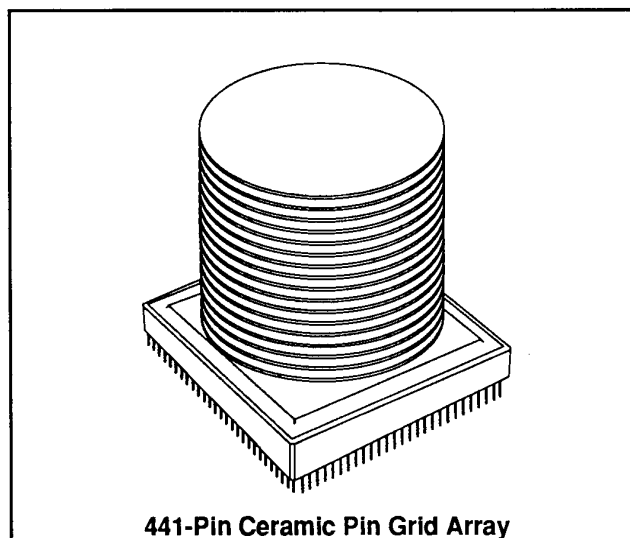
FEATURES

- High Performance Logic
 - 80 ps/gate typical at 2.95 mW¹
 - 135 ps/gate typical at 1.11 mW¹
- 13440 Maximum Equivalent Gates
- 40960 bit = (256w x 20b) x 8 RAM
- 3-level Series Gating
- Loaded Delay Performance
 - 250 ps/gate typical at 4.6 mW²
 - 300 ps/gate typical at 2.95 mW²
 - 350 ps/gate typical at 1.11 mW²
- RAM Performance
 - T_{AA} (max.) = 2.3 ns (latch through)
 - T_{AAC} (max.) = 3.0 ns (CK to Data out)
 - T_{CYCLE} (max.) = 3.5 ns
- High I/O Count
 - 288 I/O available
- I/O Options
 - 10KH ECL
- ECL Output Options
 - 25Ω, 50Ω, and 100Ω
 - Series terminated
- Advanced Packaging Solutions
 - 441-pin ceramic pin grid array package
 - Supplied with pre-attached heat sinks
 - Multiple heat sink options available
 - TAB processing used

E10040VHM Gate Array Summary	
Maximum Internal Gates	13440
Bits of RAM	40960
Maximum I/O	288
Maximum Outputs	222

Notes:

1. Unloaded F/I = F/O = 1, L = 0 mm.
2. Loaded F/I = F/O = 3, L = 3 mm.



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