T-46-23-12

RAMTRON

FM 1208 FRAM® Memory

4,096-Bit Nonvolatile Ferroelectric RAM
Product Preview

Features

- 4,096-Bit Nonvolatile Ferroelectric RAM Organized as 512w x 8b
- CMOS Technology with Integrated Ferroelectric Storage Cells
- Fully Synchronous Symmetrical Operation with Two Modes of Operation
  - Dynamic Mode Offers Unlimited Read/Write Endurance
  - Nonvolatile Mode Offers a Minimum of 10^8 Endurance Cycles
- Provides Single Memory Function for Storage of Both Data and Instructions
- On-Chip Data Protection Circuit
- 10-Year Data Retention without Power
- Dynamic Mode
  - 150ns Maximum Read Access
  - 300ns Maximum Read/Write Cycles
- Nonvolatile Mode
  - 250ns Maximum Read Access
  - 500ns Maximum Read/Write Cycles
- Single 5 Volt ±10% Supply
  - 44mW Maximum Dynamic Power at Minimum Cycle Time
  - 550μW Maximum Static Power
- CMOS/TTL Compatible I/O Pins
- 24-Pin Ceramic Skinny DIP and Plastic Skinny DIP and SOP Packages
- 0-70°C Ambient Operating Temperature Range

Description

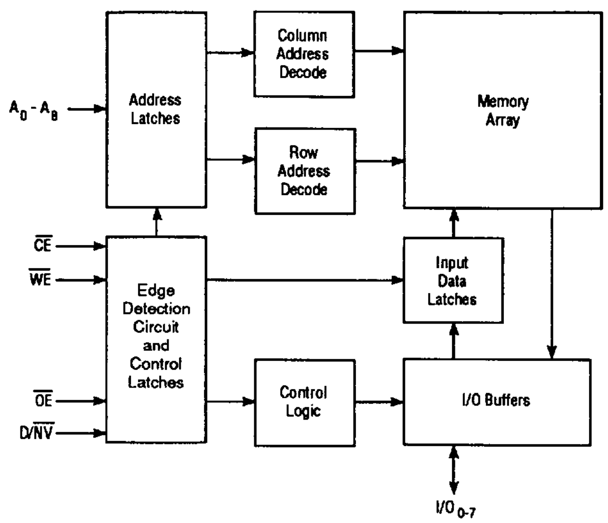
The FM 1208 is a bytewide ferroelectric RAM, or FRAM®, product organized as 512 x 8. FRAM memory products from Ramtron combine the read/write characteristics of semiconductor RAM with the nonvolatile retention of magnetic storage. The FM 1208 is manufactured in a 1.8 micron Si gate CMOS technology with the addition of integrated thin film ferroelectric storage cells developed and patented by Ramtron.

The ferroelectric cells developed by Ramtron exhibit two properties — high dielectric constant and spontaneous polarization — that have led to the development of a FRAM product with two modes of operation: dynamic and nonvolatile.

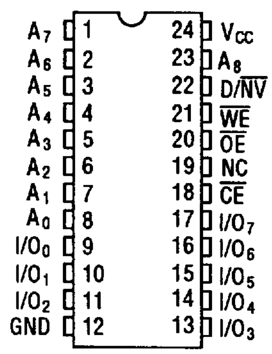
Nonvolatile applications that require unlimited read/write endurance can utilize the dynamic mode of operation with a mode conversion cycle (<50μs) to nonvolatile mode on power down or power loss. Applications that are not memory cycle intensive (<10^8 read/write cycles) can continuously operate the part in nonvolatile mode and eliminate the need for refresh and mode conversion.

Ramtron's FRAM products operate from a single +5 volt power supply and are TTL/CMOS compatible on all inputs and outputs. The FM 1208 utilizes the standard bytewide SRAM pinout with added mode pin.

Functional Diagram



Pin Configuration



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Pin Names

Pin Names	Function
A_0 - A_2	Column Address Inputs
A_3 - A_8	Row Address Inputs
I/O_0 - I/O_7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Ouput Enable Input
D/$\overline{NV}$	Mode Control Input
V_{CC}	+5 Volts
GND	Ground
NC	No Connect

E.S.D. Characteristics

Symbol	Parameter	Value
V_{ZAP} (1)	E.S.D. Tolerance	>2000 Volts

(1) Characterized to MIL-STD-883 test method 3015. Not tested.

Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	0 to +70°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V

AC Conditions of Test

AC Conditions	Test
Input Pulse Levels	0 to 3 V
Input Rise and Fall Time	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and CL = 50pF

DC Operating Conditions

T_A = 0° to 70°C Unless Otherwise Noted

Symbol	Parameters	Min	Max	Test Condition
V_{CC}	Power Supply Voltage	4.5V	5.5V	
I_{CC1}	Power Supply Current - Refresh	350µA[1]	8mA	V_{CC} = Max, $\overline{CE}$ Cycling at Minimum Cycle Time D/$\overline{NV}$ = V_{CC}, $I_{I/O}$ = 0mA, CMOS Input Levels, $\overline{OE}$ = $\overline{WE}$ = V_{CC}
I_{CC2}	Power Supply Current - Active		8mA	V_{CC} = Max, $\overline{CE}$ Cycling at Minimum Cycle Time CMOS Input Levels, $I_{I/O}$ = 0mA
I_{SB1}	Power Supply Current - Standby (CMOS)		100µA	V_{CC} = Max, $\overline{CE}$ = V_{CC}, D/$\overline{NV}$ = GND CMOS Input Levels, $I_{I/O}$ = 0mA
I_{SB2}	Power Supply Current - Standby (TTL)		1.2mA	V_{CC} = Max, $\overline{CE}$ = V_{IH}, D/$\overline{NV}$ = V_{IL} TTL Input Levels, $I_{I/O}$ = 0mA
I_{IL}	Input Leakage Current		10µA	V_{IN} = GND to V_{CC}
I_{OL}	Output Leakage Current		10µA	V_{OUT} = GND to V_{CC}
$I_{D/\overline{NV}}$	D/$\overline{NV}$ Pin Input Leakage Current		100µA	D/$\overline{NV}$ = V_{IH}
V_{IL}	Input Low Voltage	-1V	0.8V	
V_{IH}	Input High Voltage	2.0V	V_{CC} +1V	
V_{OL}	Output Low Voltage		0.4V	I_{OL} = 4.2mA
V_{OH}	Output High Voltage	2.4V		I_{OH} = -2mA

(1) Minimum refresh current measured at 15.6µs cycle time.

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Capacitance

$T_A = 25°C$, f = 1.0MHz, $V_{CC} = 5V$

Parameter	Description	Max	Test Condition
$C_{I/O}$ (1)	Input/Output Capacitance	8pF	$V_{I/O}$ = 0V
C_{IN} (1)	Input Capacitance	6pF	$V_{I/O}$ = 0V

(1) This parameter is periodically sampled and not 100% tested.

Mode Selection

H = V_{IH}, L = V_{IL}, X = Don't Care

$\overline{CE}$	D/$\overline{NV}$	$\overline{WE}$	$\overline{OE}$	I/O	Status
H	X	X	X	Output High-Z	Chip Not Selected
L	X	L	L	Output Data	Not Allowed
L	L	L	H	Input Data	Nonvolatile Write
L	L	H	L	Output Data	Nonvolatile Read/Conversion
L	L	H	H	Output High-Z	Nonvolatile Conversion
L	H	L	H	Input Data	Dynamic Write
L	H	H	L	Output Data	Dynamic Read/Refresh
L	H	H	H	Output High-Z	Dynamic Refresh

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Theory of Operation

The FM 1208 memory uses a two transistor, two capacitor memory structure illustrated below.

Dynamic Mode

The dynamic mode utilizes the high dielectric constant of the ferroelectric cells to store data as an electrical charge. During a write operation, data is transferred from the I/O pins to the bit lines (true and complement). When the word line pass transistor is enabled, the data voltage will charge the selected capacitors. Since the plate is grounded in this mode, the capacitor polarization does not switch and the stored charge must be periodically refreshed to offset circuit leakage. To read the memory, the selected memory cell address pass transistor connects the capacitors to the bit lines. The sense amplifier differentially senses the stored charge of each cell to detect the data value. The data is transferred to I/O buffers. Since the memory reference is destructive, the data is automatically restored to the cell by recharging the capacitors.

Since the polarity of the capacitors is not switched during dynamic mode operation, the memory can operate continuously at the minimum clock cycle rate during normal operation without fatiguing the memory cells, thus read/write endurance is unlimited. Data stored as an electric charge in dynamic mode can be made nonvolatile (at the time of a power loss) by selecting the nonvolatile mode and performing a mode conversion prior to loss of operating voltage. On power recovery, data can be recovered by performing a conversion operation before switching to the dynamic mode.

In the dynamic mode of operation, the memory is capable of 10^8 power-up/down cycles without degradation of its nonvolatile retention characteristics.

Nonvolatile Mode

The nonvolatile mode utilizes the bistable characteristic of the ferroelectric cell to store data. Operating the FM 1208 in continuous nonvolatile mode requires that the D/$\overline{NV}$ pin always be held low.

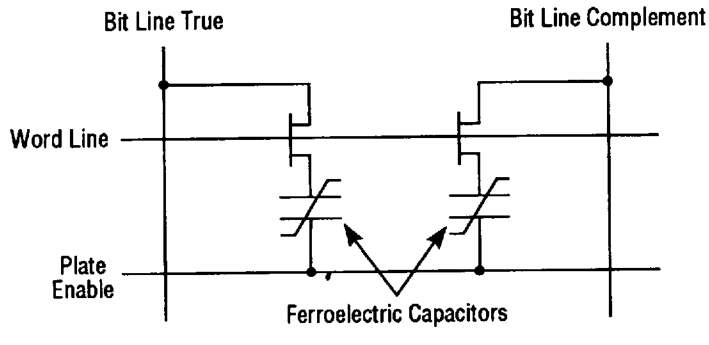
During a write operation, data is transferred from the I/O pins to the bit lines. When the word line pass transistor is enabled and the common plate is pulsed, the data will be stored by polarizing the ferroelectric cell in one of two states. To read data, the pass transistor is enabled and the sense amplifier senses the difference in polarization of the ferroelectric cells to determine the stored data state. Since the read operation is destructive, the data is then automatically rewritten back to the ferroelectric cell by switching the polarization. The memory can be cycled up to 10^8 cycles in continuous nonvolatile mode without degrading the data retention characteristics of the memory. Operation beyond 10^8 cycles will eventually result in nonvolatile data retention failure.

Operating the FM 1208 Continuously in Nonvolatile Mode

The FM 1208 can be operated continuously in the nonvolatile mode, polarizing the ferroelectric cells on every read and write cycle. This mode of operation does not require refresh operations or a mode conversion upon power down to retain data. The memory is limited to 10^8 endurance cycles, and unnecessary cycling of $\overline{CE}$ should be avoided while in the nonvolatile mode of operation.

The FM 1208 features a pull-down D/$\overline{NV}$ mode pin. The part will default to the nonvolatile mode of operation unless the D/$\overline{NV}$ pin is held high (D/$\overline{NV}$=V_{IH}).

Dual Memory Capacitor Cell



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Read Cycle (Dynamic and Nonvolatile Mode)

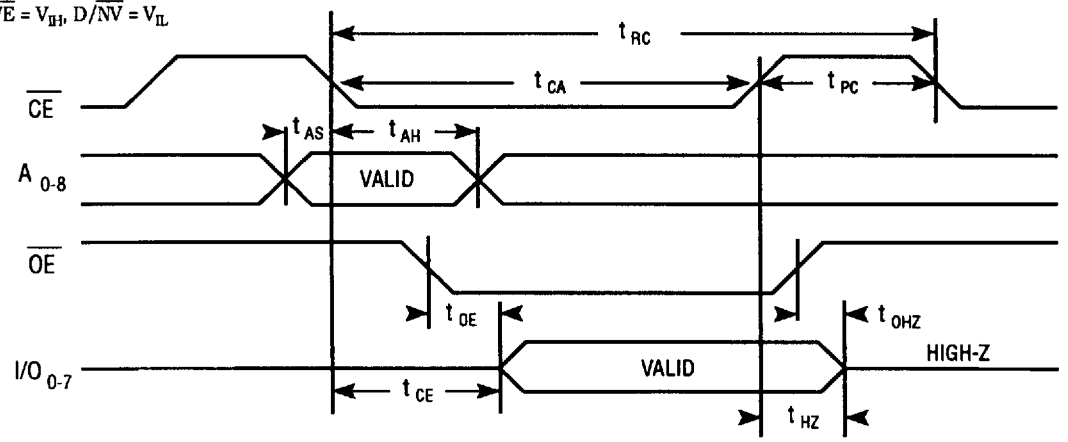
The FRAM memory operates synchronously using the $\overline{CE}$ signal as the clock. The memory read cycle time t_{RC} is measured between falling edges of $\overline{CE}$. The memory $\overline{CE}$ signal must be active time, t_{CA}. The memory requires a minimum precharge time t_{PC} to precharge the internal busses between operations.

The memory latches the address internally on the falling edge of $\overline{CE}$. The address data must meet a minimum setup time t_{AS} and hold time t_{AH} relative to a clock edge.

Read data is valid a maximum access time t_{CE} after the beginning of the read cycle. The $\overline{OE}$ signal is used to gate the data to the I/O pins. It must be enabled time t_{OE} prior to the time data is required on the I/O pins. Output data remains valid on the outputs until disabled by either the rising edge of $\overline{OE}$ or $\overline{CE}$. The output becomes high-Z after time t_{HZ} from the $\overline{CE}$ signal and time t_{OHZ} from the $\overline{OE}$ signal. The $\overline{WE}$ signal is high during the entire read operation.

Read Cycle Timing

Dynamic: $\overline{WE} = V_{IH}$, $D/\overline{NV} = V_{IH}$
Nonvolatile: $\overline{WE} = V_{IH}$, $D/\overline{NV} = V_{IL}$



Read Cycle AC Parameters

T_A = 0° to 70°C, V_{CC} = 5V +/- 10% Unless Otherwise Noted

Symbol	Parameter	JEDEC Symbol	Mode of Operation: Dynamic Min	Dynamic Max	Nonvolatile Min	Nonvolatile Max	Unit
t_{RC}	Read Cycle Time	t ELEL	300		500		ns
t_{CA}	Chip Enable Active Time		150	10,000	250	10,000	ns
t_{PC}	Precharge Time	t EHEL	150		250		ns
t_{AS}	Address Setup Time	t AVEL	0		0		ns
t_{AH}	Address Hold Time	t ELAX	30		30		ns
t_{CE}	Chip Enable Access Time	t ELQV		150		250	ns
t_{OE}	Output Enable Access Time	t OLQV	30		30		ns
t_{HZ}	Chip Enable to Output High-Z	t EHQZ		45		45	ns
t_{OHZ}	Output Enable to Output High-Z	t OHQZ		35		35	ns

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Write Cycle (Dynamic and Nonvolatile Mode)

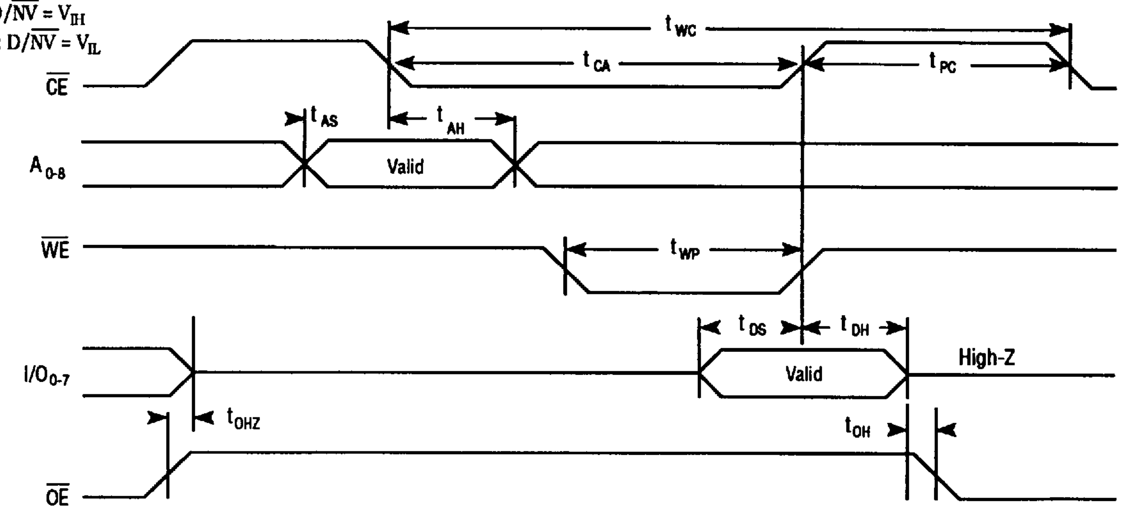
The FM 1208 operates synchronously using the $\overline{CE}$ signal as a clock. The memory write cycle time t_{WC} is measured between falling edges of $\overline{CE}$. The memory $\overline{CE}$ must be active time, t_{CA}. The memory requires a minimum precharge time t_{PC} to precharge the internal busses between operations.

The memory latches the addresses internally on the falling edge of $\overline{CE}$. The address data must meet a minimum setup time t_{AS} and hold time t_{AH} relative to the clock edge.

The data must be valid on the I/O pins time t_{DS} prior to the rising edge of $\overline{WE}$ and held time t_{DH} after $\overline{WE}$. $\overline{WE}$ must be stable time t_{WP} prior to the rising edge of $\overline{CE}$. The $\overline{OE}$ signal must disable the chip outputs time t_{OHZ} prior to placing data on the I/O pins to prevent a data conflict. $\overline{OE}$ must remain disabled until time t_{OH} after the data is removed from the bus.

Write Cycle Timing

Dynamic: D/$\overline{NV}$ = V_{IH}
Nonvolatile: D/$\overline{NV}$ = V_{IL}



Write Cycle AC Parameters

T_A = 0° to 70°C, V_{CC} = 5V +/- 10% Unless Otherwise Noted

Symbol	Parameter	JEDEC Symbol	Mode of Operation				Unit
			Dynamic		Nonvolatile		
			Min	Max	Min	Max	
t_{WC}	Write Cycle Time	t_{ELEL}	300		500		ns
t_{CA}	Chip Enable Active Time		150	10,000	250	10,000	ns
t_{PC}	Precharge Time	t_{EHEL}	150		250		ns
t_{AS}	Address Setup Time	t_{AVEL}	0		0		ns
t_{AH}	Address Hold Time	t_{ELAX}	30		30		ns
t_{WP}	Write Enable Pulse Width	t_{WLWH}	80		80		ns
t_{DS}	Data Setup Time	t_{DVWL}	40		40		ns
t_{DH}	Data Hold Time	t_{WLDX}	5		5		ns
t_{OHZ}	Output Enable to Output High-Z	t_{OHQZ}		35		35	ns
t_{OH}	Output Enable Hold Time		0		0		ns

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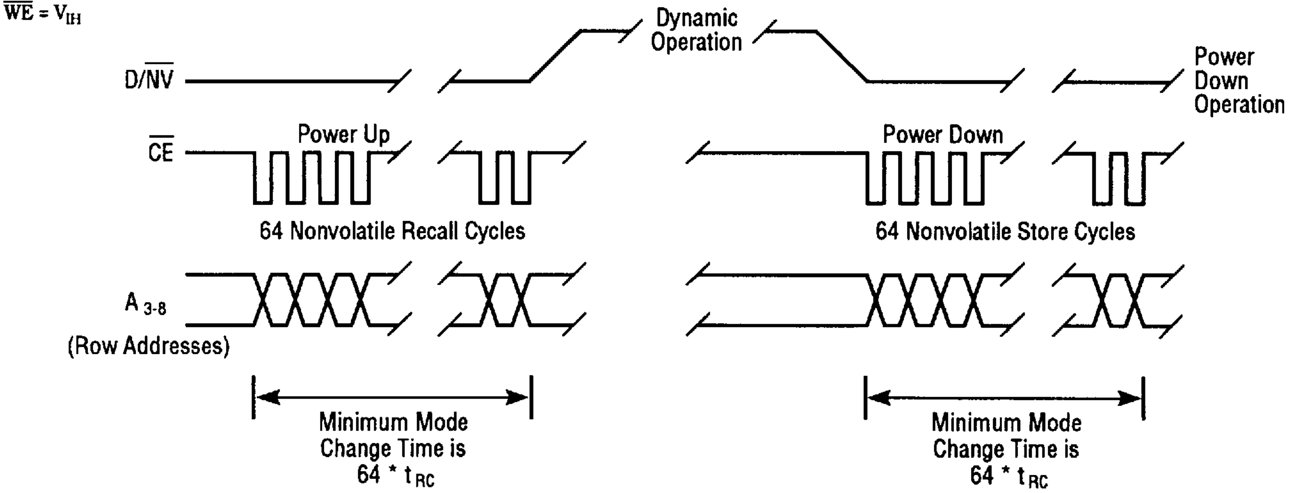
Mode Conversion (Dynamic and Nonvolatile Mode)

The D/$\overline{NV}$ input pin specifies the storage mode of the memory cells. During nonvolatile mode (D/$\overline{NV}$ = V_{IL}), data is stored by polarizing the ferroelectric capacitor. During dynamic mode (D/$\overline{NV}$ = V_{IH}), data is stored by charging the ferroelectric capacitor. During the transition from one mode to the other, it is necessary to convert data from one storage mode to the other. This is implemented by requiring that all row addresses be converted following a power-up/down mode transition.

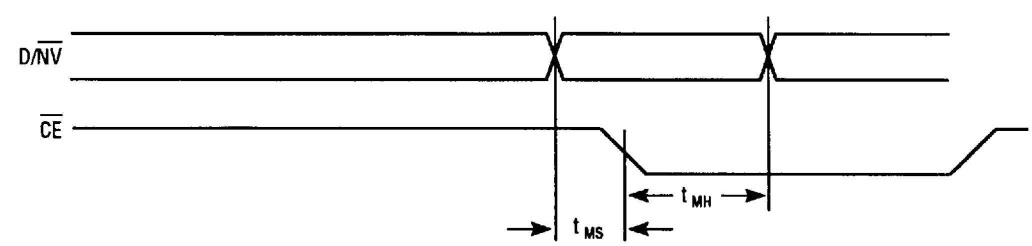
Similar to performing the refresh operation, the user must provide the addresses. After mode conversion to dynamic mode, refresh operations must continue at a rate sufficient to refresh all rows every 1msec. Since the memory is operated in dynamic mode during normal operation but nonvolatile storage is desired at power loss, it is necessary to detect the power failure in time to switch to nonvolatile mode and perform the data conversion operations prior to the power supply voltage dropping below V_{CC} minimum. The power-down conversion is implemented by performing conversion cycles at each row address following the nonvolatile mode transition. These conversion cycles can occur at the minimum nonvolatile mode cycle time of the memory, t_{RC}.

The mode select input is captured on the falling edge of $\overline{CE}$. Therefore, D/$\overline{NV}$ must be stable mode select setup time t_{MS} before $\overline{CE}$ and held mode select hold time t_{MH}, after $\overline{CE}$.

Mode Conversion



Mode Select



Symbol	Parameter	Min	Max	Unit
t_{MS}	Mode Select Setup Time	0		ns
t_{MH}	Mode Select Hold Time	30		ns

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Refresh Cycle (Dynamic Mode)

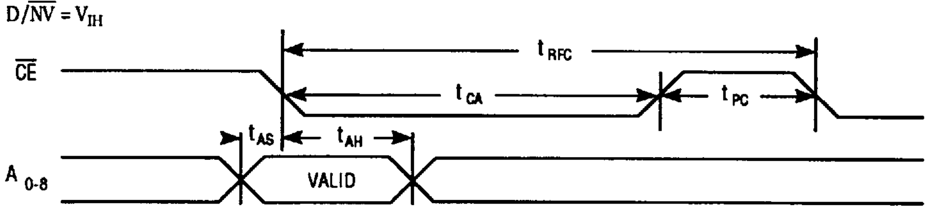
During refresh the memory operates synchronously using the $\overline{CE}$ signal as a clock. Every time a refresh cycle is desired the memory must be clocked with $\overline{CE}$. The refresh cycle time t_{RFC} is measured between falling edges of $\overline{CE}$. The memory requires a minimum chip enable active time t_{CA} to perform a refresh operation and a minimum precharge time t_{PC} to precharge the internal busses between operations.

Refresh operations must be performed at all row addresses every 1msec. This requires a refresh cycle every 15.6µsec.

Refresh is identical to a normal read operation but with the I/O bus disabled by $\overline{OE}$ = V_{IH}. The address must meet a minimum setup time t_{AS} and hold time t_{AH} relative to the $\overline{CE}$ clock edge.

Refresh Cycle Timing

$\overline{WE} = V_{IH}$, $\overline{OE} = V_{IH}$, $D/\overline{NV} = V_{IH}$



Refresh Cycle AC Parameters

T_A = 0° to 70°C, V_{CC} = 5V +/- 10% Unless Otherwise Noted

Symbol	Parameter	JEDEC Symbol	Mode of Operation				Unit
			Dynamic		Nonvolatile		
			Min	Max	Min	Max	
t_{RFC}	Refresh Cycle Time		300	15,600	500	15,600	ns
t_{CA}	Chip Enable Active Time		150		250		ns
t_{PC}	Precharge Time	t_{EHEL}	150		250		ns
t_{AS}	Address Setup Time	t_{AVEL}	0		0		ns
t_{AH}	Address Hold Time	t_{ELAX}	30		30		ns

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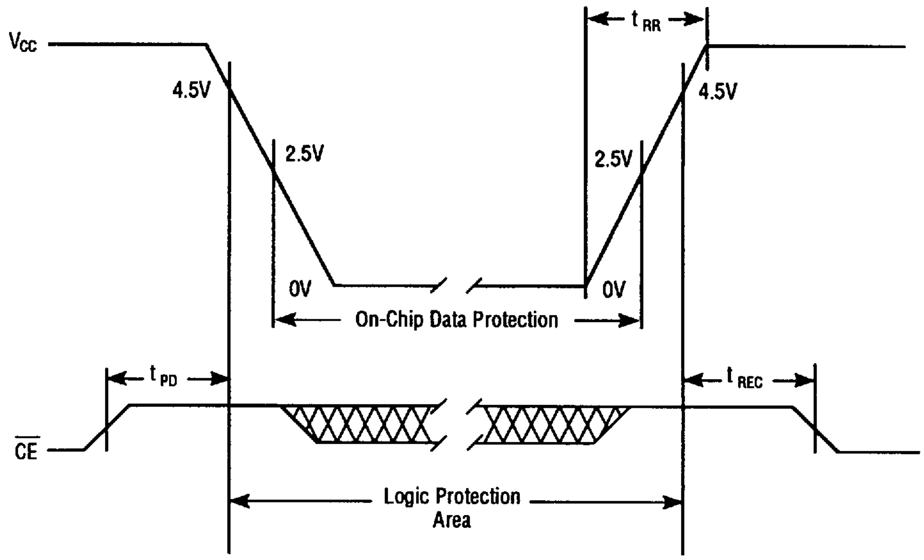
Power-Down/Power-Up Conditions

If the memory is operated in dynamic mode during normal operation, data must be made nonvolatile by switching to nonvolatile mode and converting all rows prior to operating voltage loss. If the memory is operating in nonvolatile mode continuously during normal operation, a mode conversion operation is not required before power cycling.

Care must be taken during power sequencing to prevent data loss resulting from memory operations during out of spec voltage conditions. This is managed by detecting power failure with sufficient time to disable memory operation time t_{PD} prior to V_{CC} reaching its lower specification, +4.5 volts. During power up, the memory operation should be disabled until time t_{REC} after V_{CC} reaches its operating voltage, +4.5 volts.

The memory has an on-chip data protection circuit which prevents memory operation when V_{CC} is less than +2.5 volts. This will protect the data in CMOS systems where the system control logic continues to function to +2.5 volts. However, external circuitry is required to force $\overline{CE}$ to a high level in systems with control logic that does not operate to +2.5 volts to prevent false memory operations from being initiated by the system control logic during this unspecified voltage range. There are a number of precision DC voltage detector circuits available to implement this function.

Power-Down/Power-Up Conditions



Power-Down/Power-Up AC Parameters

Symbol	Parameter	Min	Max	Unit
t_{PD}	Control Signals Stable to Power-Down	250		ns
t_{REC}	Power-Up to Operation		250	ns
t_{RR}	Power-Up Ramp Rate (0-5V)	150		µs

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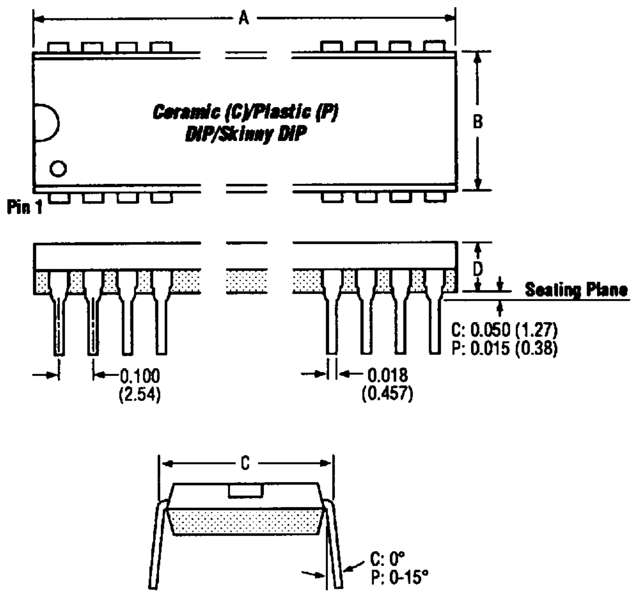
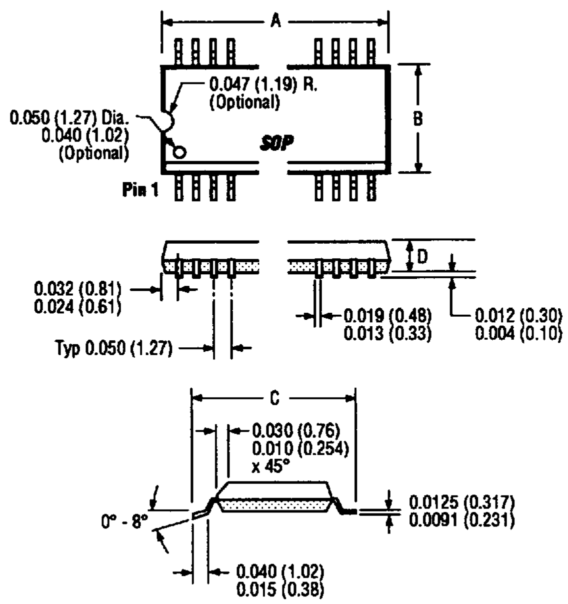
Packaging Information

Package	Type	Dimensions in Inches (Millimeters)			
		FM 1208 24-Pin			
		A	B	C	D
Ceramic DIP	D	1.200 (30.48)	0.595 (15.113)	0.600 (15.24)	0.100 (2.54)
Ceramic Skinny DIP	DS	1.200 (30.48)	0.295 (7.49)	0.300 (7.62)	0.100 (2.54)
Plastic DIP	P	1.250 (31.75)	0.540 (13.72)	0.600 (15.24)	0.150 (3.81)
Plastic Skinny DIP	PS	1.185 (30.10)	0.260 (6.60)	0.300 (7.62)	0.130 (3.30)
Plastic SOP	S	0.614 (15.59) 0.598 (15.19)	0.300 (7.62) 0.287 (7.29)	0.416 (10.57) 0.398 (10.11)	0.094 (2.34) 0.090 (2.29)





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Ordering Information

FM 1208 - 250 D C

- **Commercial Temperature Range (0-70°C)**
- **Package Type (24-Pin)**
  - D - Ceramic DIP
  - DS - Ceramic Skinny DIP
  - P - Plastic DIP
  - PS - Plastic Skinny DIP
  - S - Plastic SOP
- **Nonvolatile Access Time (ns)**
  - 250
- **Memory Configuration**
  - 1208 512 x 8
- **Ramtron Ferroelectronic Memory**