

8388608-word $\times$ 8-bit Dynamic Random Access Memory

HITACHI

ADE-203-458(A) (Z)
Preliminary
Rev. 0.1
Apr. 30, 1996

The Hitachi HM5164805A Series, HM5165805A Series are CMOS dynamic RAMs organized 8,388,608-word $\times$ 8-bit. They employ the most advanced CMOS technology for high performance and low power. The HM5164805A Series, HM5165805A Series offer Extended Data Out (EDO) Page Mode as a high speed access mode.

[illegible]

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.



HM5164805A Series, HM5165805A Series

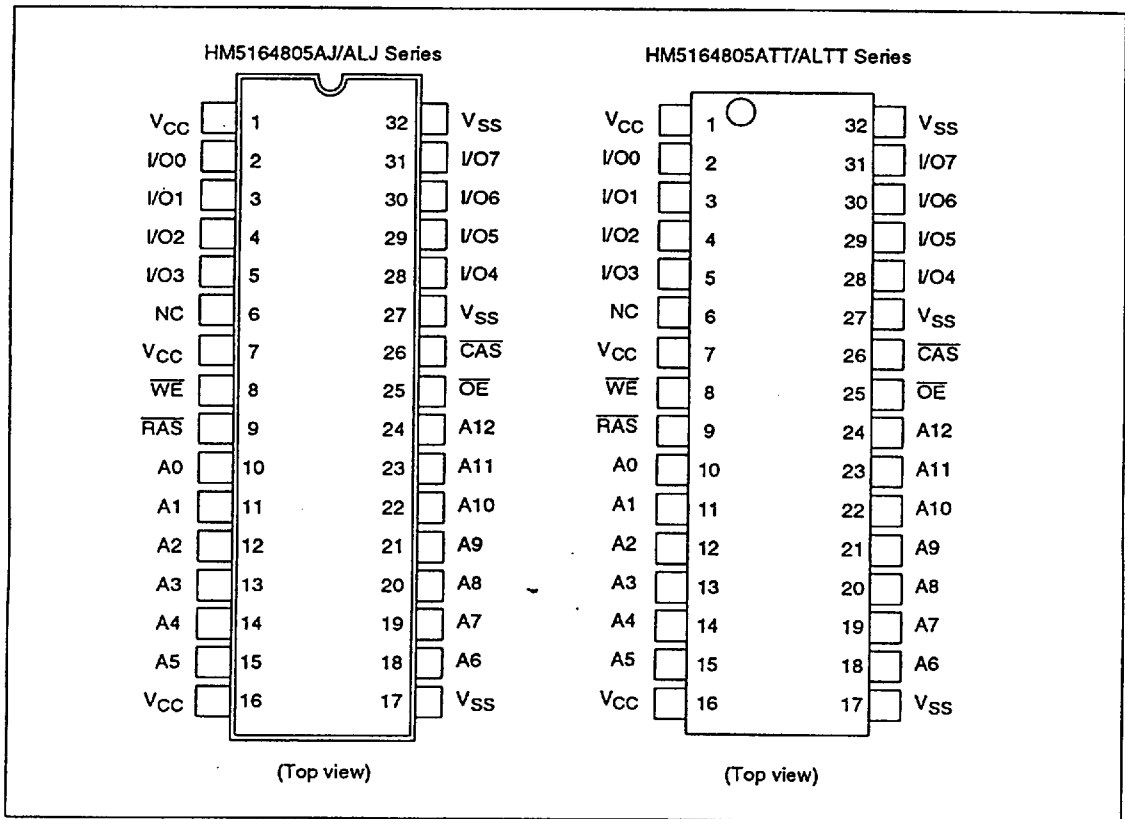
- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh (L-version)
- Battery backup operation (L-version)

Ordering Information

Type No.	Access time	Package
HM5164805AJ-5	50 ns	400-mil 32-pin plastic SOJ (CP-32DC)
HM5164805AJ-6	60 ns	
HM5164805AJ-7	70 ns	
HM5164805ALJ-5	50 ns	
HM5164805ALJ-6	60 ns	
HM5164805ALJ-7	70 ns	
HM5165805AJ-5	50 ns	
HM5165805AJ-6	60 ns	
HM5165805AJ-7	70 ns	
HM5165805ALJ-5	50 ns	
HM5165805ALJ-6	60 ns	
HM5165805ALJ-7	70 ns	
HM5164805ATT-5	50 ns	400-mil 32-pin plastic TSOP II (TTP-32DC)
HM5164805ATT-6	60 ns	
HM5164805ATT-7	70 ns	
HM5164805ALTT-5	50 ns	
HM5164805ALTT-6	60 ns	
HM5164805ALTT-7	70 ns	
HM5165805ATT-5	50 ns	
HM5165805ATT-6	60 ns	
HM5165805ATT-7	70 ns	
HM5165805ALTT-5	50 ns	
HM5165805ALTT-6	60 ns	
HM5165805ALTT-7	70 ns	

HITACHI

Pin Arrangement



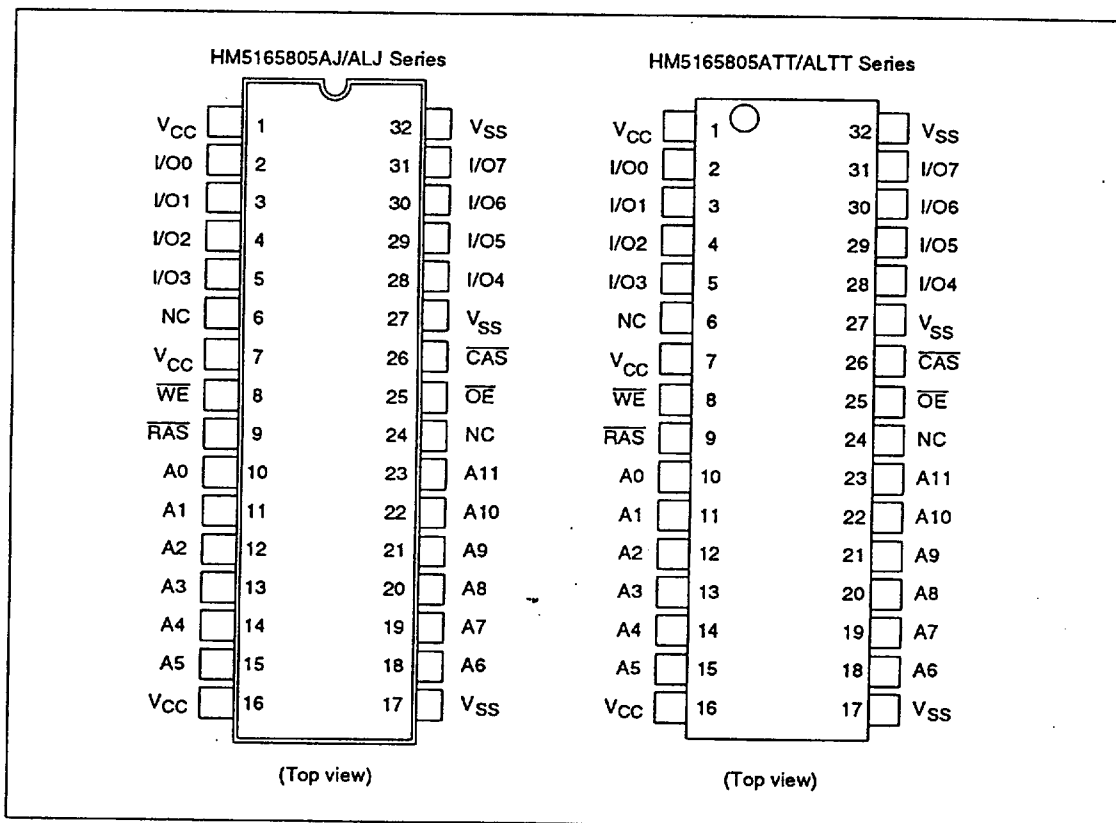
Pin Description

Pin name	Function
A0 to A12	Address input — Row/Refresh address A0 to A12 — Column address A0 to A9
I/O0 to I/O7	Data input/Data output
RAS	Row address strobe
CAS	Column address strobe
WE	Read/Write enable
OE	Output enable
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

HITACHI

HM5164805A Series, HM5165805A Series

Pin Arrangement

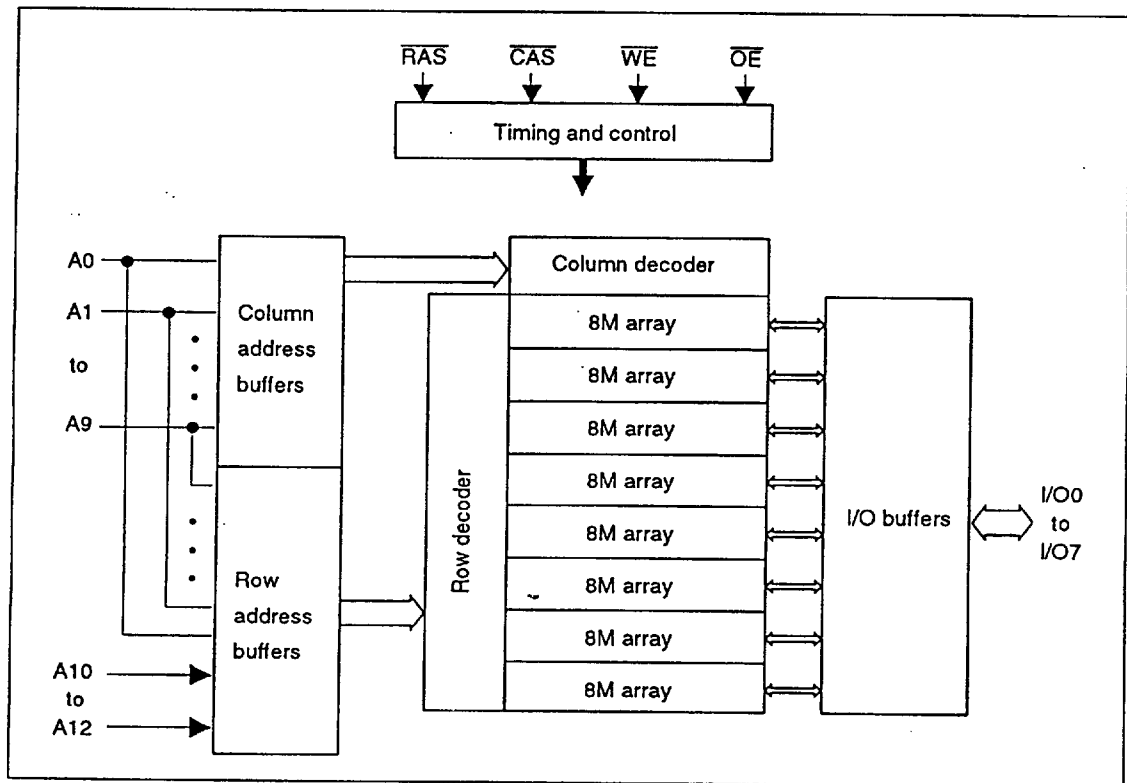


Pin Description

Pin name	Function
A0 to A11	Address input — Row/Refresh address A0 to A11 — Column address A0 to A10
I/O0 to I/O7	Data input/Data output
RAS	Row address strobe
CAS	Column address strobe
WE	Read/Write enable
OE	Output enable
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

HITACHI

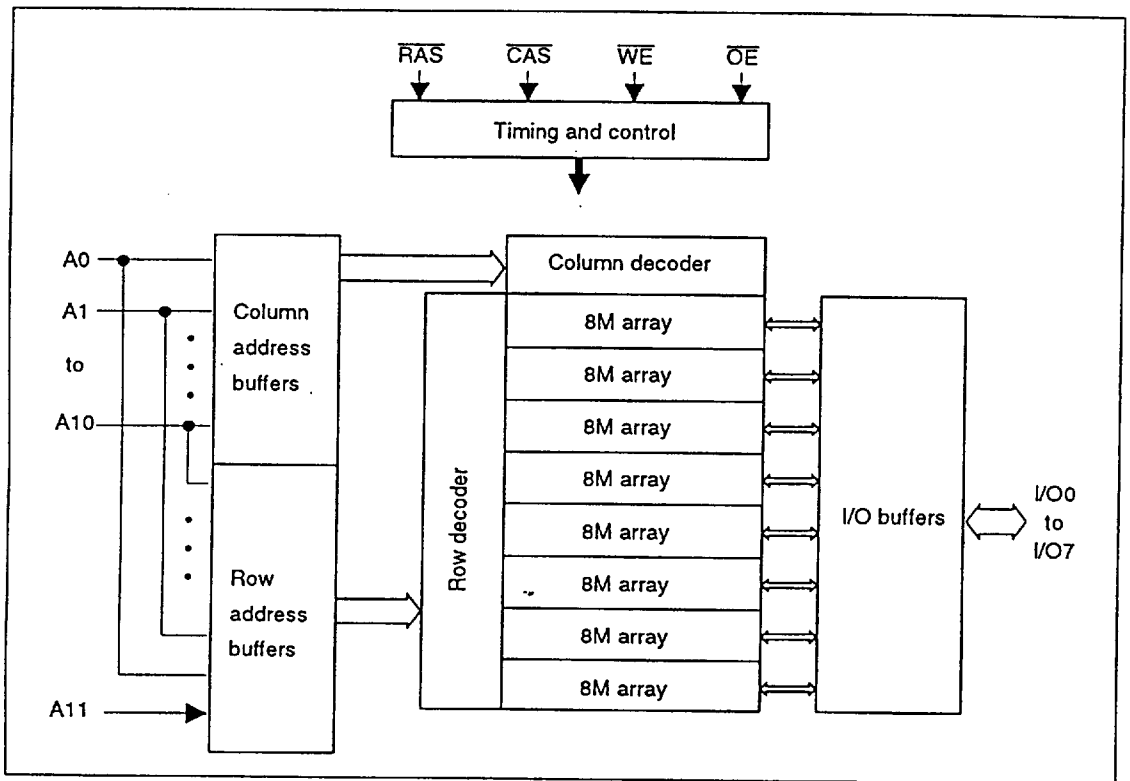
Block Diagram (HM5164805A Series)



HITACHI

HM5164805A Series, HM5165805A Series

Block Diagram (HM5165805A Series)



HITACHI

HM5164805A Series, HM5165805A Series

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{ss}	V_T	-0.5 to $V_{cc} + 0.5$ (≤ 4.6 V (max))	V
Supply voltage relative to V_{ss}	V_{cc}	-0.5 to $+4.6$	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to $+70$	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to $+125$	$^{\circ}\text{C}$

Recommended DC Operating Conditions ($T_a = 0$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{cc}	3.0	3.3	3.6	V	1, 2
Input high voltage	V_{IH}	2.0	—	$V_{cc} + 0.3$	V	1
Input low voltage	V_{IL}	-0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{ss} .

2. The supply voltage with all V_{cc} pins must be on the same level. The supply voltage with all V_{ss} pins must be on the same level.

HITACHI

HM5164805A Series, HM5165805A Series

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HM5164805A Series)

HM5164805A									
Parameter	Symbol	-5		-6		-7		Unit	Test conditions
		Min	Max	Min	Max	Min	Max		
Operating current* ^{1, *2}	I _{CC1}	—	TBD	—	135	—	115	mA	t _{RC} = min
Standby current	I _{CC2}	—	TBD	—	2	—	2	mA	TTL interface RAS, CAS = V _{IN} Dout = High-Z
		—	TBD	—	1	—	1	mA	CMOS interface RAS, CAS ≥ V _{CC} - 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	TBD	—	TBD	—	TBD	μA	CMOS interface RAS, CAS ≥ V _{CC} - 0.2 V Dout = High-Z
RAS-only refresh current* ²	I _{CC3}	—	TBD	—	135	—	115	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	TBD	—	5	—	5	mA	RAS = V _{IN} , CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	TBD	—	150	—	130	mA	t _{RC} = min
EDO page mode current* ^{1, *3}	I _{CC7}	—	TBD	—	145	—	125	mA	t _{HPC} = min
Battery backup current* ⁴ (Standby with CBR refresh) (L-version)	I _{CC10}	—	TBD	—	TBD	—	TBD	μA	CMOS interface Dout = High-Z, CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	TBD	—	TBD	—	TBD	μA	CMOS interface RAS, CAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _I	TBD	TBD	-10	10	-10	10	μA	0 V ≤ Vin ≤ V _{CC} + 0.3
Output leakage current	I _{LO}	TBD	TBD	-10	10	-10	10	μA	0 V ≤ Vin ≤ V _{CC} + 0.3 Dout = disable
Output high voltage	V _{OH}	TBD	TBD	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = -2 mA
Output low voltage	V _{OL}	TBD	TBD	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while RAS = V_{il}.

3. Address can be changed once or less within one page mode cycle t_{HPC}.

4. V_{ih} ≥ V_{CC} - 0.2 V, 0 V ≤ V_{il} ≤ 0.2 V.

HITACHI

HM5164805A Series, HM5165805A Series

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HM5165805A Series)

HM5165805A									
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current ^{*1, *2}	I _{CC1}	—	TBD	—	185	—	165	mA	t _{RC} = min
Standby current	I _{CC2}	—	TBD	—	2	—	2	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z
		—	TBD	—	1	—	1	mA	CMOS interface RAS, CAS ≥ V _{CC} - 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	TBD	—	TBD	—	TBD	μA	CMOS interface RAS, CAS ≥ V _{CC} - 0.2 V Dout = High-Z
RAS-only refresh current ^{*2}	I _{CC3}	—	TBD	—	185	—	165	mA	t _{RC} = min
Standby current ^{*1}	I _{CC5}	—	TBD	—	5	—	5	mA	RAS = V _{IH} , CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	TBD	—	150	—	130	mA	t _{RC} = min
EDO page mode current ^{*1, *3}	I _{CC7}	—	TBD	—	145	—	125	mA	t _{HPC} = min
Battery backup current ^{*4} (Standby with CBR refresh) (L-version)	I _{CC10}	—	TBD	—	TBD	—	TBD	μA	CMOS interface Dout = High-Z, CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	TBD	—	TBD	—	TBD	μA	CMOS interface RAS, CAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _I	TBD	TBD	-10	10	-10	10	μA	0 V ≤ Vin ≤ V _{CC} + 0.3 V
Output leakage current	I _{LO}	TBD	TBD	-10	10	-10	10	μA	0 V ≤ Vin ≤ V _{CC} + 0.3 V Dout = disable
Output high voltage	V _{OH}	TBD	TBD	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = -2 mA
Output low voltage	V _{OL}	TBD	TBD	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while RAS = V_{IL}.

3. Address can be changed once or less within one page mode cycle t_{HPC}.

4. V_{IH} ≥ V_{CC} - 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

HITACHI

HM5164805A Series, HM5165805A Series

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{i1}	—	5	pF	1
Input capacitance (Clocks)	C_{i2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	C_{io}	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{RAS}}$ and $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

HITACHI

HM5164805A Series, HM5165805A Series

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0 \text{ V}$) *1. *2. *3.*18

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: $V_{IL} = 0 \text{ V}$, $V_{IH} = 3 \text{ V}$
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5164805A/HM5165805A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	TBD	—	104	—	124	—	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	TBD	—	40	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	TBD	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	TBD	TBD	60	10000	70	10000	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	TBD	TBD	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	TBD	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	TBD	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	TBD	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	TBD	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	TBD	TBD	20	45	20	52	ns	3
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	TBD	TBD	15	30	15	35	ns	4
$\overline{\text{RAS}}$ hold time	t_{RSH}	TBD	—	15	—	18	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	TBD	—	48	—	58	—	ns	20
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	TBD	—	5	—	5	—	ns	
$\overline{\text{OE}}$ to Din delay time	t_{OED}	TBD	—	15	—	18	—	ns	5
$\overline{\text{OE}}$ delay time from Din	t_{DZO}	TBD	—	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	t_{DZC}	TBD	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	TBD	TBD	2	50	2	50	ns	7

HITACHI

HM5164805A Series, HM5165805A Series

Read Cycle

HM5164805A/HM5165805A									
Parameter	Symbol	-5		-6		-7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	TBD	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	TBD	—	15	—	18	ns	9, 10, 16
Access time from address	t_{AA}	—	TBD	—	30	—	35	ns	9, 11, 16
Access time from $\overline{\text{OE}}$	t_{OEA}	—	TBD	—	15	—	18	ns	9
Read command setup time	t_{RCS}	TBD	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	TBD	—	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	TBD	—	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	TBD	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	TBD	—	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	TBD	—	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	TBD	—	0	—	0	—	ns	
Output data hold time	t_{OH}	TBD	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	TBD	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	TBD	—	15	—	15	ns	13, 19
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	TBD	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	TBD	—	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	TBD	—	3	—	3	—	ns	
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	TBD	—	15	—	15	ns	19
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	TBD	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	TBD	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	TBD	—	15	—	18	—	ns	

HITACHI

HM5164805A Series, HM5165805A Series

Write Cycle

		HM5164805A/HM5165805A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t _{WCS}	TBD	—	0	—	0	—	ns	14
Write command hold time	t _{WCH}	TBD	—	10	—	13	—	ns	
Write command pulse width	t _{WP}	TBD	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t _{RWL}	TBD	—	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t _{CWL}	TBD	—	10	—	13	—	ns	
Data-in setup time	t _{DS}	TBD	—	0	—	0	—	ns	
Data-in hold time	t _{DH}	TBD	—	10	—	13	—	ns	

Read-Modify-Write Cycle

		HM5164805A/HM5165805A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	TBD	—	149	—	175	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	TBD	—	78	—	91	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	TBD	—	33	—	39	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	TBD	—	48	—	56	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	TBD	—	15	—	18	—	ns	

Refresh Cycle

		HM5164805A/HM5165805A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{\text{CAS}}$ setup time (CBR refresh cycle)	t_{CSR}	TBD	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ hold time (CBR refresh cycle)	t_{CHR}	TBD	—	10	—	10	—	ns	
$\overline{\text{WE}}$ setup time (CBR refresh cycle)	t_{WRP}	TBD	—	0	—	0	—	ns	
$\overline{\text{WE}}$ hold time (CBR refresh cycle)	t_{WRH}	TBD	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	t_{RPC}	TBD	—	0	—	0	—	ns	

HITACHI

HM5164805A Series, HM5165805A Series

EDO Page Mode Cycle

		HM5164805A/HM5165805A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t_{HPC}	TBD	—	25	—	30	—	ns	18
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	TBD	—	100000	—	100000	ns	15
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	TBD	—	35	—	40	ns	9, 16
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	TBD	—	35	—	40	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	TBD	—	3	—	3	—	ns	9, 16
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	TBD	—	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	TBD	—	10	—	10	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	TBD	—	35	—	40	—	ns	
Write pulse width during $\overline{CAS}$ precharge	t_{WPE}	TBD	—	10	—	10	—	ns	
$\overline{OE}$ precharge time	t_{OEP}	TBD	—	10	—	10	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HM5164805A/HM5165805A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode read-modify-write cycle time	t_{HPRWC}	TBD	—	68	—	79	—	ns	
WE delay time from $\overline{CAS}$ precharge	t_{CPW}	TBD	—	54	—	62	—	ns	14

Refresh (HM5164805A Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	64	ms	8192 cycles
Refresh period (L-version)	t_{REF}	128	ms	8192 cycles

Refresh (HM5165805A Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	64	ms	4096 cycles
Refresh period (L-version)	t_{REF}	128	ms	4096 cycles

HITACHI

HM5164805A Series, HM5165805A Series

Self Refresh Mode (L-version)

		HM5164805AL/HM5165805AL							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
RAS pulse width (self refresh)	t _{RASS}	TBD	—	100	—	100	—	μs	
RAS precharge time (self refresh)	t _{RPS}	TBD	—	110	—	130	—	ns	
CAS hold time (self refresh)	t _{CHS}	TBD	—	–50	—	–50	—	ns	

Notes: 1. AC measurements assume $t_r = 2 \text{ ns}$.

- An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh).
- Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
- Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
- Either t_{OED} or t_{CDD} must be satisfied.
- Either t_{DZO} or t_{DZC} must be satisfied.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
- Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
- Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\geq t_{\text{RAD}} + t_{\text{AA}}$ (max).
- Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\leq t_{\text{RAD}} + t_{\text{AA}}$ (max).
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
- t_{OFF} (max), t_{DEZ} (max), t_{WEZ} (max) and t_{OFR} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
- t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}$ (min), $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), and $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min), or $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min) and $t_{\text{CPW}} \geq t_{\text{CPW}}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- t_{RASp} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
- Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
- All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
- t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2 t_r$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
- Output is disable after both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ go to high.
- t_{CSH} (min) can be achieved when $t_{\text{RCD}} \leq t_{\text{CSH}}$ (min) - t_{CAS} (min).

HITACHI

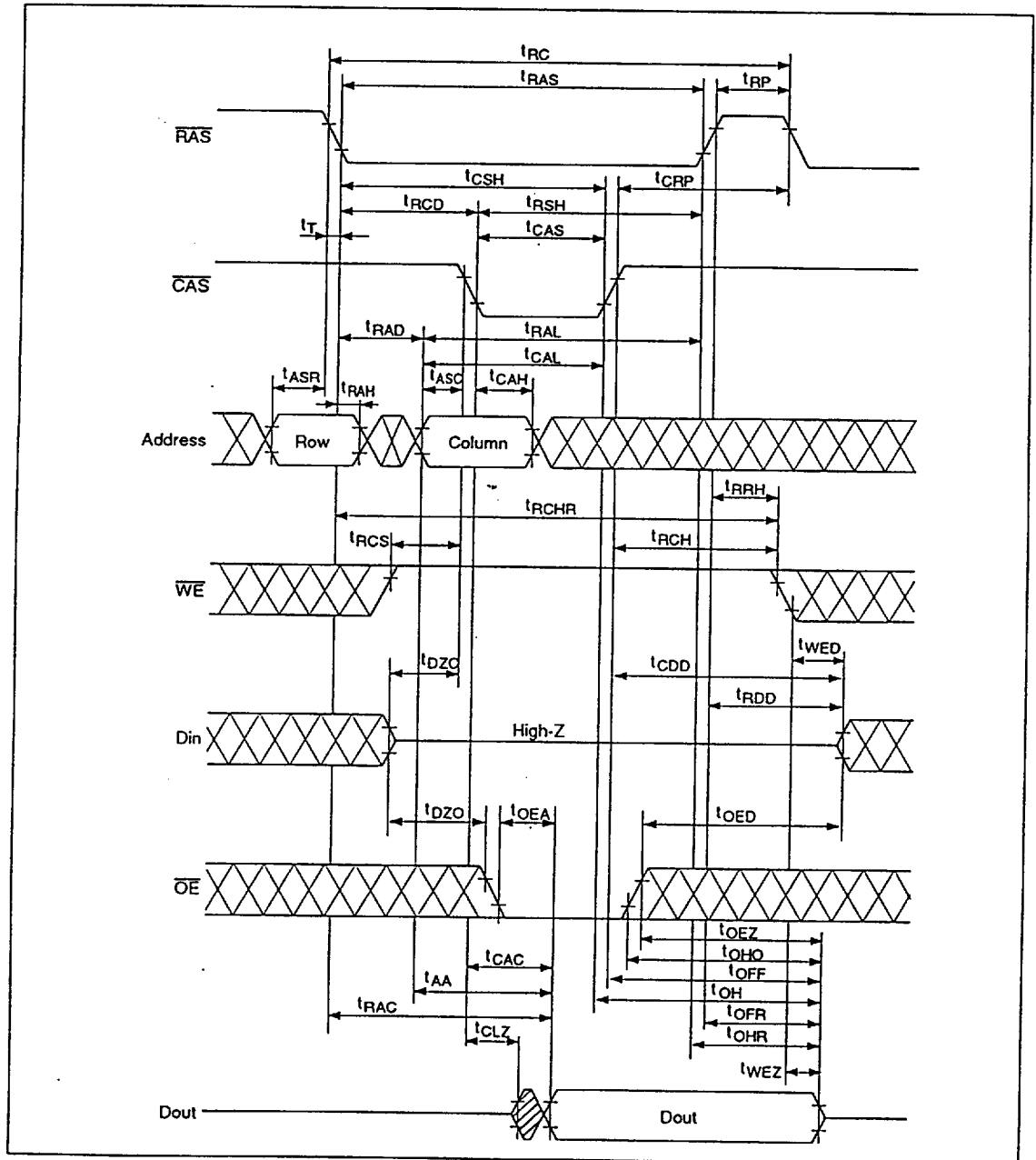
HM5164805A Series, HM5165805A Series

21. Please do not use t_{PASS} timing, $10 \mu\text{s} \leq t_{\text{PASS}} \leq 100 \mu\text{s}$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{\text{PASS}} > 100 \mu\text{s}$, then $\overline{\text{RAS}}$ precharge time should use t_{RPS} instead of t_{RP} .
22. CBR burst refresh or 4096 cycles of distributed CBR refresh with $15.6 \mu\text{s}$ interval should be executed within 64 ms immediately after exiting from and before entering into the self refresh mode.
23. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
24.  H or L (H: $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$, L: $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$)
 Invalid Dout

HITACHI

Timing Waveforms*24

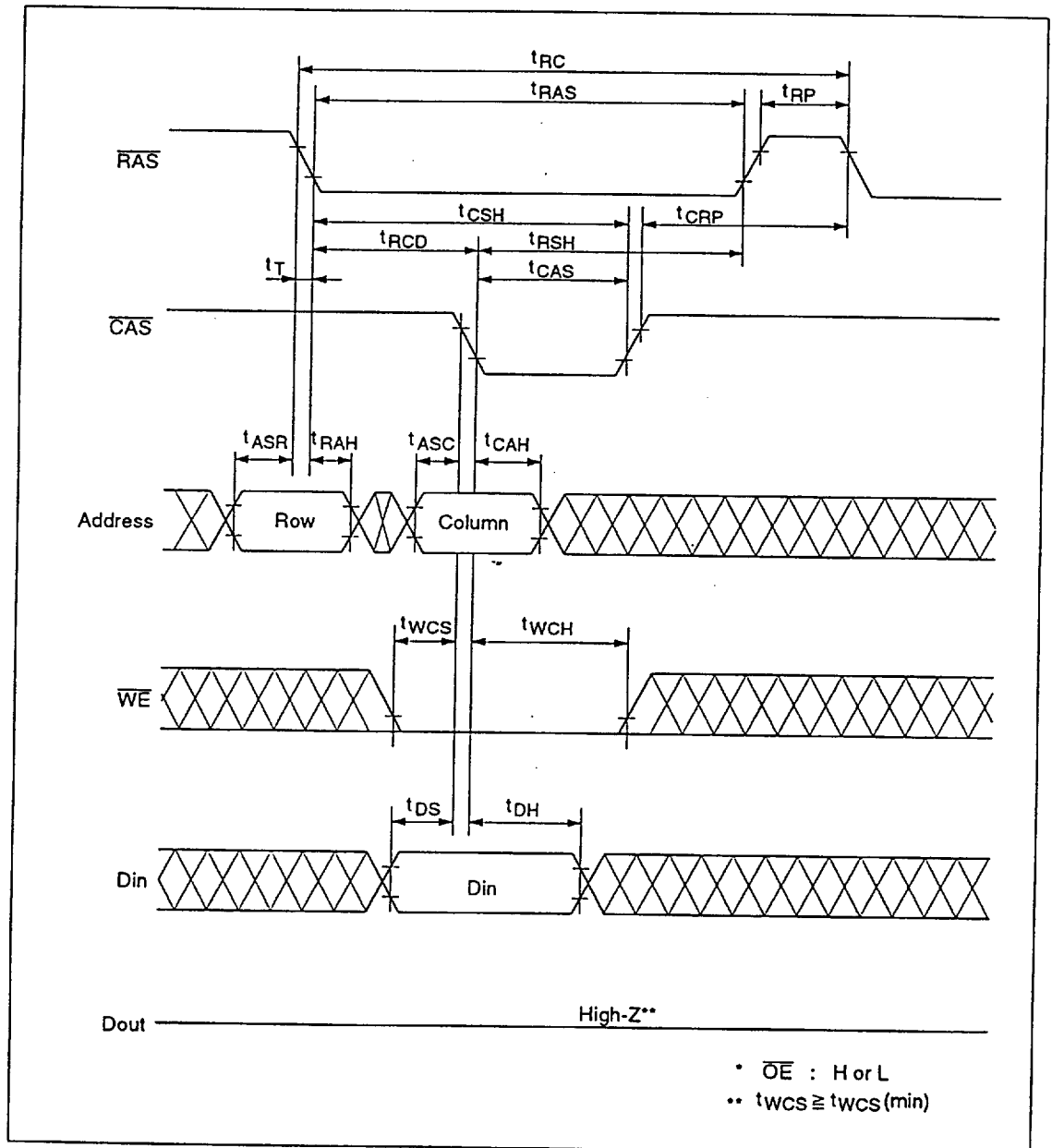
Read Cycle



HITACHI

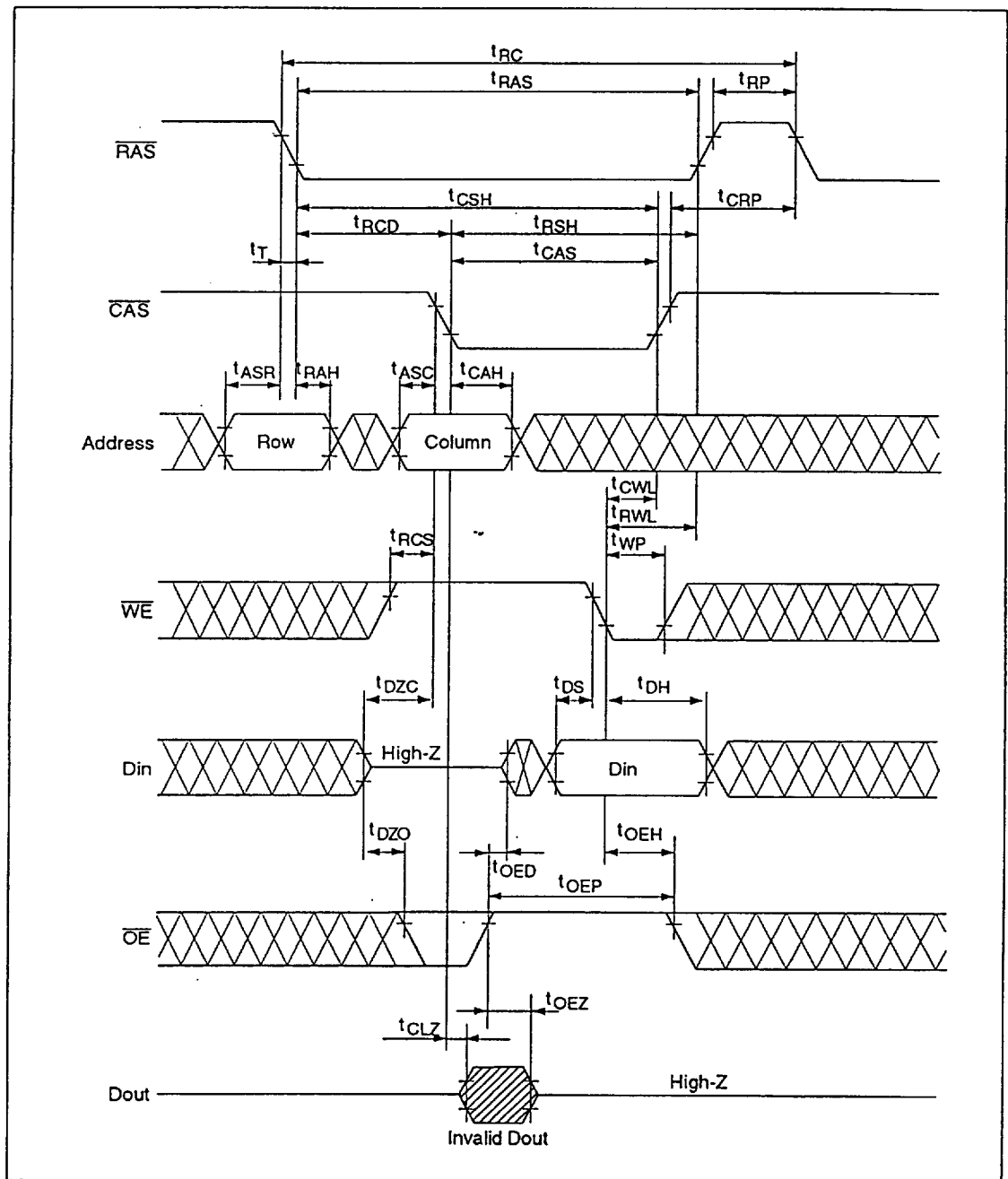
HM5164805A Series, HM5165805A Series

Early Write Cycle



HITACHI

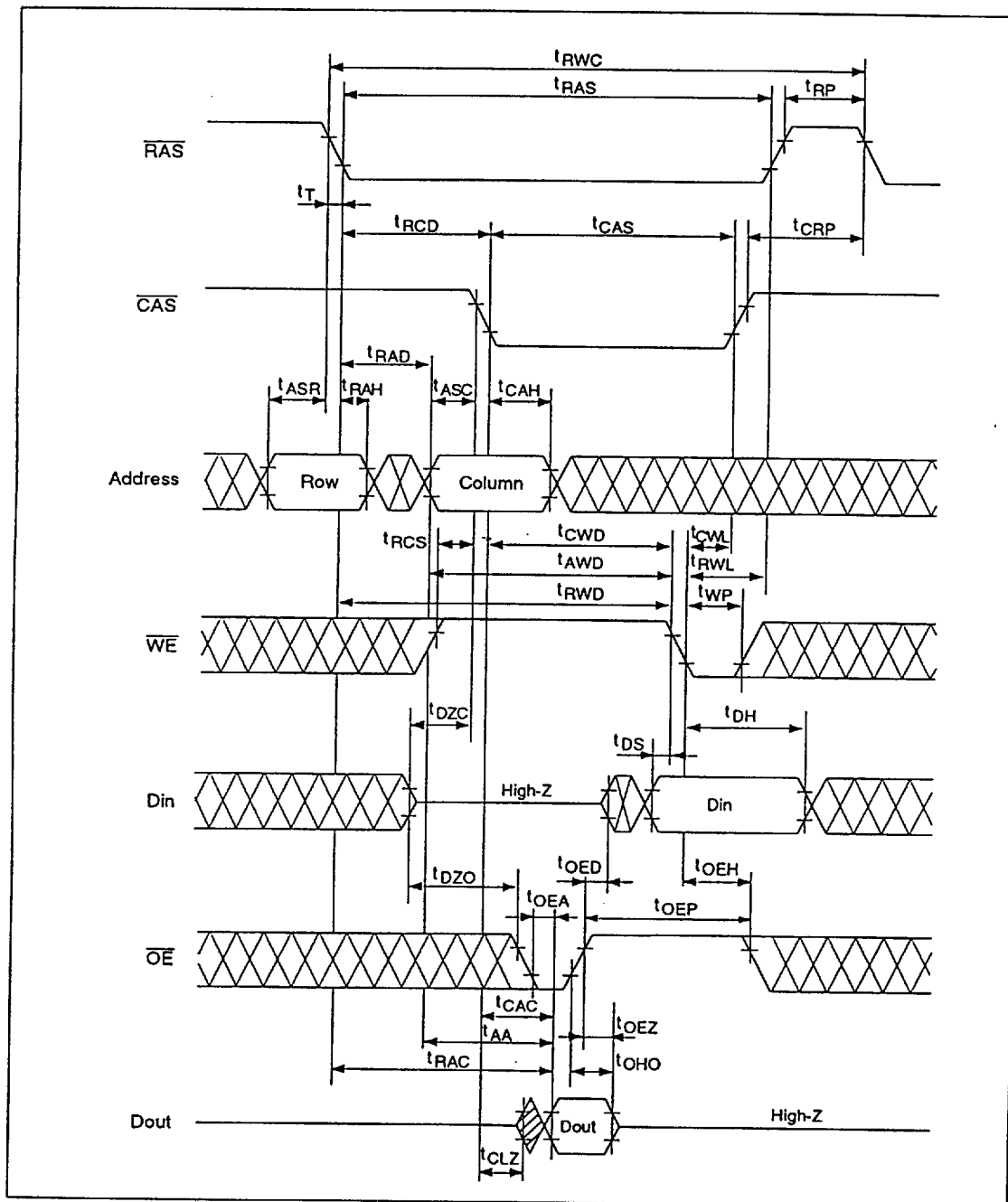
Delayed Write Cycle



HITACHI

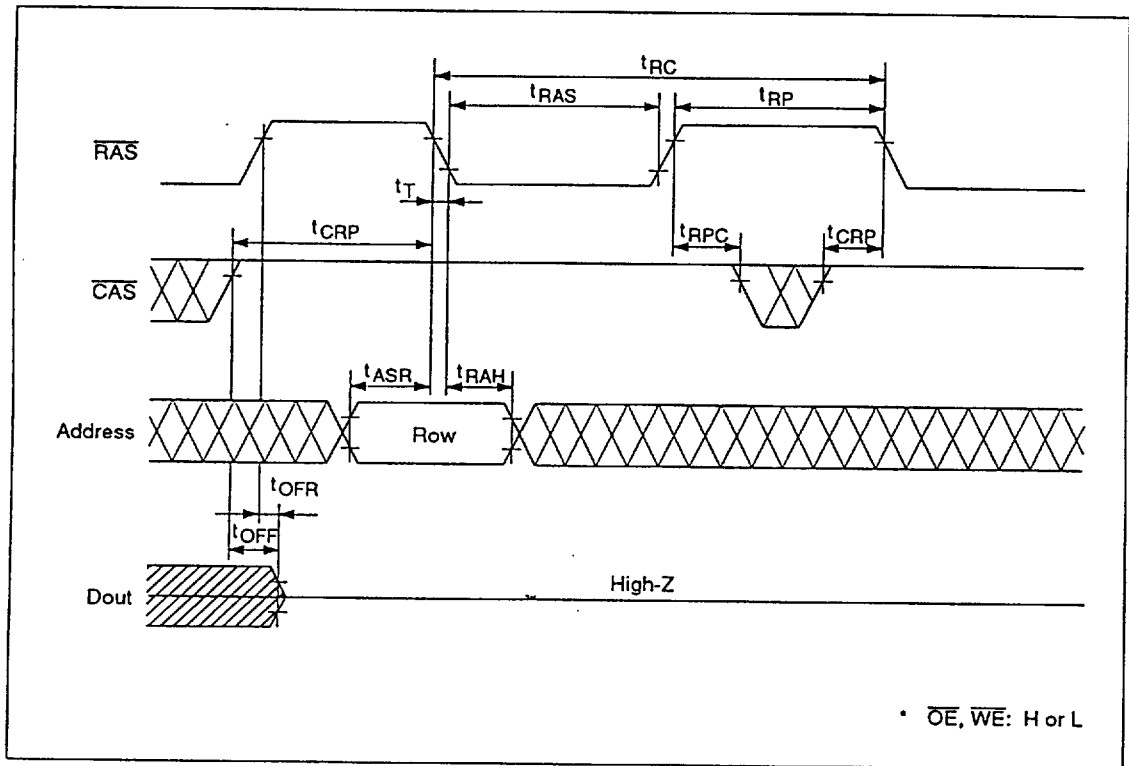
HM5164805A Series, HM5165805A Series

Read-Modify-Write Cycle



HITACHI

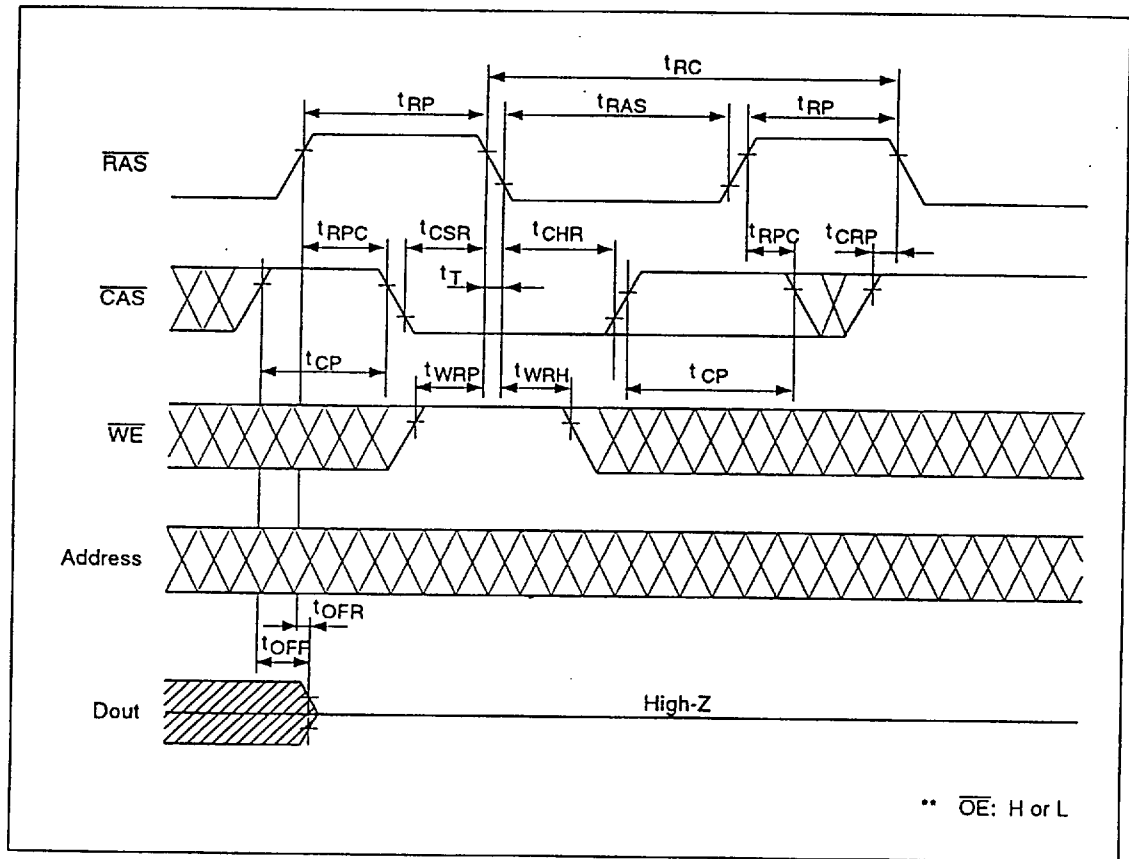
RAS Only Refresh Cycle



HITACHI

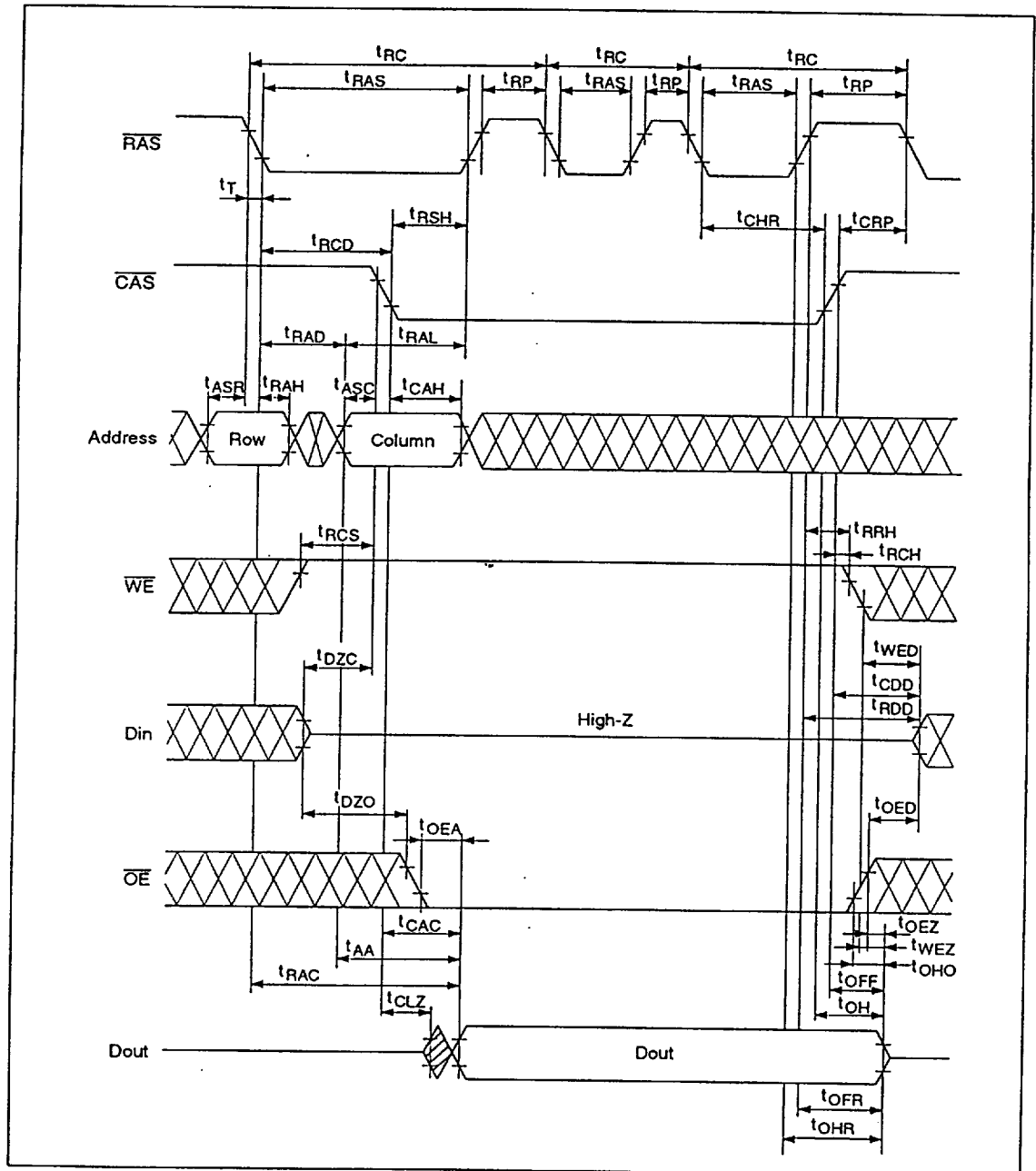
HM5164805A Series, HM5165805A Series

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



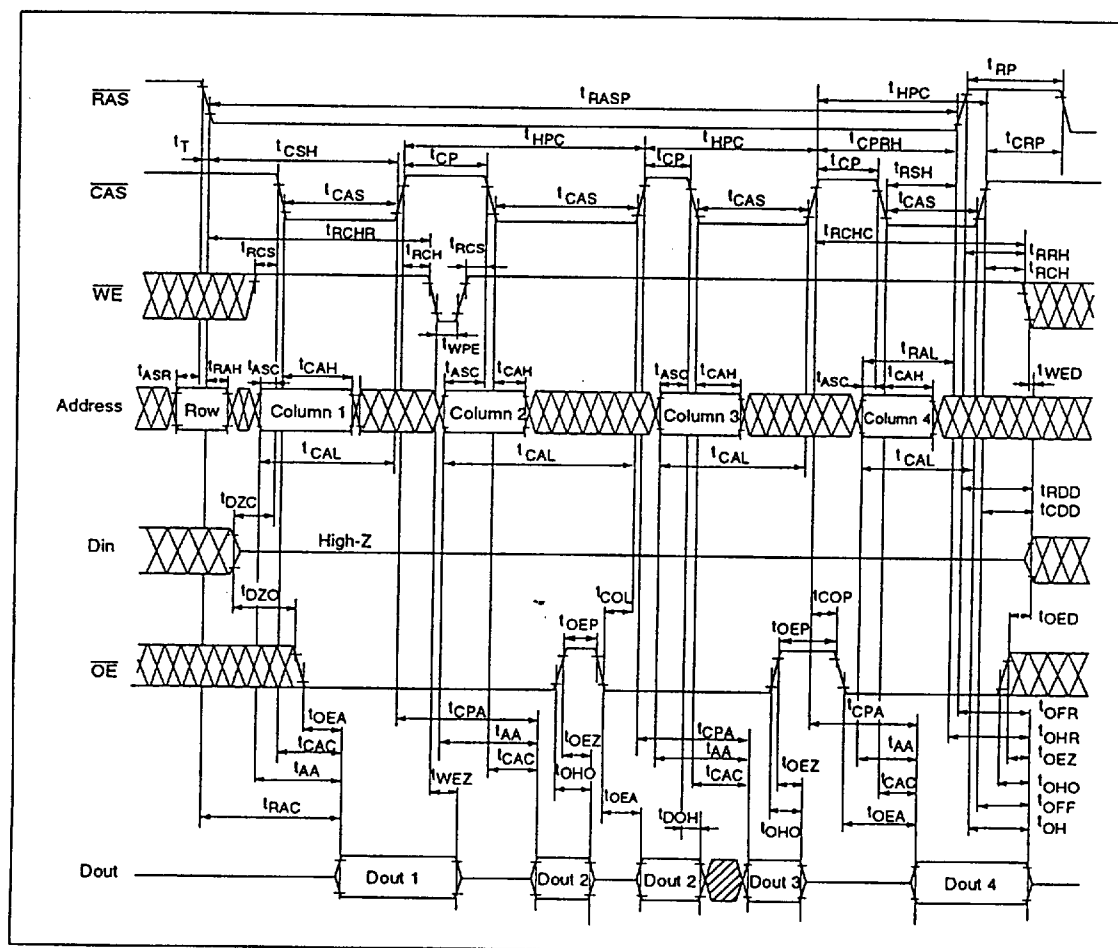
HITACHI

Hidden Refresh Cycle



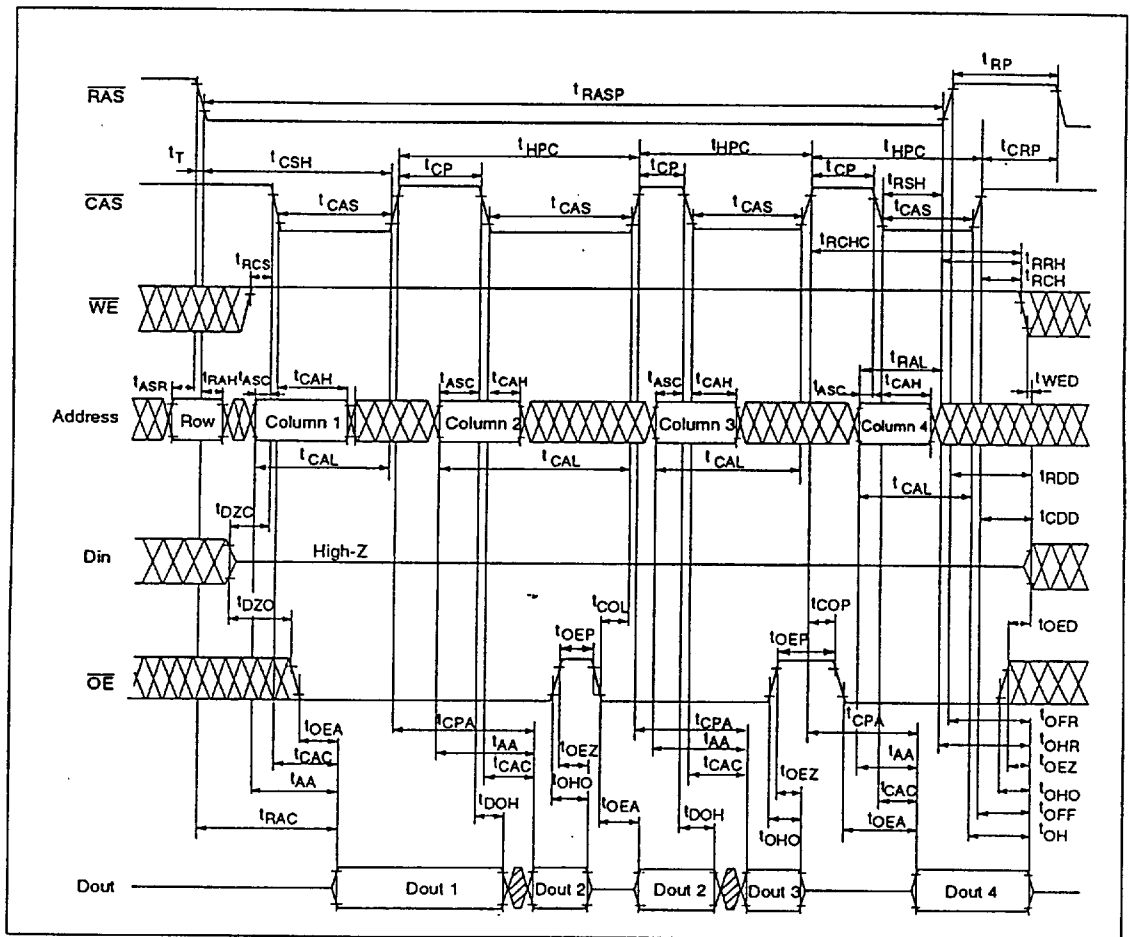
HITACHI

EDO Page Mode Read Cycle (1)



24

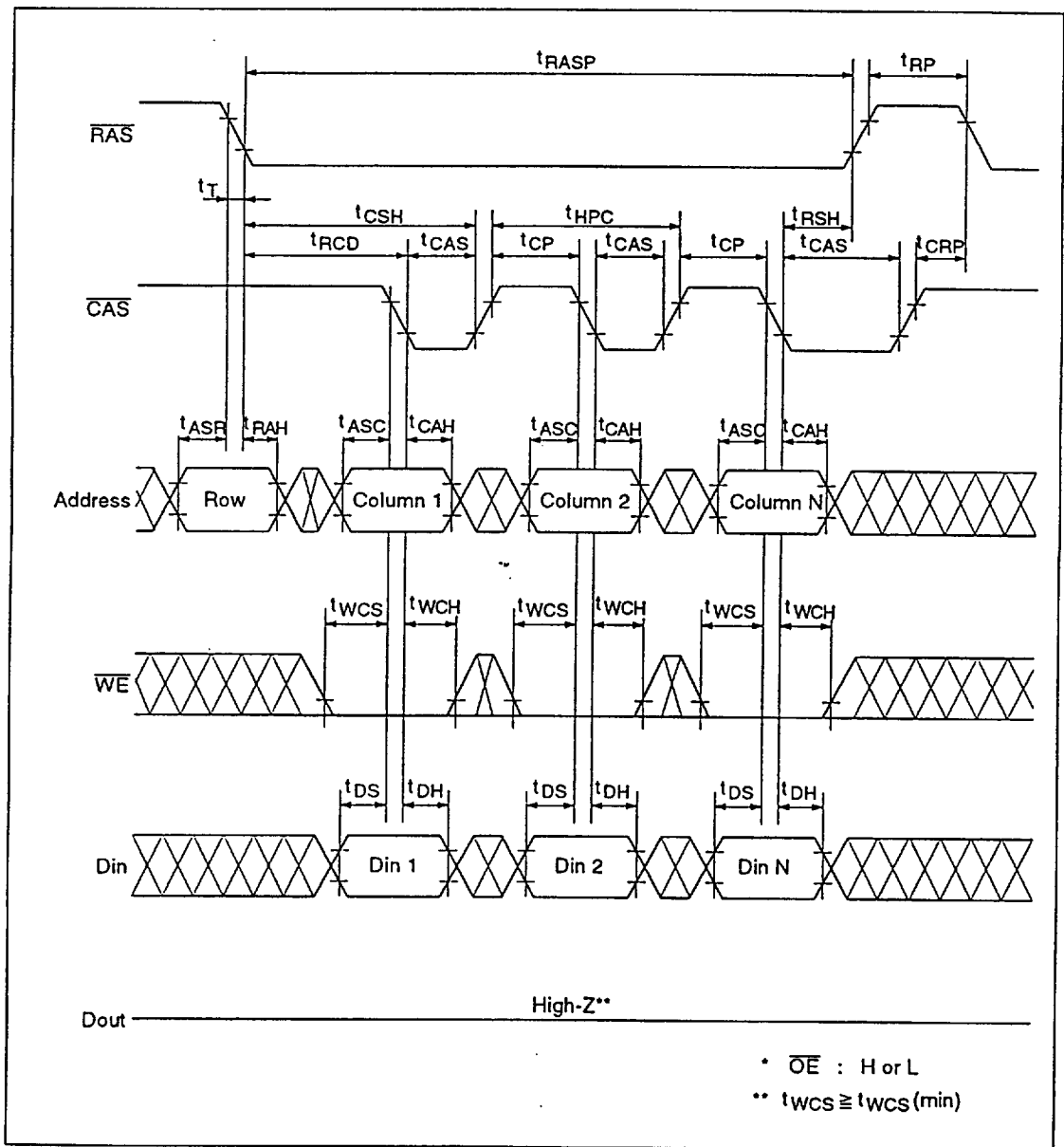
Powered by ICminer.com Electronic-Library Service Copyright 2003



25

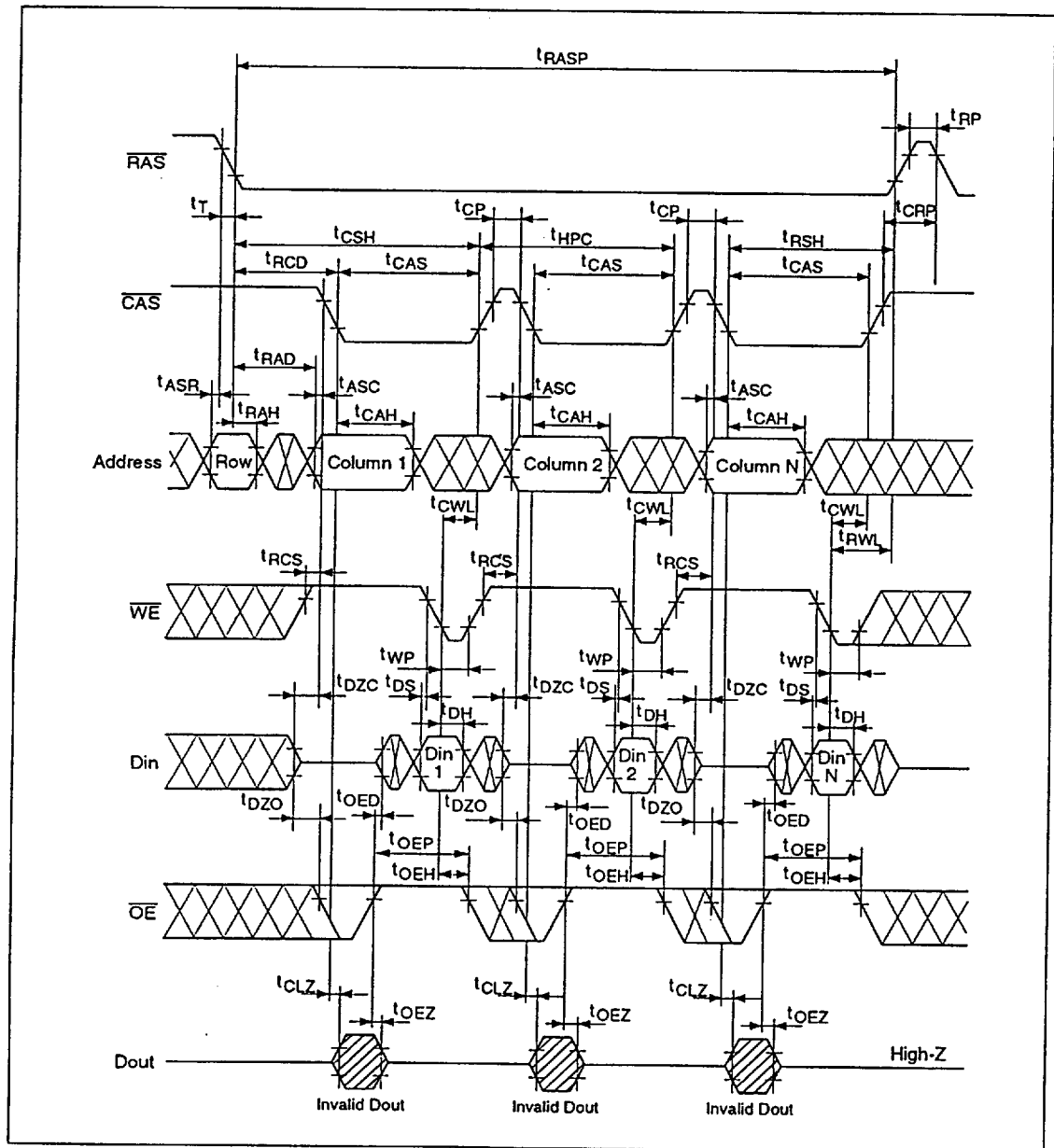
HM5164805A Series, HM5165805A Series

EDO Page Mode Early Write Cycle



HITACHI

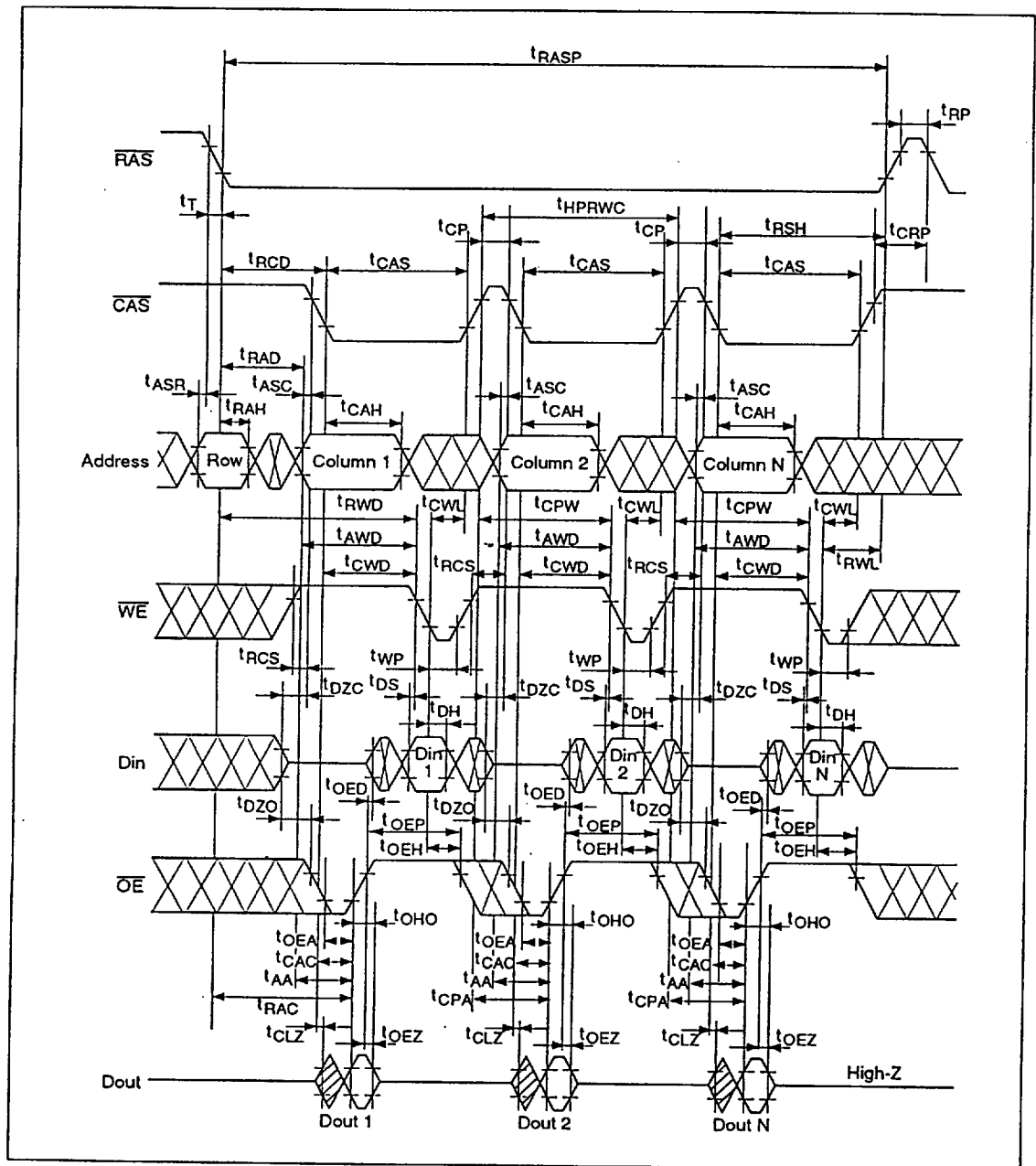
EDO Page Mode Delayed Write Cycle



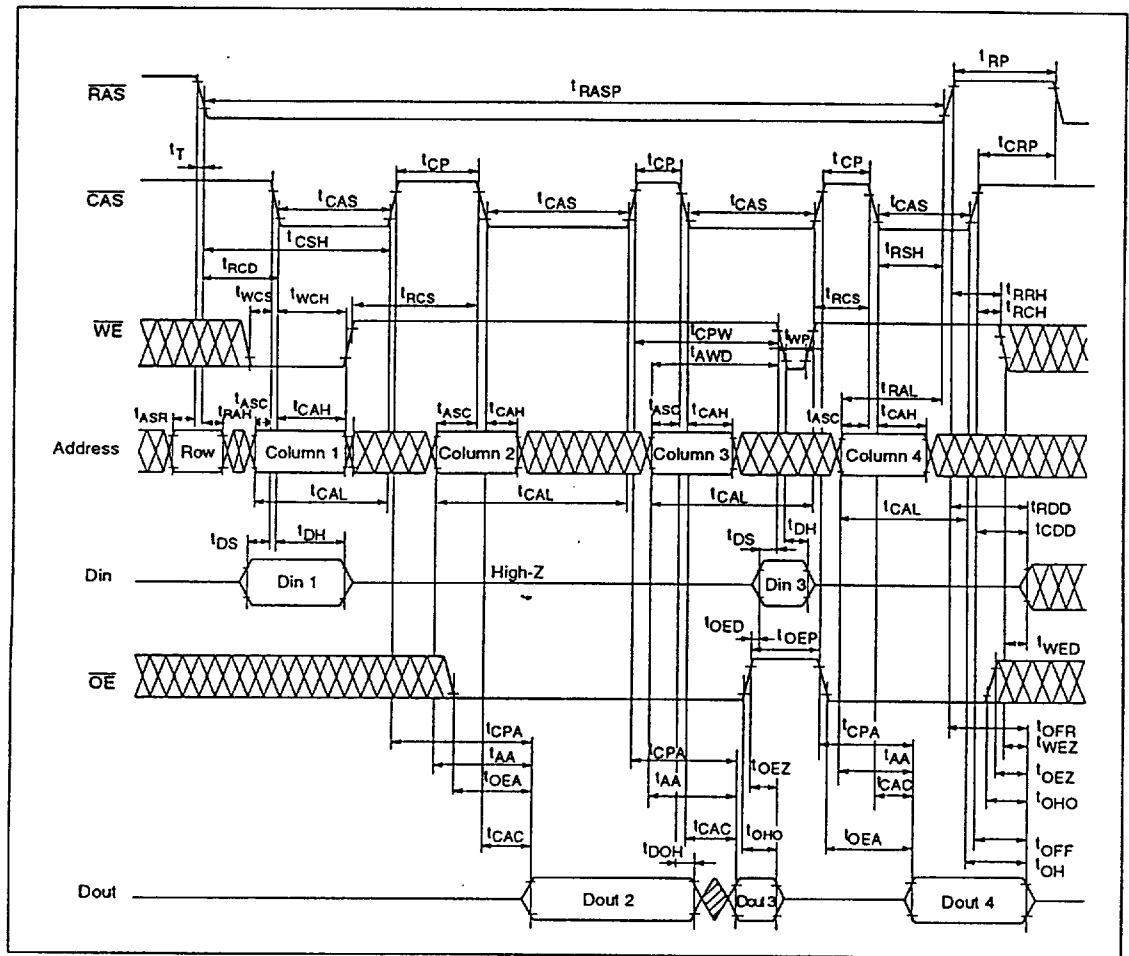
HITACHI

HM5164805A Series, HM5165805A Series

EDO Page Mode Read-Modify-Write Cycle

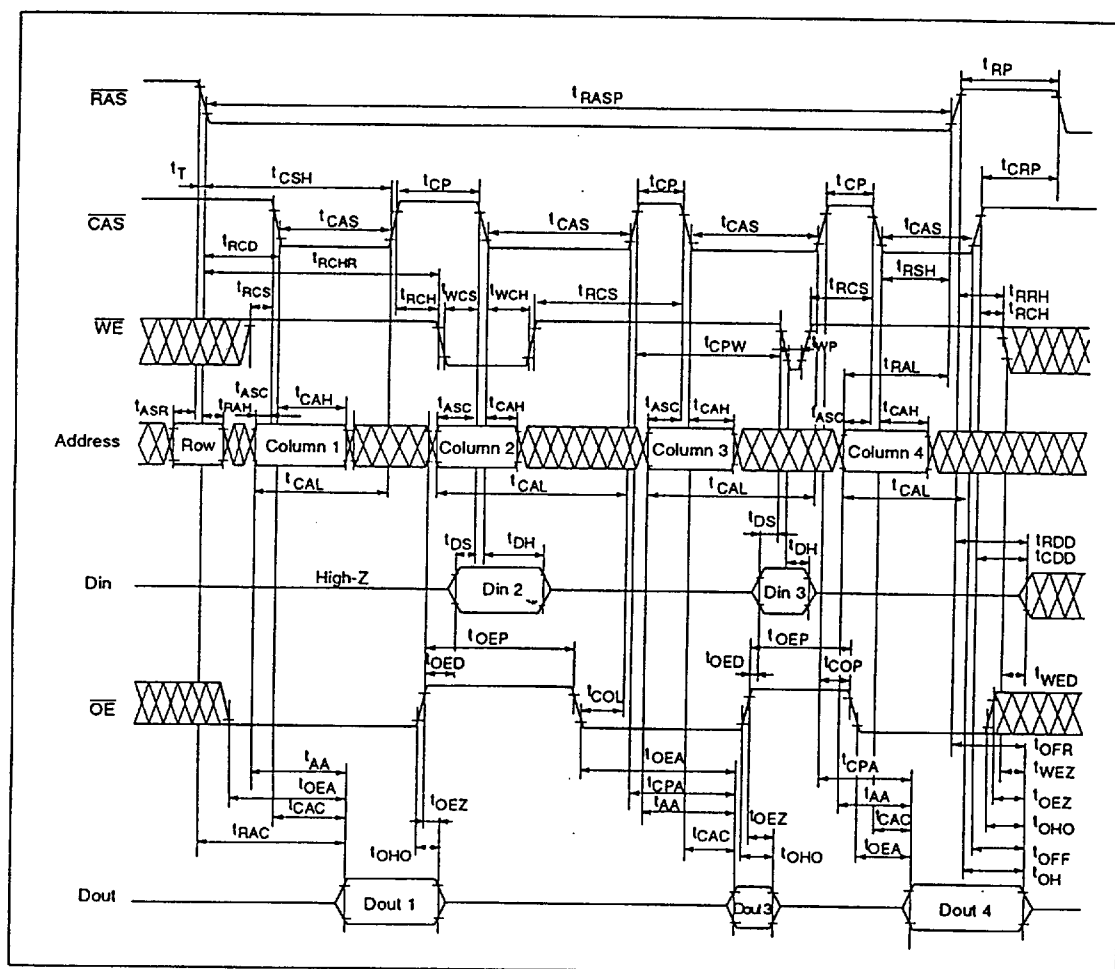


HITACHI



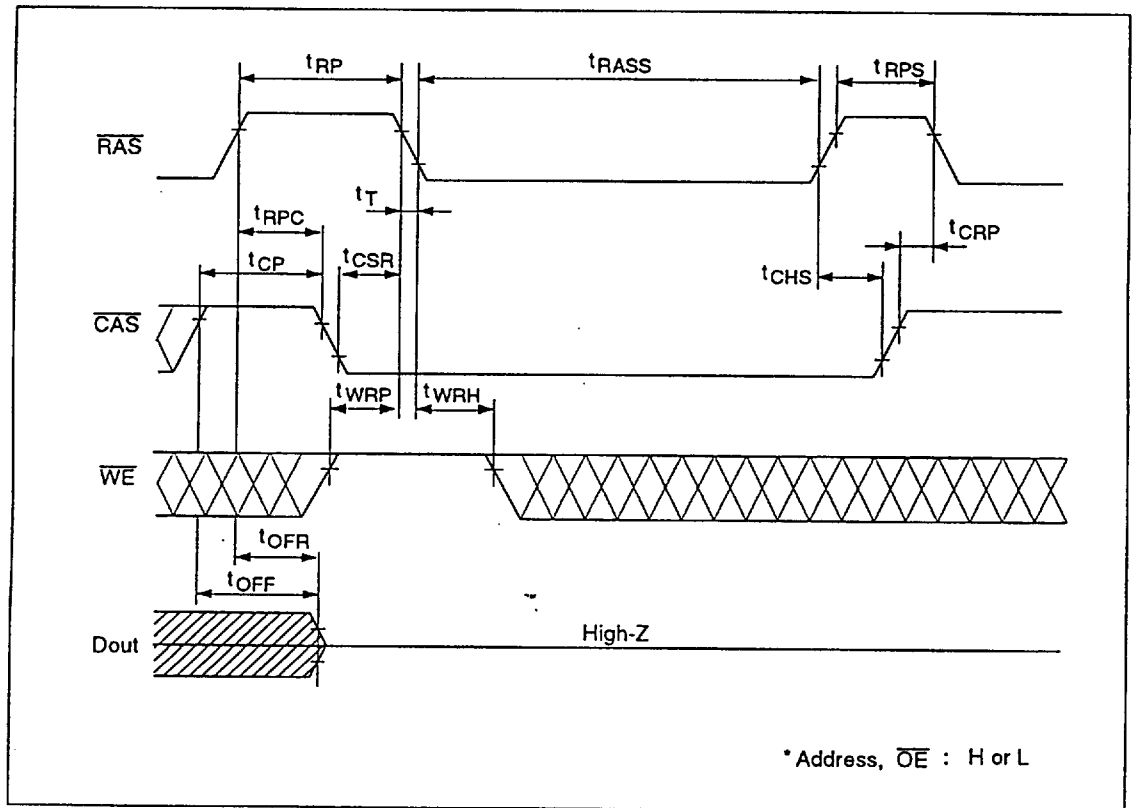
29

EDO Page Mode Mix Cycle (2)



HITACHI

Self Refresh Cycle (L-version)*21, 22, 23



HITACHI

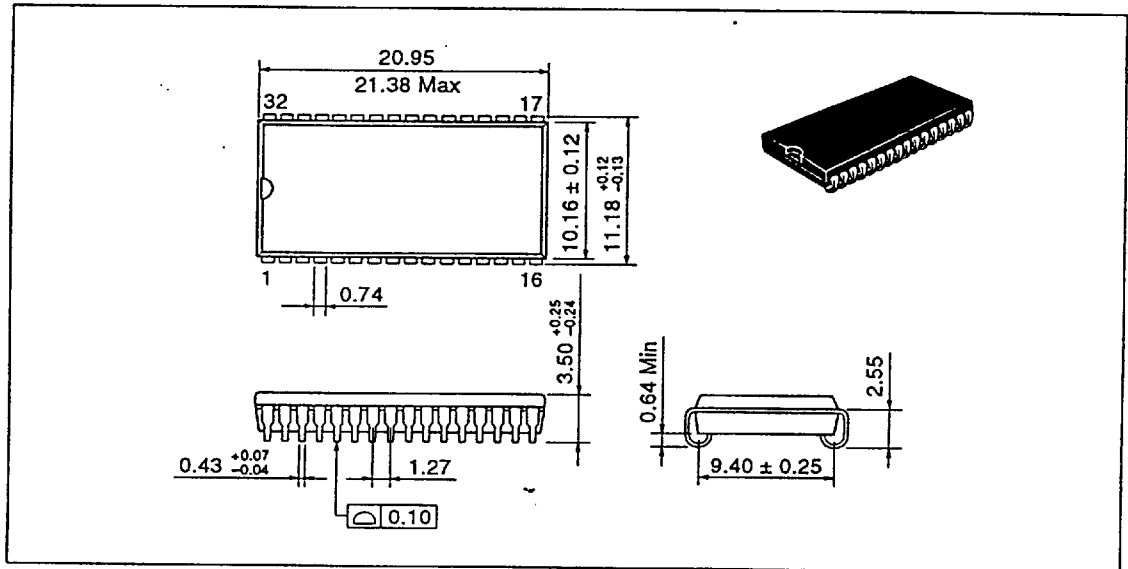
HM5164805A Series, HM5165805A Series

Package Dimensions

HM5164805AJ/ ALJ Series

HM5165805AJ/ ALJ Series (CP-32DC)

Unit: mm



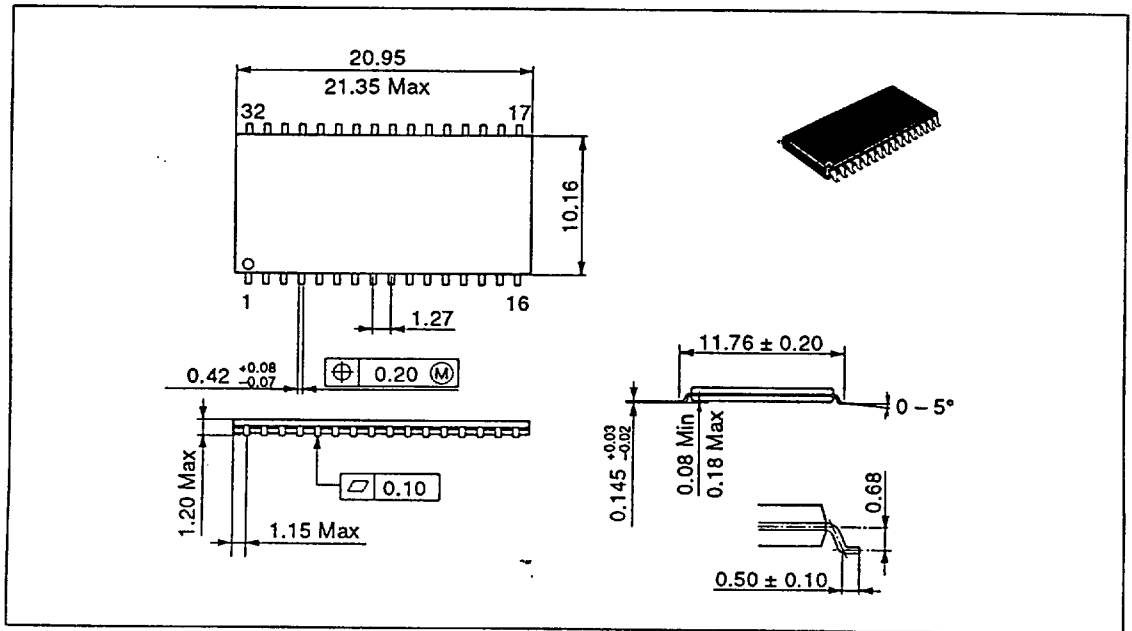
HITACHI

HM5164805A Series, HM5165805A Series

HM5164805ATT/ALTT Series

HM5165805ATT/ALTT Series (TTP-32DC)

Unit: mm



HITACHI