HT7620
PIR Controller With Dimmer

Features

- Dimmer function
- Dimmer status memory
- Linear or 3-step dimmer control
- Adjustable output duration
- CDS input
- 40 second warm-up
- ON/AUTO/OFF 3 mode operation
- Auto-reset when no ZC signal for over 3 s
- Built-in regulator
- Operating voltage: 5V~12V
- 16 pin DIP/SOP package

Applications

- PIR automatic light controller

General Description

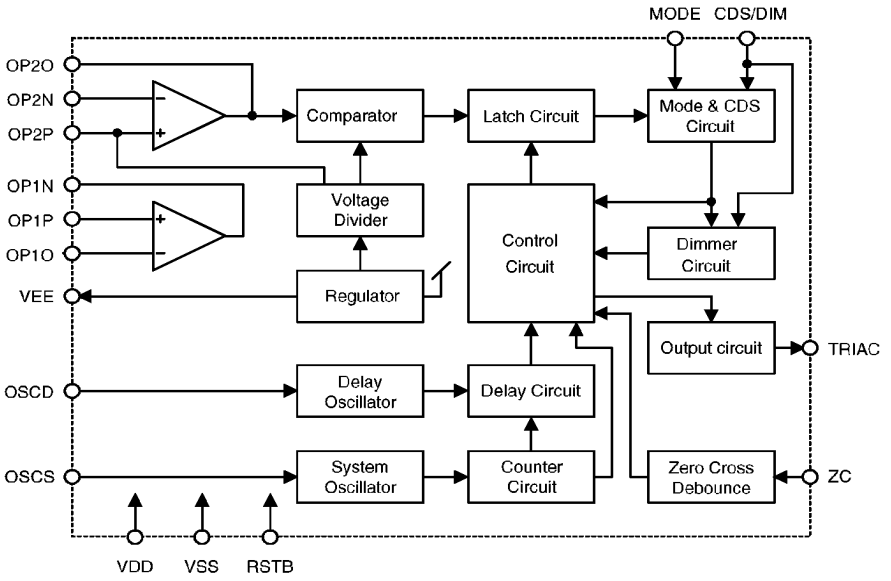
The HT7620 is a CMOS LSI designed for automatic PIR lamp control with dimmer control function. By controlling the conduction angle of a triac, the lamp brightness can be controlled according to the PIR's trigger signal and the dimmer status. For easy-installation, it is designed to work under a AC 2 wire power supply configuration.

The chip provides three operating modes (ON, AUTO, OFF) selectable with the MODE pin. When the lamp is turned on, the brightness can be adjusted by triggering the DIMMER key. The dimmer steps can be selected to be linear or 3-step.

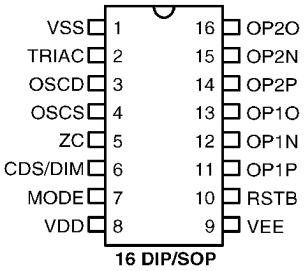
The chip also equiped with 2 operational amplifiers, zero crossing and CDS input circuitry. It is therefore suitable for products designed for direct mounting in a limited wall switch box space.

The IC is enclosed in a 16 pin DIP or SOP.

Block Diagram



Pin Assignment



HT7620A (60Hz,3-Step Dimmer) **HT7620C** (50Hz,3-Step Dimmer)
HT7620B (60Hz,Linear Dimmer) **HT7620D** (50Hz,Linear Dimmer)

Pin Description

Pin No.	Pin Name	I/O	Internal Connect	Description
1	VSS	I	—	Negative power supply.
2	TRIAC	O	CMOS	Output pin to drive triac. Normally high. Pulse output when active.
3	OSCD	I/O	PMOS IN NMOS OUT	Output timing oscillator I/O pin. Connect to external RC to adjust output active duration when triggered.
4	OSCS	I/O	PMOS IN NMOS OUT	System oscillator I/O pin. Connect to external RC to generate system frequency. The system frequency≅ 16KHz for normal application.
5	ZC	I	CMOS	Input pin for zero cross detecting. 60Hz : HT7620A, HT7620B 50Hz : HT7620C, HT7620D
6	CDS/DIM	I	CMOS	Dual-function input pin. With this pin connected to the external CDS voltage divider, the PIR trigger function will be disabled during daytime. When the lamp is on the dimmer function is performed by triggering a button switch connected between CDS/DIM and VSS. A linear or 3-step dimmer can be slected. Linear dimmer : HT7620B, HT7620D 3-Step dimmer : HT7620A, HT7620C
7	MODE	I	CMOS	Operating mode selection input. V_{DD} : output always ON—output pulse to drive TRIAC. V_{SS} : output always OFF—stays high. Open : Auto detecting.
8	VDD	I	—	Positive power supply.
9	VEE	O	NMOS	Regulated voltage output pin. The output voltage is about -3.9V with respect to VDD.
10	RSTB	I	Pull-High	Chip reset input pin. Active low.
11	OP1P	I	PMOS	Noninverting input of OP1.
12	OP1N	I	PMOS	Inverting input of OP1.

Pin No.	Pin Name	I/O	Internal Connect	Description
13	OP1O	O	NMOS	Output of OP1.
14	OP2P	I	PMOS	Noninverting input of OP2. Internally biased to the comparator window center voltage.
15	OP2N	I	PMOS	Inverting input of OP2.
16	OP2O	O	NMOS	Output of OP2. Internally connected to the comparator input.

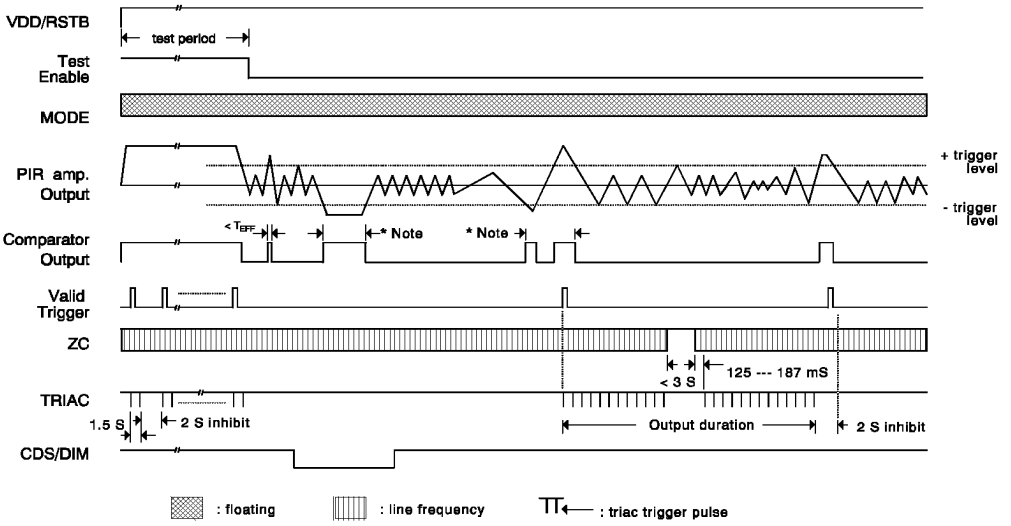
Absolute Maximum Ratings

Supply Voltage .....–0.3V to 13V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature.....–50°C to 125°C
Operating Temperature ..... –25°C to 75°C
Zero Crossing Current ..... max. 300μA

Electrical Characteristics

Symbol	Parametar	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	5	9	12	V
V_{EE}	Regulator Output Voltage	12V	V_{DD}–V_{EE}	3.4	3.9	4.4	V
I_{DD}	Operating Current	12V	No Load, OSC On.	—	450	800	μA
V_{IH1}	CDS "H" Transfer Voltage	12V	—	7.4	8.9	10.6	V
V_{IL1}	CDS "L" Transfer Voltage	12V	—	4.4	5.3	6.4	V
I_{OH1}	TRIAC Source Current	12V	V_{OH}=10.8V	–6	–12	—	mA
I_{OL1}	TRIAC Sink Current	12V	V_{OL}=1.2V	40	80	—	mA
I_{OL2}	VEE Sink Current	12V	V_{DD}–V_{EE}=3.9V	—	1	—	mA
V_{IH2}	MODE "H" Input Voltage	—	—	0.8V_{DD}	—	—	V
V_{IL2}	MODE "L" Input Voltage	—	—	—	—	0.2V_{DD}	V
V_{IH3}	ZC "H" Transfer Voltage	12V	—	4.7	6.7	8.7	V
V_{IL3}	ZC "L" Transfer Voltage	12V	—	1.3	1.8	2.3	V
F_{SYS}	System Oscillator Frequency	12V	R_{OSCS}=430K C_{OSCS}=100P	12.8	16	19.2	KHz
F_d	Delay Oscillator Frequency	12V	R_{OSCD}=430K C_{OSCD}=100P	12.8	16	19.2	KHz
A_{VO}	OP Amp Open Loop Gain	12V	No load	60	80	—	dB
V_{OS}	OP Amp Input Offset Voltage	12V	No load	—	10	35	mV
V_{IL4}	DIM Trigger Input Voltage	12V	—	V_{SS}-0.3	0.1	0.5	V

Trigger Timing



Note:

- The output will be activated if the trigger signal meets the following criteria:
  - 2 effective trigger signals within 2s with one trigger signal sustained ≥ 0.16s.
  - A trigger signal with a sustained duration ≥ 0.34s.
  - More then 3 triggers within 2 seconds.
- The effective comparator output trigger width can be selected to be 24ms or 32ms or 48ms by mask option. The default is 24ms (system frequency = 16KHz).
- The output duration is set by external RC network connected to the OSCD pin.

Functional Description

VEE

Supplies power to the analog front end circuits with a stablized voltage which is –3.9V with respect to VDD normally.

OSCS

System oscillator input pin, connect to external RC network to generate a 16KHz system frequency.

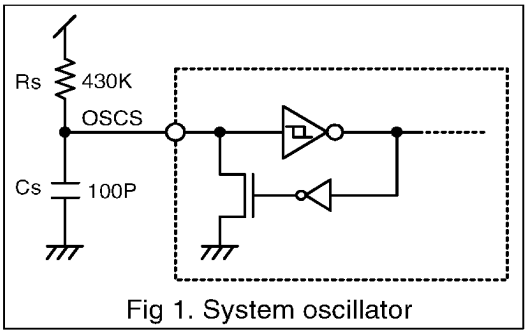


Fig 1. System oscillator

OSCD

Timing oscillator input pin. Connect to external RC network to obtain the desired output turn-on duration. Variable output turn-on duration can be obtained by selecting various values of RC or using a variable resistor.

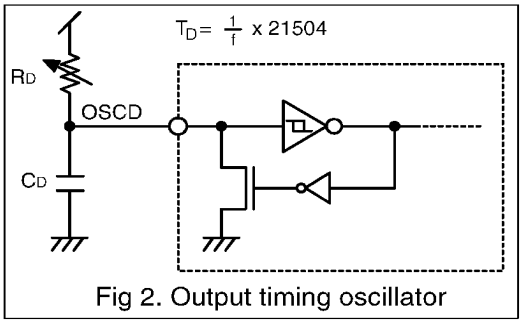


Fig 2. Output timing oscillator

TRIAC

Output pin for driving a triac to turn on the lamp. High output when the chip is in stand-by in AUTO mode (MODE=Open) or when the chip is in OFF mode (MODE=VSS).

Activated when:

- The chip is in ON mode (MODE=VDD).
- Triggered by PIR signal in AUTO mode (MODE=Open).
- Triggered by PIR signal during test operating (MODE=Open)
- Triggered by amplifier settling during warm-up period (MODE=Open).

The output waveform is a pulse train whose period is synchronized by line frequency and whose conducting angle is controlled by the dimmer status.

CDS/DIM

CMOS schmitt trigger input structure. Used to receive dimmer control input as well as to distinguish between day time & night.

- CDS

When CDS is low the PIR will be disabled. The input disable to enable debounce time is 5 seconds. Connect this pin to VDD when not using this function. The CDS input is ignored when output is active.

CDS	status	PIR Input
LOW	Day Time	Disable
HIGH	Night	Enable

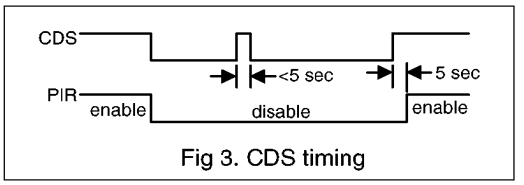


Fig 3. CDS timing

- Dimmer

When the lamp is on, the brightness can be controlled by a low trigger signal (< 0.5V) to this pin. The dimmer step can be selected to be linear or 3-steps (high–medium–low).

The dimmer adjusting input is inhibited when the lamp is off.

Selection Table

Part No.	Dimmer	Line Frequency
HT7620A	3-Step	60 Hz
HT7620B	Linear	60Hz
HT7620C	3-Step	50Hz
HT7620D	Linear	50Hz

Consult the diagram below for application of CDS/DIM pin.

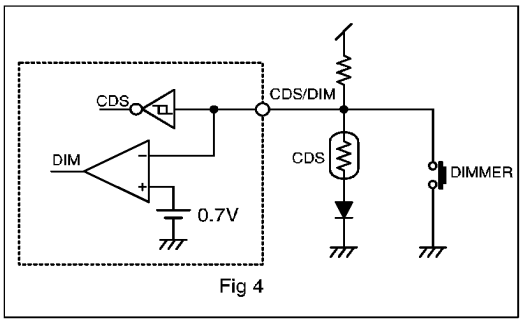


Fig 4

- 3-Step Dimmer

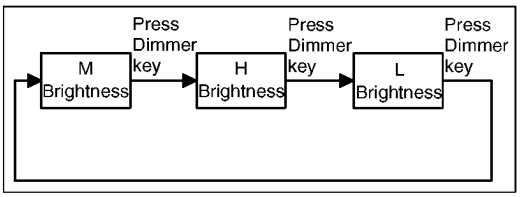
HT7620A and HT7620C have 3-step dimmer functions. When the lamp is on pressing the DIMMER key will change the dimmer step cyclically.

L: minimum brightness. TRIAC trigger angle=121.4°

M: medium brightness. TRIAC trigger angle=89°

H: maximum brightness. TRIAC trigger angle=24.2°

The default is medium brightness (M) after power-on.



- Linear Dimmer

The HT7620B and HT7620D have linear dimmer functions. When the lamp is on pressing DIMMER key will change the dimmer step linearly.

If the key is pressed and held the brightness will linearly change from low to maximum and then from maximum to minimum cyclically. When the key is released it will remain at that level until the next time the key is pressed. The default brighness at power-on is 1/2 maximum brightness.

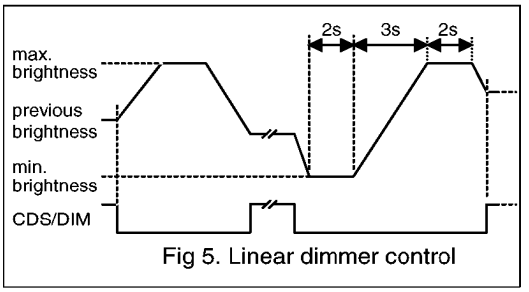


Fig 5. Linear dimmer control

Minimum brightness: TRIAC trigger angle=159.6°

Maximum brightness: TRIAC trigger angle=24.2°

Default brightness after power on: TRIAC trigger angle=89°

MODE

This is a tri-state input pin for operating mode selection.

MODE Status	Operating Mode	Description
VDD	ON	Output always ON: TRIAC pin outputs a pulse train synchronized by ZC.
VSS	OFF	Output always OFF: TRIAC pin output high.
Open	AUTO	Output remains off. Will be activated by a valid PIR input trigger signal.

RSTB

Used to reset the chip. Internal pull-high, active low.

Fig 6. shows an RSTB application example. Using C_{RST} can extend the power-on initial time. If the RSTB pin is open circuit (without C_{RST}), the initial time is equal to the default (40s).

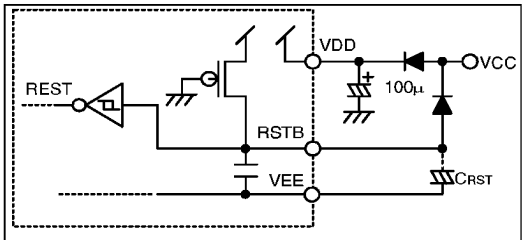


Fig 6. RSTB application example

If the ZC signal disappears for more than 3 seconds, it will restart the initial operation. The restared initial time is always 40 seconds and cannot be extended by adding C_{RST} to the RSTB pin as shown in Fig 6.

ZC

CMOS input structure. Receives AC line frequency and generates zero crossing pulses to synchronize the triac driver.

MASK OPTIONS

- Option for effective PIR trigger pulse width: >24ms, >32ms or >48ms. The default is >24ms.
- Option for setting comparator window to be $\frac{1}{16}$ $\frac{1}{11.3}$ or $\frac{1}{9}$ (VDD–VEE).The default is $\frac{1}{16}$ (VDD–VEE).
- Option for test mode entrance.
  - Fixed 60 second test enable time after power-on or reset.
  - Automatically enter test mode after power-on or reset and go to AUTO mode only when there is no PIR trigger signal for a time interval of more than 32 seconds.

The default is 60 second testing time after power-on or reset.

TEST MODE

The chip provides 2 kinds of test modes selected by mask option.

- Fixed 60 second testing time after power-on or reset and then enter AUTO mode automatically if MODE=Open.
- Enter test mode after power-on or reset and go to AUTO MODE (if MODE=open) only when there is no valid PIR trigger signal for

During test mode the output is nontriggerable and will be turned-on for 1.5 second each time it is triggered by a valid PIR trigger signal.

The inhibit time for next trigger is 2 second. The default is fixed 60 second testing time after power-on.

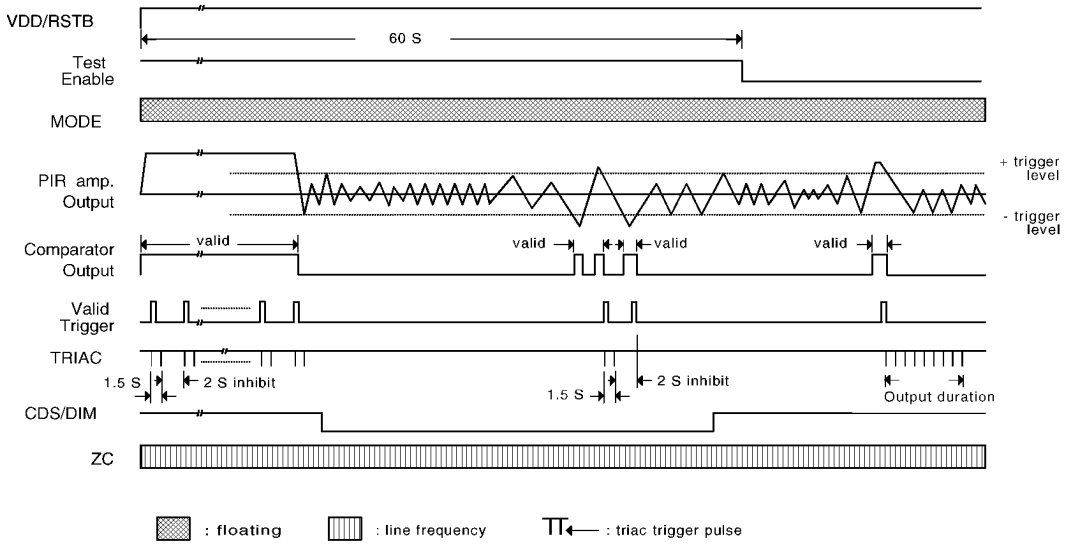


Fig. 7 60 second fixed test mode

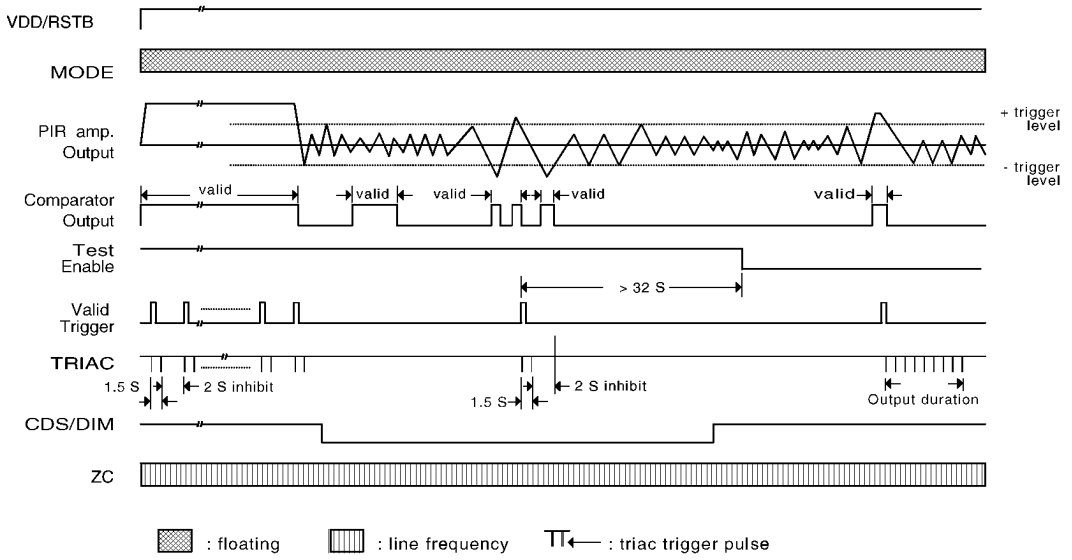


Fig. 8 Auto-test mode

PIR Amplifier

Consult the diagram below for details of the PIR front end amplifier.

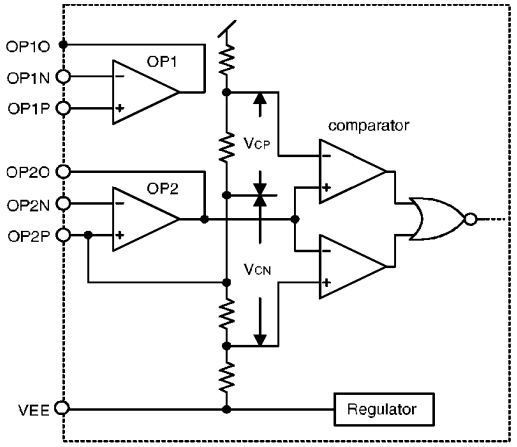


Fig 9. PIR amplifier block diagram

In Fig 9. there are 2 op-amps with different applications. OP1 can be used independently as a first stage inverting or non-inverting amplifier for the PIR.

As the output of OP2 is directly connected to the input of the comparator it is therefore used as a second stage amplifying device.

The non-inverting input of OP2 is connected to the comparator's window centerpoint and can be used to check this voltage and to provide a bias voltage that is equal to the centerpoint voltage of the comparator.
In Fig 9. the comparator can have 3 window levels, set by mask options.

1. $\frac{1}{16}$ (VDD–VEE)

2. $\frac{1}{11.3}$ (VDD–VEE)

3. $\frac{1}{9}$ (VDD–VEE)

If not specified the default window will be set to $\frac{1}{16}$ (VDD–VEE). The preset voltage for VDD–VEE is 3.9V. The V_{CP} and V_{CN} default value is therefore 0.24V, ($\frac{3.9}{16}$V).

Second Stage Amplifier

Usually, the second stage PIR amplifier is a simple capacitively coupled inverting amplifier with low pass configuration. The noninverting input terminal is biased to the center point of the comparator window and the output of the second stage amplifier is directly coupled to the comparator center point.

In Fig 10. OP2P is directly connected to the comparator window center, and with the C3 filter can act as the bias for OP2. For this configuration, $A_V=\frac{R2}{R1}$, low cutoff frequency $f_L=\frac{1}{2\pi R1C1}$, high cutoff frequency $f_H=\frac{1}{2\pi R2C2}$. By changing the value of R2 the sensitivity can be varied. C1 and C3, must be low leakage types, to prevent the DC operating point from changing due to current leakage.

Each op-amp current consumption is approx. 5μA with all of the op-amps and comparator's working voltage provided by the regulator.

Consult the following diagrams for typical PIR front end circuits.

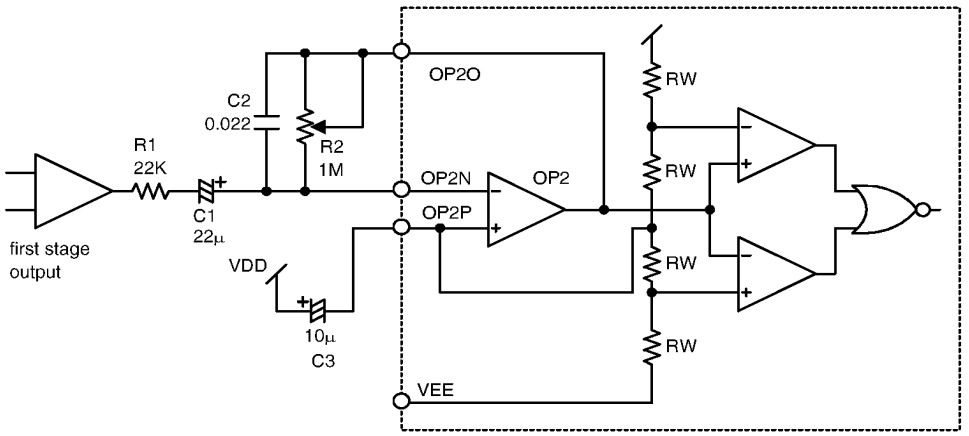


Fig 10. Typical second stage amplifier

First Stage of PIR Amplifier

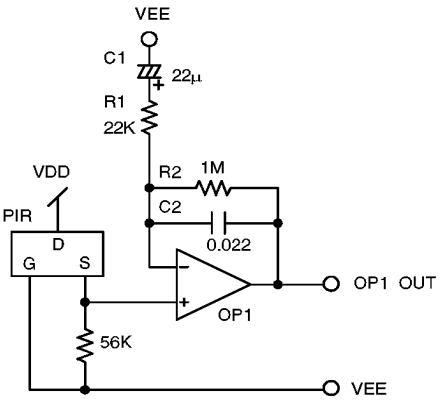


Fig 11. Typical PIR amplifier

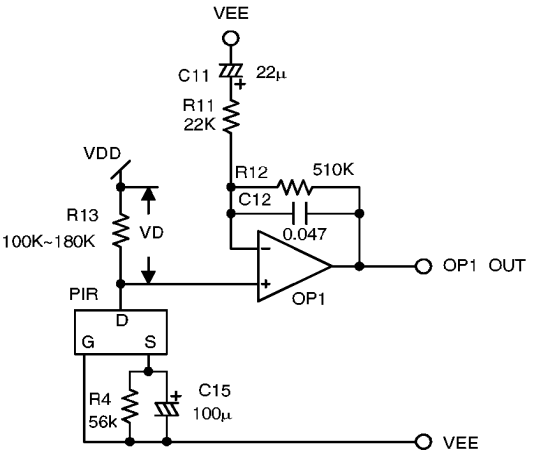


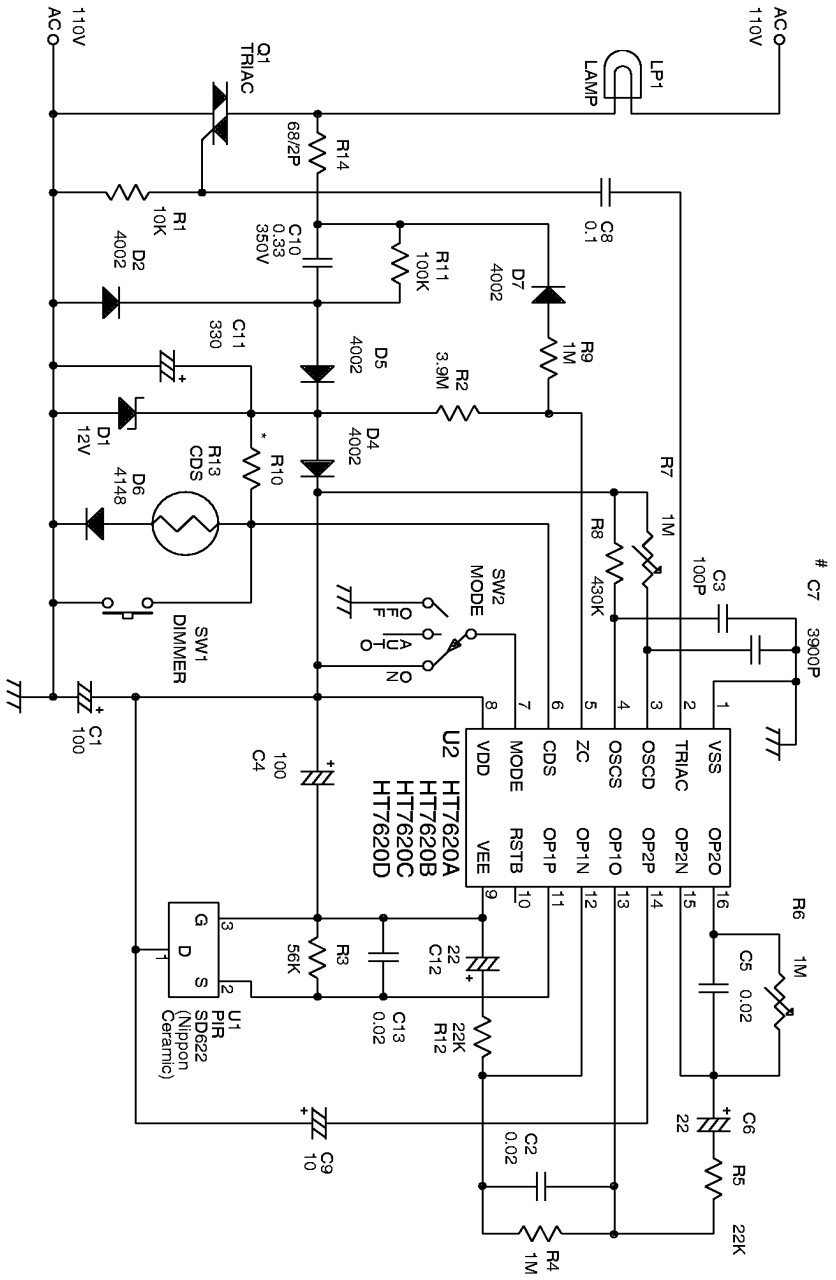
Fig 12. High gain first stage

Fig 11. shows a typical first stage amplifier. C2 and R2 form a simple low pass filter with cut off frequency at 7Hz. The low frequency response is governed by R1 and C1 with cut-off frequency at 0.33Hz.

$$A_V=\frac{(R1+R2)}{R1}$$

Fig 11. and 12. are similar but in Fig 12. the amplifier's input signal is taken from the drain of the PIR. This has higher gain than Fig 11. since OP1 is PMOS input V_D must be greater than 1.2V for adequate operation.

Application Circuit



Note: 1. Adjust R10 to fit various CDS.
2. Change C7 to obtain the desired adjusting range of output duration.
3. For 220V AC application change the value of C10 to 0.15μF/600V