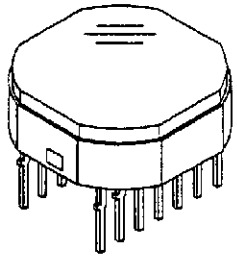
SONY

ICX059ALB

Diagonal 6mm (Type 1/3) CCD Image Sensor for CCIR B/W Camera

14 pin DIP (Ceramic)



Description

The ICX059ALB is an interline transfer CCD solid-state image sensor suitable for CCIR B/W video cameras. High sensitiveness and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

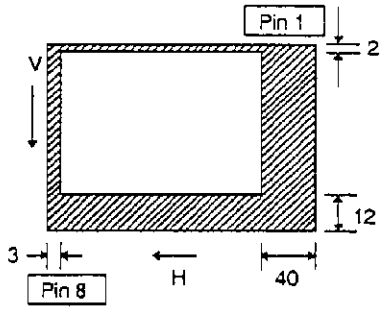
This chip features a field integration read out system and an electronic shutter with variable charge-storage time. Also, this outline is miniaturized by using original package.

Features

- High image, high sensitivity and low dark current
- Consecutive various speed shutter
  1/50s (Typ.), 1/120s to 1/10000s
- Low smear
- High antiblooming
- Horizontal register 5V drive
- Reset gate 5V drive

Device Structure

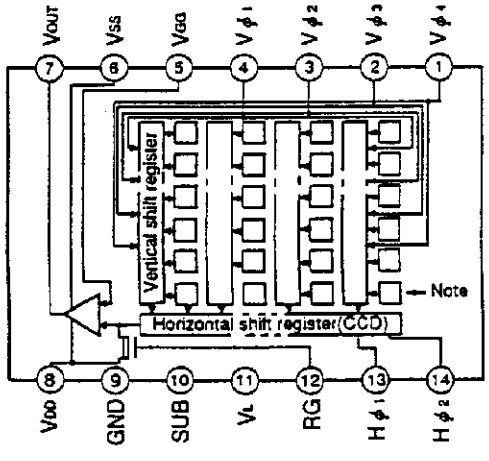
- Image size: Diagonal 6mm (Type 1/3)
- Number of effective pixels: 752 (H)×582 (V) Approx. 440k pixels
- Number of total pixels: 795 (H)×596 (V) Approx. 470k pixels
- Interline transfer CCD image sensor
- Chip size: 6.00mm (H)×4.96mm (V)
- Until cell size: 6.5 μm (H)×6.25 μm (V)
- Optical black: Horizontal (H) direction: Front 3 pixels Rear 40 pixels
  Vertical (V) direction: Front 12 pixels Rear 2 pixels
- Number of dummy bits: Horizontal: 22
  Vertical: 1 (even field only)
- Board material: N-type silicon

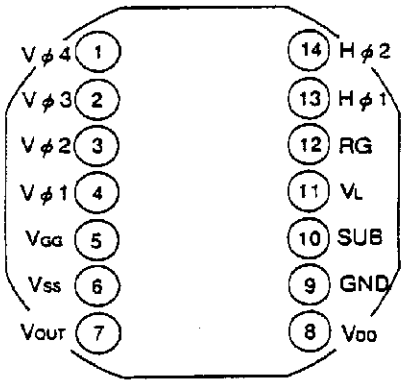


Optical black position (Top View)

E93584D9X

Block Diagram (Top View)





Note ← □ : Photo sensor

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	8	VDD	Output amplifier drain supply
2	Vφ3	Vertical register transfer clock	9	GND	GND
3	Vφ2	Vertical register transfer clock	10	SUB	Substrate (Overflow drain)
4	Vφ1	Vertical register transfer clock	11	VL	Protective transistor bias
5	VGG	Output amplifier gate bias	12	RG	Reset gate clock
6	VSS	Output amplifier source	13	Hφ1	Horizontal register transfer clock
7	VOUT	Signal output	14	Hφ2	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB−GND		−0.3 to +55	V	
Supply voltage	VDD, VOUT, VSS−GND	−0.3 to +18	V	
	VDD, VOUT, VSS −SUB	−55 to +10	V	
Vertical clock input voltage	Vφ1,Vφ2, Vφ3, Vφ4 − GND	−15 to +20	V	
	Vφ1,Vφ2, Vφ3, Vφ4 − SUB	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*
Voltage difference between horizontal clock input pins		to +17	V	
Hφ1,Hφ2 − Vφ4		−17 to +17	V	
Hφ1,Hφ2,RG,VGG − GND		−10 to +15	V	
Hφ1,Hφ2,RG,VGG − SUB		−55 to +10	V	
VL − SUB		−65 to +0.3	V	
Vφ1,Vφ2, Vφ3, Vφ4 , VDD, VOUT − VL		−0.3 to +30	V	
RG − VL		−0.3 to +24	V	
VGG, VSS, Hφ1, Hφ2 −VL		−0.3 to +20	V	
Storage temperature		−30 to +80	℃	
Operating temperature		−10 to +60	℃	

* +27V(Max.) when clock width < 10 μs, duty factor < 0.1%.

Bias Conditions

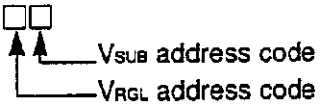
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier gate voltage	V_{GG}	3.8	4.2	4.65	V	
Output amplifier source	V_{SS}	Ground through 820 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*2
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*2 *6
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*3				

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		5		mA	
Input current	I_{IN1}			1	μA	*4
Input current	I_{IN2}			10	μA	*5

* 2 Substrate voltage (V_{SUB}) · reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ±3%.

V_{SUB} code address−1 digit display
V_{RGL} code address−1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL} = 3.0V
V_{SUB} = 12.0V

* 3 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

* 4 1. Current to each pin when 18V is applied to V_{OD}, V_{OUT}, V_{SS} and SUB pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to Vϕ1, Vϕ2, Vϕ3 and Vϕ4, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG, Hϕ1, Hϕ2 and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Apply 30V to Pins Vϕ1, Vϕ2, Vϕ3, Vϕ4, V_{OD}, V_{OUT}; 24V to Pin RG; and 20V to Pins V_{GG}, V_{SS}, Hϕ1, Hϕ2. The above is the current that flows to Pin V_L when it is grounded. Please note that Pins GND and SUB are to be disconnected.

* 5 Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

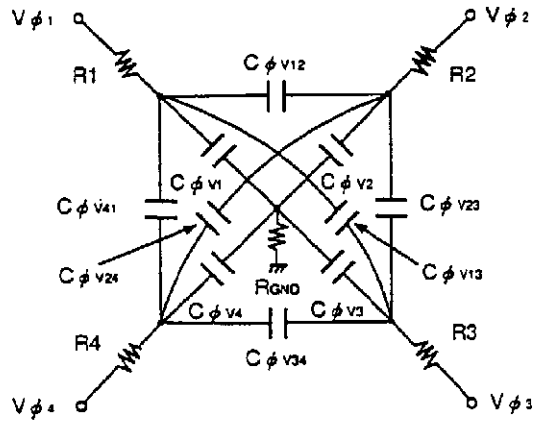
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	−0.05	0	0.05	V	2	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VH3}, V_{VH4}	−0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	−9.0	−8.5	−8.0	V	2	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	Vϕv	7.8	8.5	9.05	V	2	Vϕv=$V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1}, V_{VH2} \rvert$			0.1	V	2	
	$V_{VH3}-V_{VH}$	−0.25		0.1	V	2	
	$V_{VH4}-V_{VH}$	−0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	VϕH	4.75	5.0	5.25	V	3	
	V_{HL}	−0.05	0	0.05	V	3	
Reset gate clock voltage	VϕRG	4.5	5.0	5.5	V	4	*6
	$V_{RGLH}-V_{RGLL}$			0.8	V	4	Low level coupling
Substrate clock voltage	VϕSUB	22.5	23.5	24.5	V	5	

* 6 No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

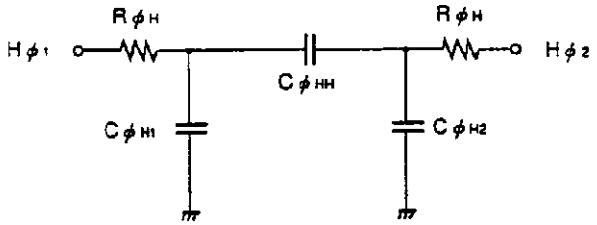
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	−0.2	0	0.2	V	4	
	VϕRG	8.5	9.0	9.5	V	4	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$		1000		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		560		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$		470		pF	
	$C\phi_{V23}$, $C\phi_{V41}$		390		pF	
	$C\phi_{V13}$		180		pF	
	$C\phi_{V24}$		100		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		47		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		51		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		8		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		270		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		80		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R\phi_H$		15		Ω	



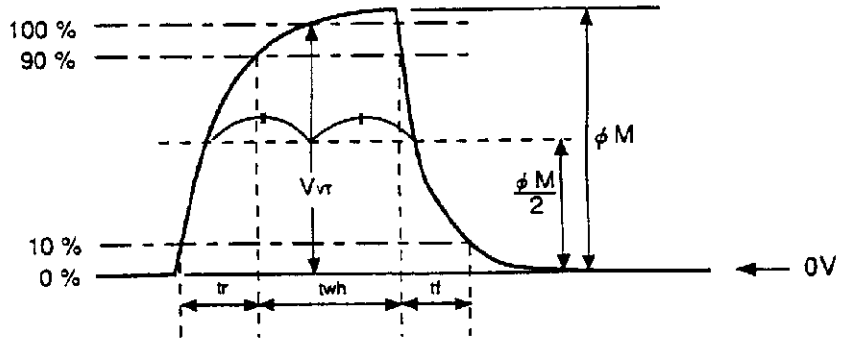
Vertical transfer clock equivalent circuit



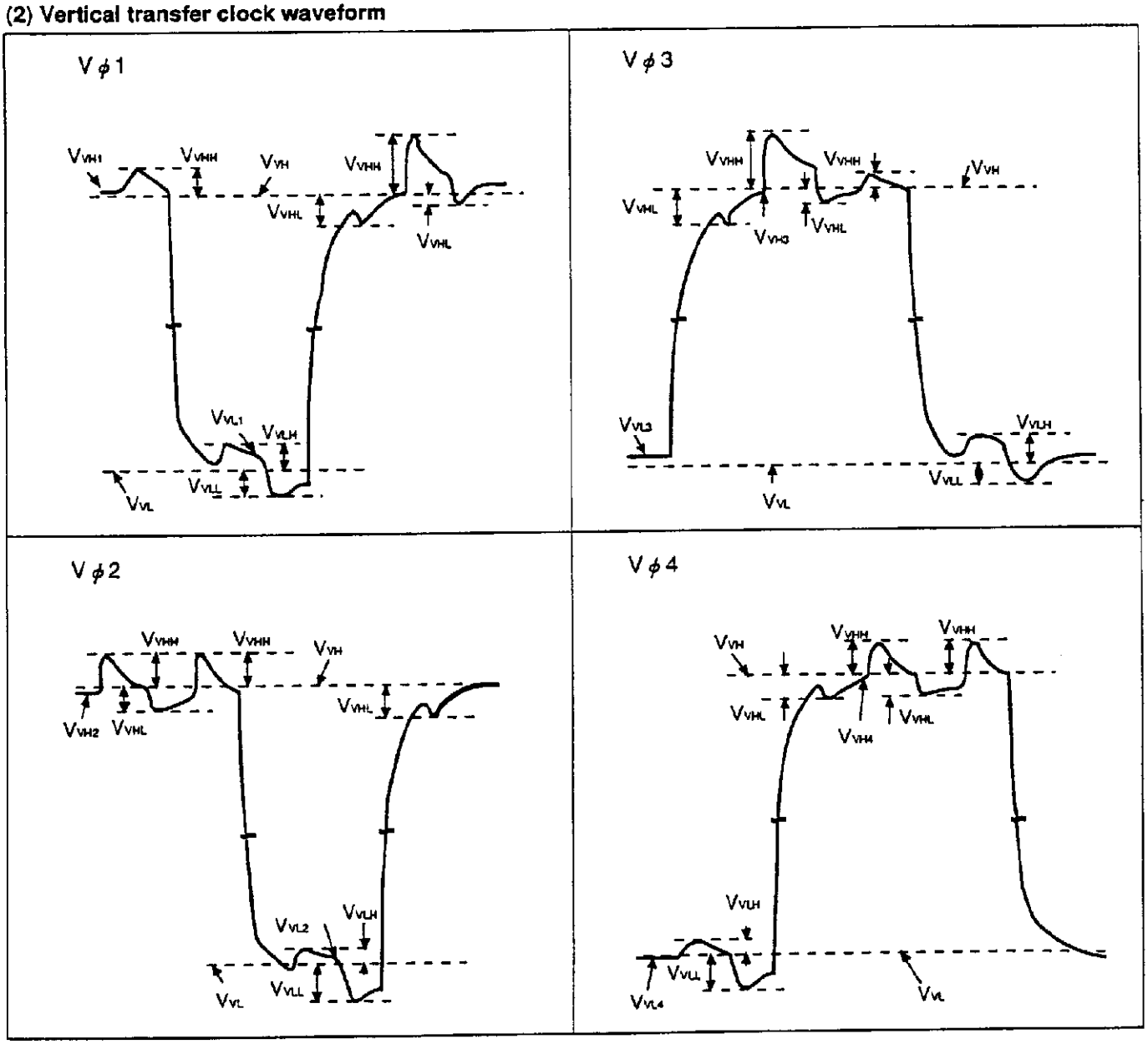
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Read out clock waveform

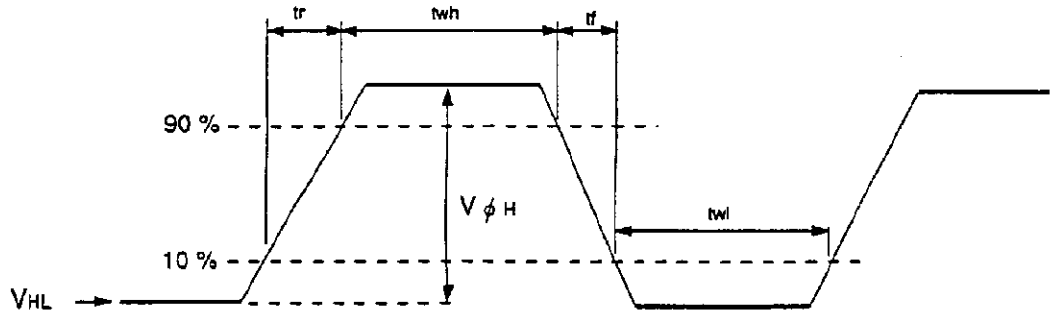


(2) Vertical transfer clock waveform

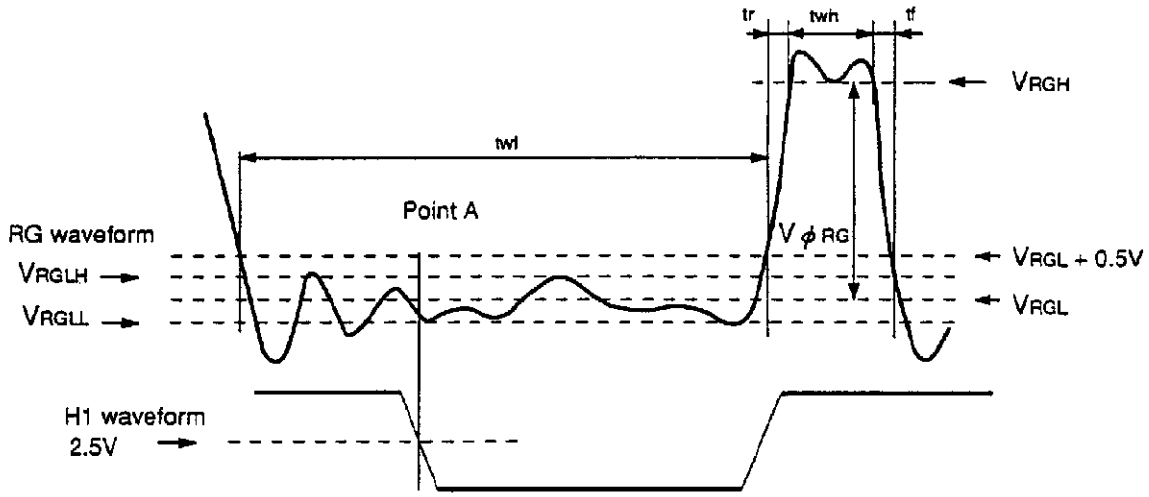


$V_{VH} = (V_{VH1} + V_{VH2})/2$
$V_{VL} = (V_{VL3} + V_{VL4})/2$
$V_{\phi V} = V_{VHn} - V_{VLn}$ (n = 1 to 4)

(3) Horizontal transfer clock waveform diagram



(4) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

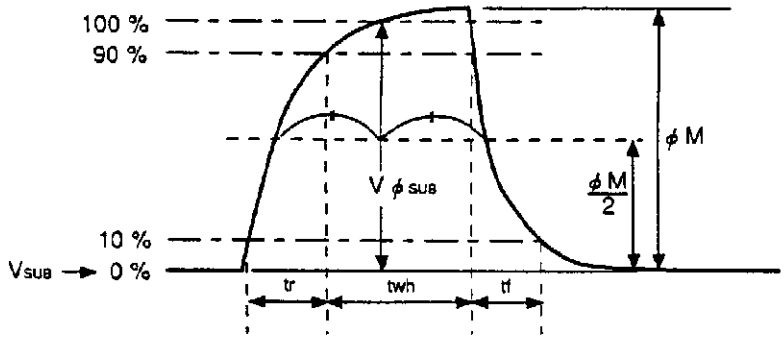
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL}.

$$V_{RGL}=(V_{RGLH}+V_{RGLL})/2$$

V_{RGH} is the minimum value for twh period.

$$V_{\phi RG}=V_{RGH}-V_{RGL}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item		Symbol	twh			twl			tr			tf			Unit	Remarks
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock		V_T	2.3	2.5						0.5			0.5		μs	During readout
Vertical transfer clock.		$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										15		250	ns	*7
Horizontal transfer clock	During imaging	$H\phi_1$	18	24		19.5	26			10	17.5		10	17.5	ns	*8
		$H\phi_2$	21	26		19	24			10	15		10	15		
	During parallel serial conversion	$H\phi_1$		6.41						0.01			0.01		μs	
		$H\phi_2$					6.41			0.01			0.01			
Reset gate clock		ϕ_{RG}	11	13			51			3			3		ns	
Substrate clock		ϕ_{SUB}	1.5	1.8							0.5			0.5	μs	During charge drain

* 7 When vertical transfer clock driver CXD1250 is in use.

* 8 tf≧tr−2 ns, and the crosspoint voltage (V_{CR}) of the $H\phi_1$ rise side of waveforms $H\phi_1$ and $H\phi_2$ must be at least 2.5V.

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	16	20		ns	*9

* 9 "two" is the overlap period of horizontal transfer clocks $H\phi_1$ and $H\phi_2$'s twh and twl.

Operating Characteristics

(Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	240	300		mV	1	
Saturation signal	Vsat	540			mV	2	Ta=60°C
Smear	Sm		0.009	0.015	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta=60°C
Dark signal shading	Δ Vdt			1	mV	6	Ta=60°C
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone Chart of Video Signal Shading

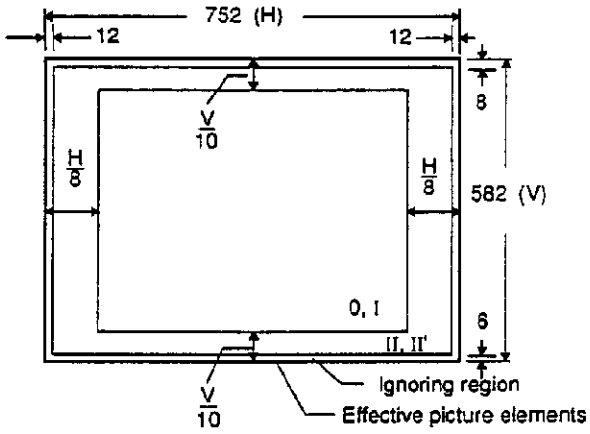


Image Sensor Characteristics Test Method

◎Test conditions

①Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are the typical value of the bias and clock voltage conditions.

②Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference, the values obtained at Ⓐ point in the figure of the Drive Circuit are utilized.

◎Definition of standard imaging conditions

①Standard imaging condition Ⅰ:(As imaging device) Use a pattern box (luminance 706 cd/m², color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t =1.0mm) as IR cut filter and image at F8. At this time, light intensity to sensor receiving surface is defined as standard sensitivity testing light intensity.

②Standard imaging condition Ⅱ: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard image condition Ⅰ. After selecting the electronic shutter mode at a 1/250s. shutter speed, measure the signal output (V_S) at the center of the screen and substitute in the following formula.

$$S = V_S \times \frac{250}{50} \text{ [mV]}$$

2. Saturation signal
   Set to standard imaging condition Ⅱ. Adjust light intensity to 10 times that of signal output average value (V_A=200mV), then test signal minimum value.

3. Smear
   Set to standard imaging condition Ⅱ. Adjust light intensity to 500 times that of signal output average value (V_A=200mV) with lens diaphragm at F5.6 to F8. Stop read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the maximum value VSm [mV] of signal output.

$$Sm = \frac{VSm}{200} \times \frac{1}{500} \times \frac{1}{10} \times 100(\%)(1/10V)$$

4. Video signal shading
   Set to standard imaging condition Ⅱ. Adjust light intensity to signal output average value (V_A=200mV) with lens diaphragm at F5.6 to F8. Then test maximum (Vmax [mV]) and minimum (Vmin [mV]) values of signal output.

   SH=(Vmax−Vmin)/200×100(%)

5. Dark signal
   Test signal output average value Vdt [mV] when the device ambient temperature is at 60℃ and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading
   Following 5, test maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of dark signal output.

   ΔVdt=Vdmax−Vdmin [mV]

7. Flicker

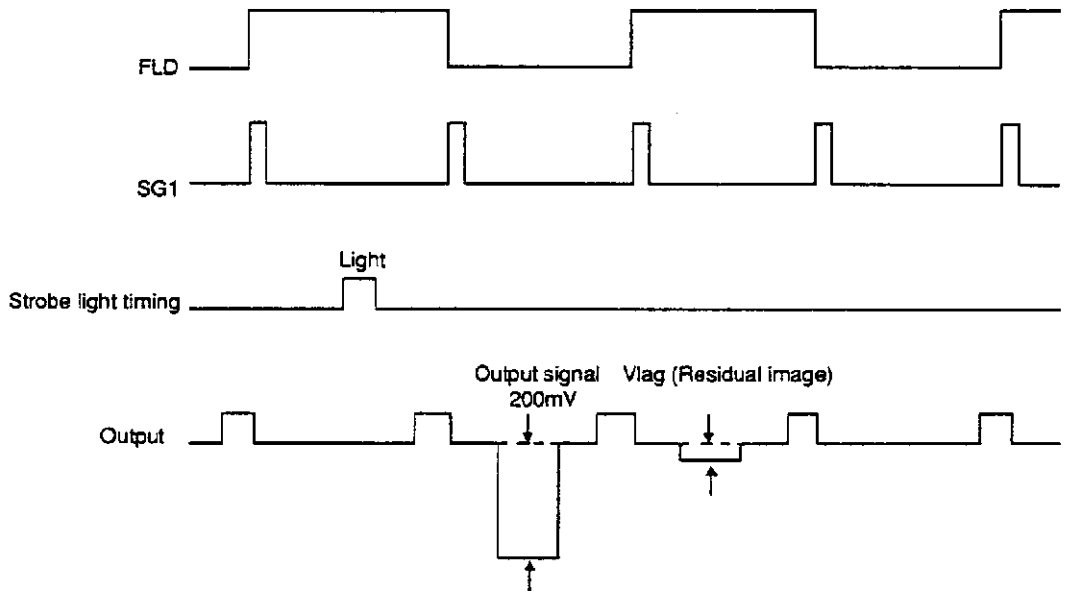
Set to standard imaging condition Ⅱ. Adjust light intensity to signal output average value (V_A=200mV). Then test the signal difference (ΔVf [mV]) between even field and odd field.

F=(ΔVf/200)×100(%)

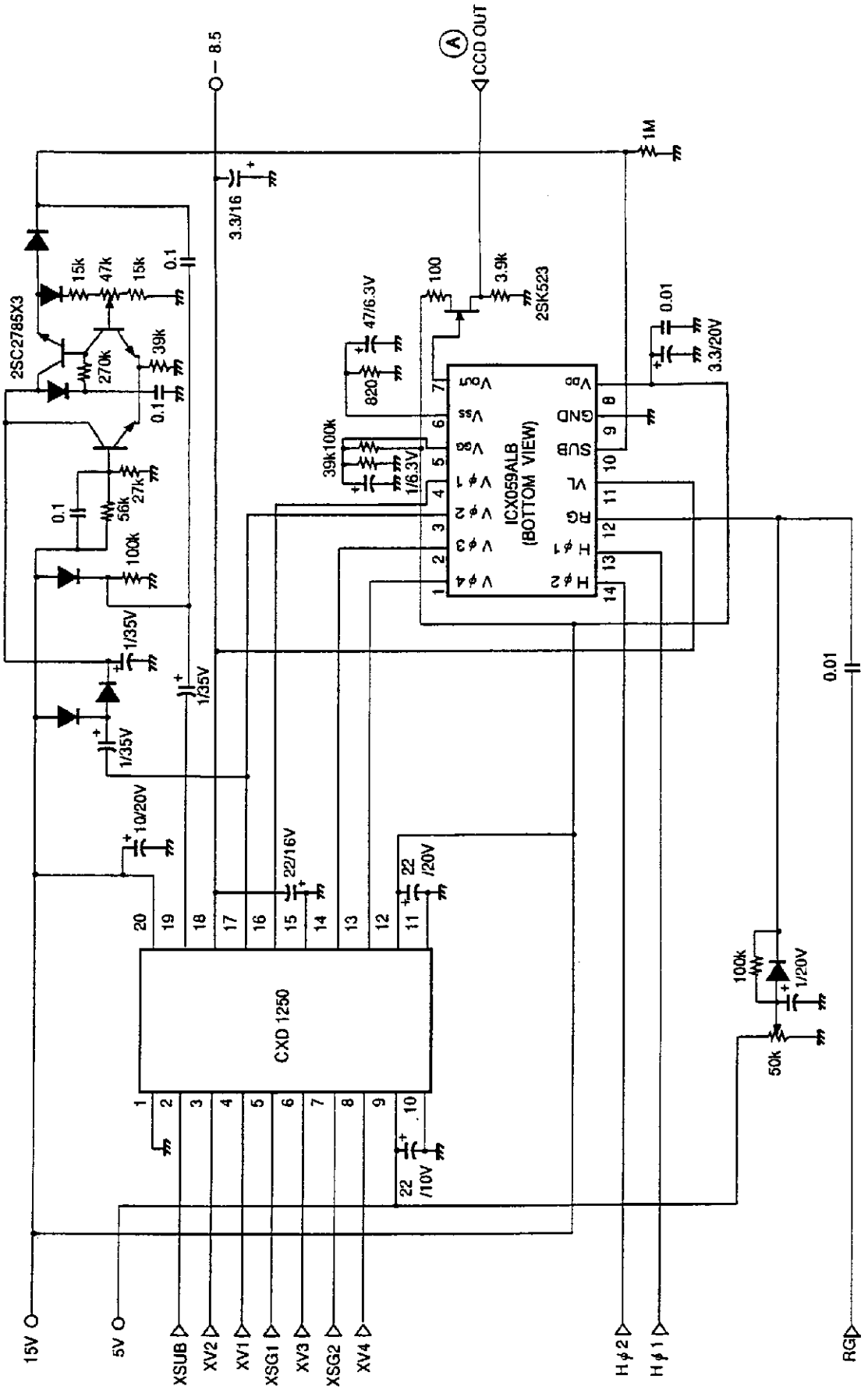
8. Residual image

Adjust signal output value by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Vlag).

Lag = (Vlag / 200) × 100 (%)



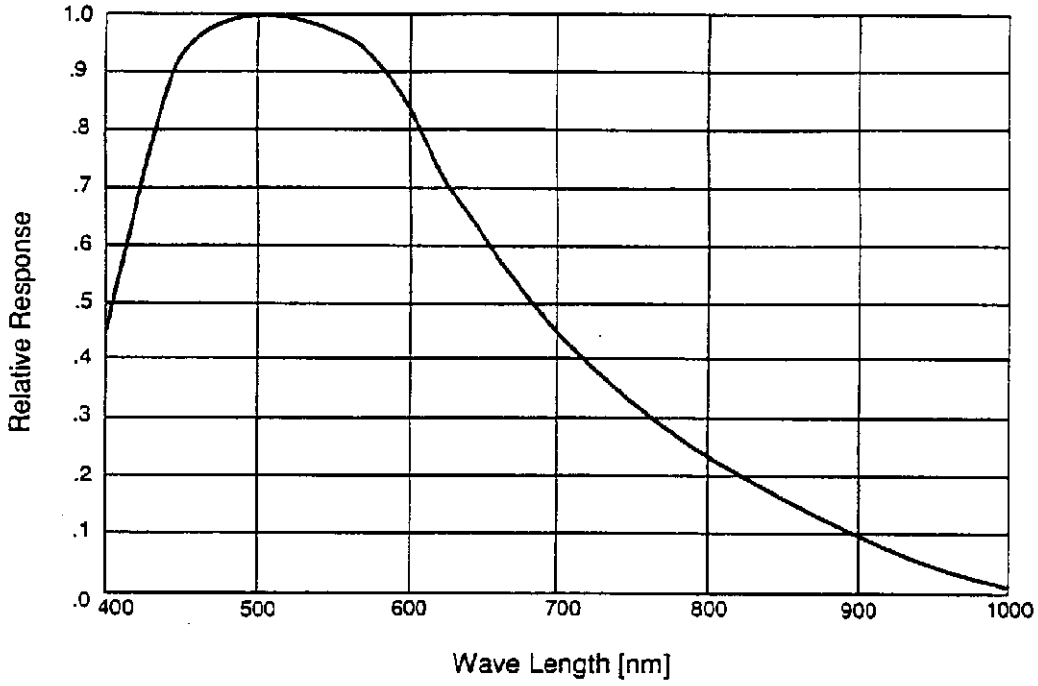
Drive Circuit



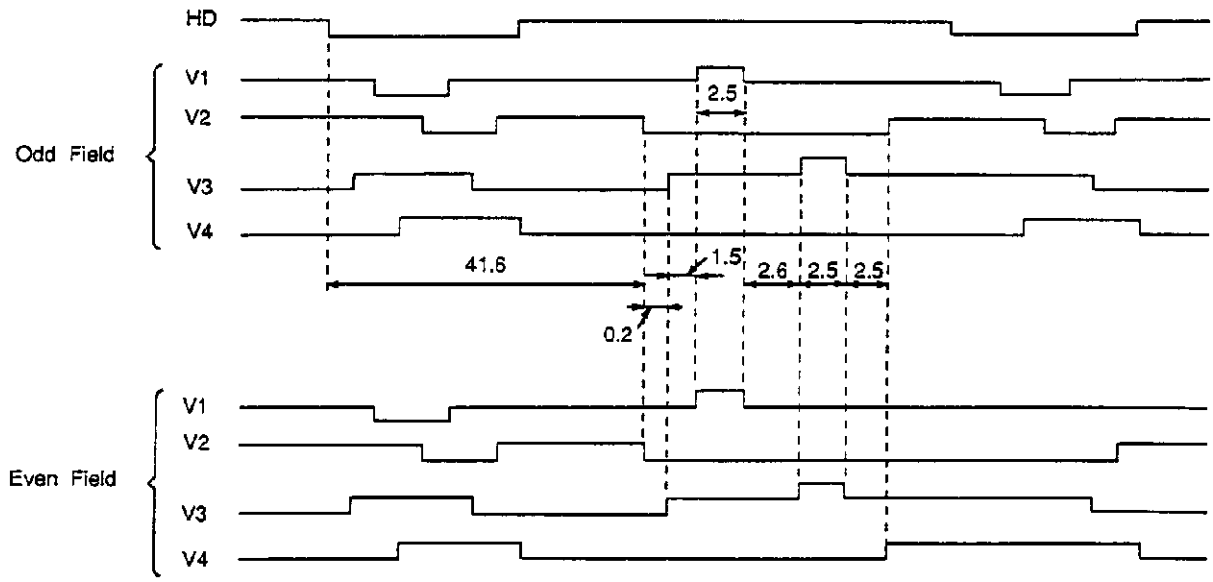
*) For head separate type camera, there are some case where this circuit can not apply.

Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

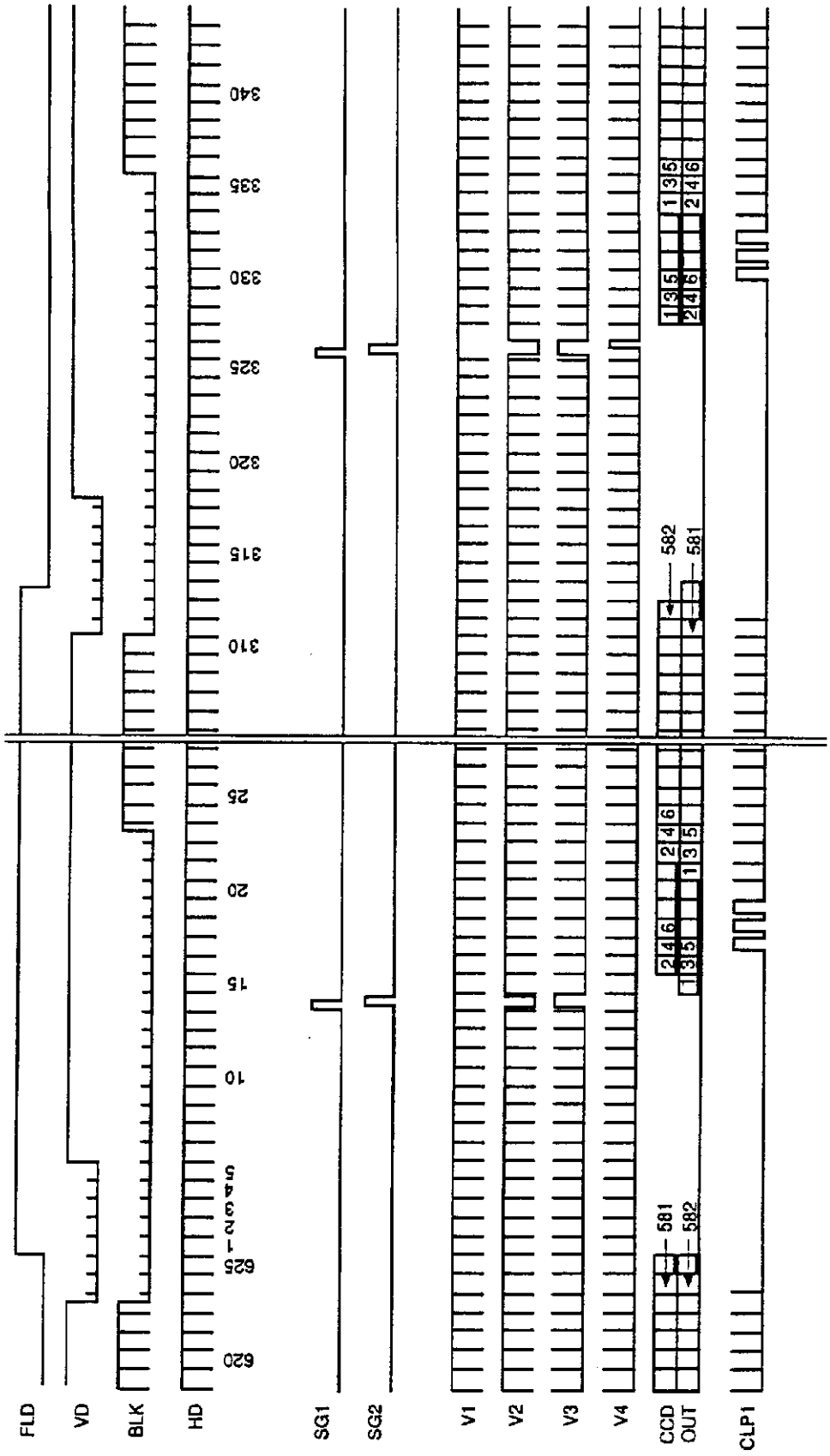


Using Read Out Clock Timing Chart

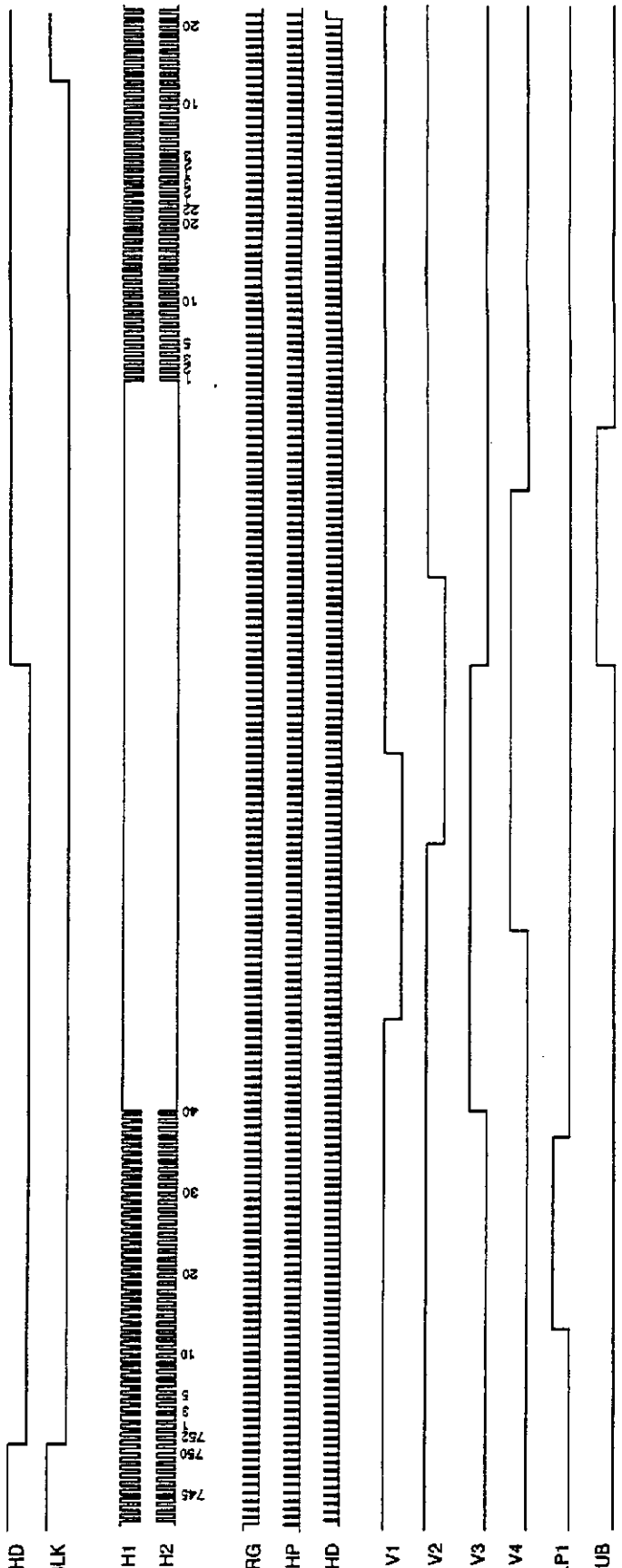


Unit : μs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizonral sync)



Notes on Handling

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended.)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

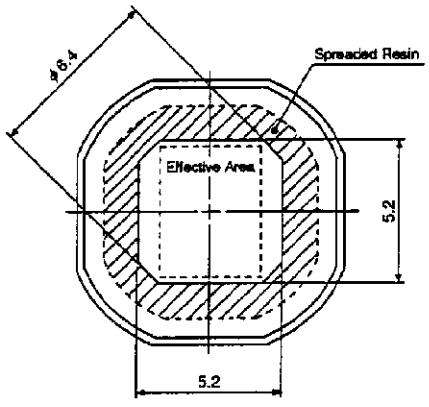
4) Do not expose to strong light (sun rays) for long periods.
For continuous using under cruel condition exceeding the normal using condition, consult our company.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to too much mechanical shocks.

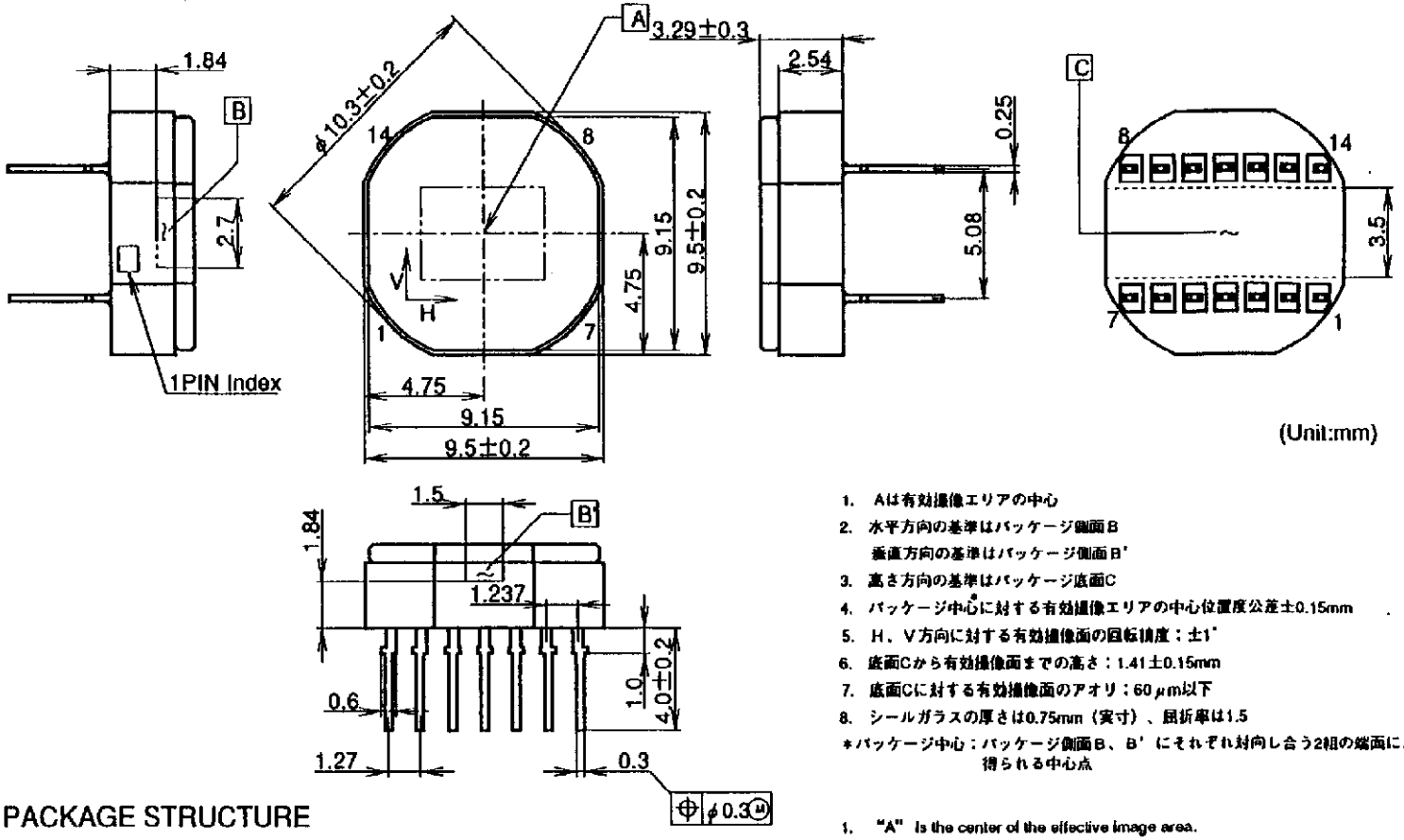
7) Eclipse (to get dark around the four corners of the picture) may occur when some object lenses are in the open iris state.

External Appearance



Package Outline Unit: mm

14pin DIP (200mil)



(Unit:mm)

1. Aは有効撮像エリアの中心
2. 水平方向の基準はパッケージ側面B
   垂直方向の基準はパッケージ側面B'
3. 高さ方向の基準はパッケージ底面C
4. パッケージ中心*に対する有効撮像エリアの中心位置度公差±0.15mm
5. H、V方向に対する有効撮像面の回転精度：±1°
6. 底面Cから有効撮像面までの高さ：1.41±0.15mm
7. 底面Cに対する有効撮像面のアオリ：60μm以下
8. シールガラスの厚さは0.75mm（実寸）、屈折率は1.5

＊パッケージ中心：パッケージ側面B、B'にそれぞれ対向し合う2組の端面により得られる中心点

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.6g

1. "A" is the center of the effective image area.
2. The point "B" of the package is the horizontal reference.
   The point "B'" of the package is the vertical reference.
3. The bottom "C" of the package is the height reference.
4. The center of the effective image area relative to the center of the package(*) is (H, V) =(0,0)±0.15mm.
5. The rotation angle of the effective image area relative to H and V is ±1°.
6. The height from the bottom "C" to the effective image area is 1.41±0.15mm.
7. The tilt of the effective image area relative to the bottom "C" is less than 60 μm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.

* Center of the package : The center is halfway between two pairs of opposite sides, as measured from "B", "B'".